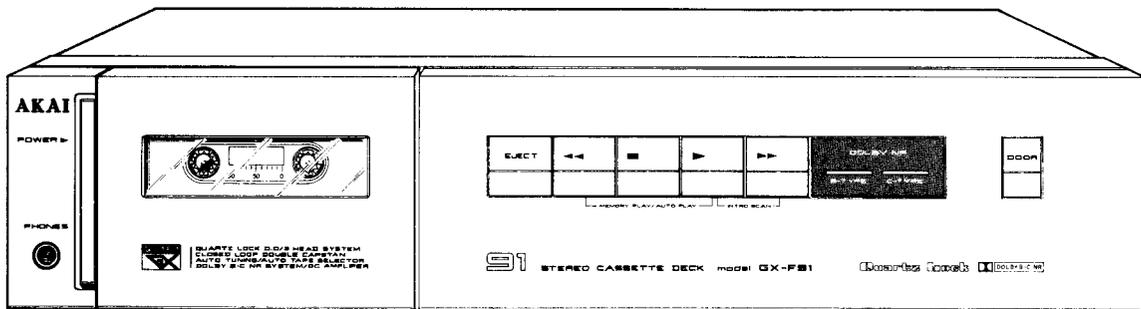


GX-F91

AKAI SERVICE MANUAL



STEREO CASSETTE DECK

MODEL **GX-F91**



STEREO CASSETTE DECK

MODEL GX-F91

THIS MANUAL IS APPLICABLE TO BOTH SILVER
AND PEARL SHADOW PANEL MODELS

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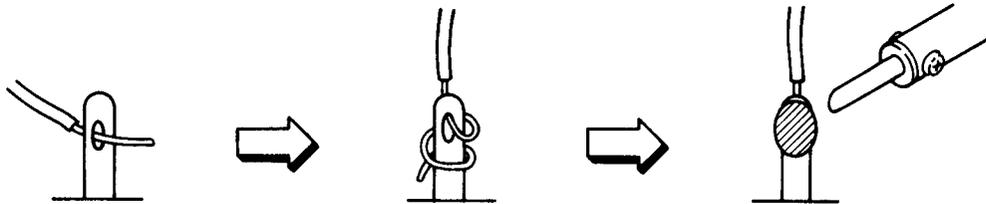
SAFETY INSTRUCTIONS

SAFETY CHECK AFTER SERVICING

Confirm the specified insulation resistance between power cord plug prongs and externally exposed parts of the set is greater than 10 Mohms, but for equipment with external antenna terminals (tuner, receiver, etc.) and is intended for **C** or **A**, specified insulation resistance should be more than 2.2 Mohms (ground terminals, microphone jacks, headphone jacks, line-in-out jacks etc.)

PRECAUTIONS DURING SERVICING

1. Parts identified by the **Δ** symbol parts are critical for safety.
Replace only with parts number specified.
2. In addition to safety, other parts and assemblies are specified for conformance with such regulations as those applying to spurious radiation. These must also be replaced only with specified replacements.
Examples: RF converters, tuner units, antenna selector switches, RF cables, noise blocking capacitors, noise blocking filters, etc.
3. Use specified internal wiring. Note especially:
 - 1) Wires covered with PVC tubing
 - 2) Double insulated wires
 - 3) High voltage leads
4. Use specified insulating materials for hazardous live parts. Note especially:
 - 1) Insulation Tape
 - 2) PVC tubing
 - 3) Spacers (Insulating Barriers)
 - 4) Insulation sheets for transistors
5. When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.), wrap ends of wires securely about the terminals before soldering.



6. Observe that wires do not contact heat producing parts (heatsinks, oxide metal film resistors, fusible resistors, etc.).
7. Check that replaced wires do not contact sharp edged or pointed parts.
8. Also check areas surrounding repaired locations.
9. Use care that foreign objects (screws, solder droplets, etc.) do not remain inside the set.

SECTION 1

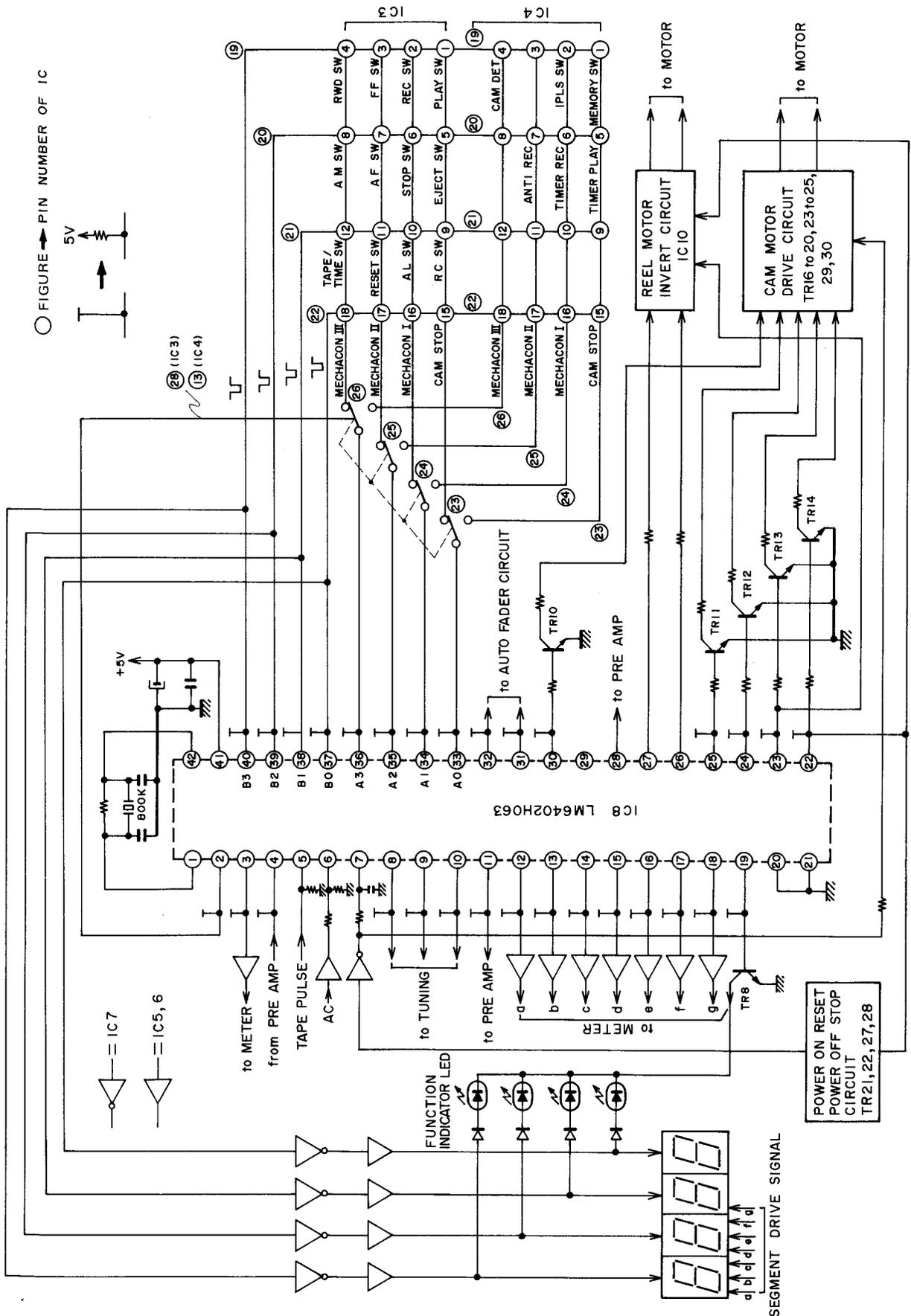
CIRCUIT OPERATION DESCRIPTION

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I. GX-F91 SYSCON CIRCUIT FUNCTIONS

1. GX-91 SYSCON BLOCK DIAGRAM





3. CONNECTION OF EACH TERMINAL OF IC (LC 7800)
FOR EXPANDING GX-F91 INPUT PORT

PIN	Items connected to IC3	Items connected to IC4							
1	PLAY SW	MEMORY SW							
2	REC SW	IPLS SW							
3	FF SW	OPEN ("H") (No connection)							
4	REW SW	R104 of cam motor drive circuit							
5	EJECT SW	TIMER PLAY SW							
6	STOP SW	TIMER REC SW							
7	AUTO FADER SW	ANTIREC SW							
8	AUTO MUTE SW	+5V (No connection)							
9	REC CANCEL SW	+5V (No connection)							
10	AUTO LOADING SW	+5V (No connection)							
11	RESET SW	+5V (No connection)							
12	TAPE/TIME SW	+5V (No connection)							
13	GND	MICON PIN2							
14	GND	GND							
15	C-stop signal of cam motor drive circuit								
16	TUNING MICON PIN 35	(For Mechacontrol Signal When TUNING)							
17	TUNING MICON PIN 36								
18	TUNING MICON PIN 3								
Mechacontrol signal from TUNING MICON									
	TUNING MICON PIN	SYSCON MICON PIN	NON OPER- ATION	STOP	FF	REW	REC/ PLAY	REC/ PAUSE	TEST OFF
	35 (O ₀) MECHACON I	34 (A1)	L	H	L	H	L	H	L
	36 (O ₁) MECHACON II	35 (A2)	L	L	H	H	L	L	L
	3 (O ₂) MECHACON III	36 (A3)	L	L	L	L	H	H	L
19	SYSCON MICON PIN 40 (B3)								
20	SYSCON MICON PIN 39 (B2)								
21	SYSCON MICON PIN 38 (B1)								
22	SYSCON MICON PIN 37 (B0)								
23	SYSCON MICON PIN 33 (A0)								
24	SYSCON MICON PIN 34 (A1)								
25	SYSCON MICON PIN 35 (A2)								
26	SYSCON MICON PIN 36 (A3)								
27	+5V							+5V	
28	MICON PIN 2							+5V	

II. AUTO TUNING SYSTEM

1. AUTO TUNING BLOCK DIAGRAM

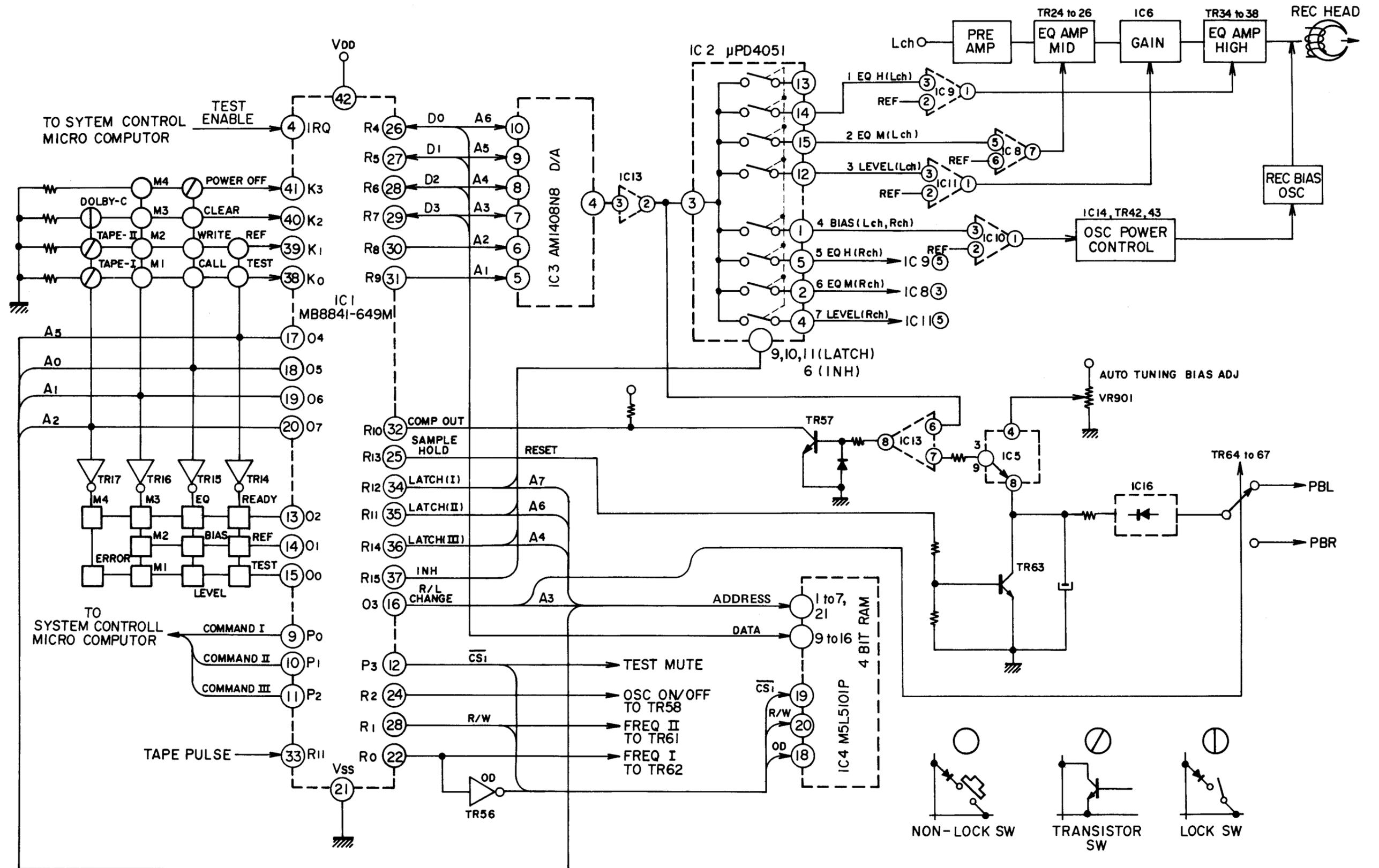


Fig. 1-3 Auto Tuning Block Diagram

2. MI-COM IN/OUT PORT

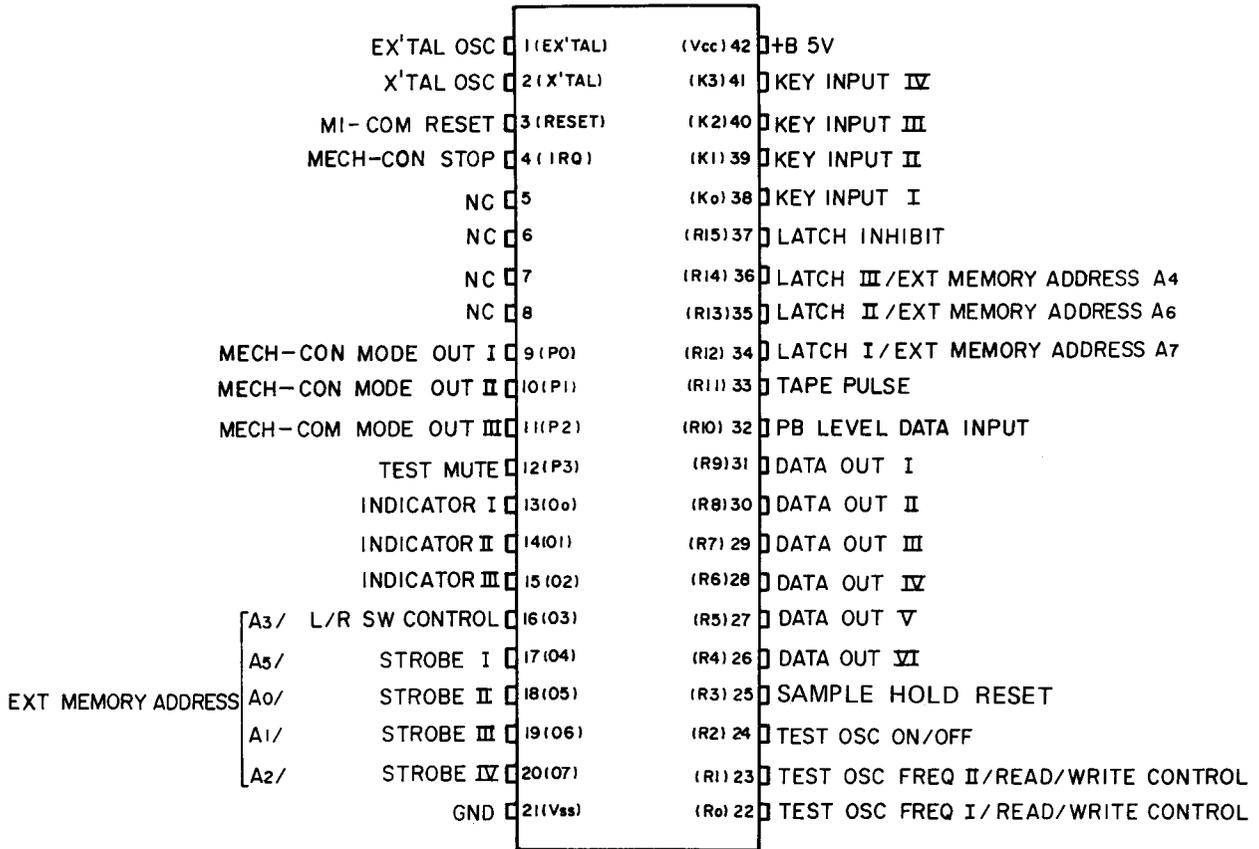


Fig. 1-4 IC1 MB8841-649M

3. DESCRIPTION OF THE TUNING MI-COM IN/OUT PORTS (MB8841-649M)

Pin No.	Port		Description																												
1 2	E X'TAL X'TAL	E X'tal X'tal	X'tal oscillator terminal. X'tal oscillator terminal																												
3	RESET	$\overline{\text{RESET}}$	Mi-Com Reset input terminal Reset when "L"																												
4	IRQ	TEST ENABLE	The STOP MODE signal is supplied from the MECH-CON. Normally is at "H" except that this is set to "L" 3 seconds after the power is turned on or when the STOP mode is established. Accepts Auto Tuning only when set to "L". Is at "H" during the auto tuning, which, however, will be stopped if "L" input is encountered.																												
5 6 7 8	SO SI SC/TO TC		Not in use.																												
9 10 11	P ₀ P ₁ P ₂	Mech-Con I Mech-Con II Mech-Con III	The mech. control outputs I, II and III allow 6 different modes (0) through (5) as shown in the table below. Without the tuning operation, the MECH-CON outputs I, II and III are all "0", establishing the (0) mode (tuning OFF). During "TEST", any one of the modes (1) through (5) is established. When the test is complete, the mode (5), or (REC/PAUSE), is established, and then the mode (0), or (Tuning OFF), after the lapse of 50 msec.																												
<table border="1"> <thead> <tr> <th>MODE</th> <th>(0) Tuning OFF</th> <th>(1) STOP</th> <th>(2) FF</th> <th>(3) RWD</th> <th>(4) REC/PB</th> <th>(5) REC/ PAUSE</th> </tr> </thead> <tbody> <tr> <td>Mech-Con I</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>Mech-Con II</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>Mech-Con III</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> </tbody> </table>				MODE	(0) Tuning OFF	(1) STOP	(2) FF	(3) RWD	(4) REC/PB	(5) REC/ PAUSE	Mech-Con I	0	1	0	1	0	1	Mech-Con II	0	0	1	1	0	0	Mech-Con III	0	0	0	0	1	1
MODE	(0) Tuning OFF	(1) STOP	(2) FF	(3) RWD	(4) REC/PB	(5) REC/ PAUSE																									
Mech-Con I	0	1	0	1	0	1																									
Mech-Con II	0	0	1	1	0	0																									
Mech-Con III	0	0	0	0	1	1																									
12	P ₃	TEST MUTE	Is at "H" during "TEST", causing the PB output to be muted. Also, during "TEST", the "H" output places the external memory (IC4) in a non-selective state ($\overline{\text{CS}}_1$) Mutes the TEST signal output with a mode other than the TEST mode.																												
13 14 15	O ₀ O ₁ O ₂	INDICATOR I INDICATOR II INDICATOR III	Are indicator outputs that provide dynamic indicator display in response to strobe signals from Pins 17 ~ 20 (O ₄ ~ O ₇). The "L" outputs cause the indicators to come on.																												
16	O ₃	L/R SWITCH CONTROL	Causes switching between Lch and Rch for the PB signal to the level level detection circuit.																												
17 18 19 20	O ₄ O ₅ O ₆ O ₇	STROBE I STROBE II STROBE III STROBE IV	Causes a 4 bit signal to be output through strobe oscillation with coordinated timing. This signal permits dynamic display of each key input and indicator output.																												
<p style="text-align: right;">DUTY CYCLE 1:5</p>																															

Pin No.	Port		Description																																								
21	V _{SS}	V _{SS}	GND																																								
22 23	R ₀ R ₁	TEST OSC FREQ I TEST OSC FREQ II	Provides the output signal that controls the oscillation frequency of the TEST signal. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td></td> <td>1 kHz</td> <td>7 kHz</td> <td>13 kHz</td> <td>15 kHz</td> </tr> <tr> <td>R₀</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>R₁</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> </table>		1 kHz	7 kHz	13 kHz	15 kHz	R ₀	0	1	0	1	R ₁	0	0	1	1																									
	1 kHz	7 kHz	13 kHz	15 kHz																																							
R ₀	0	1	0	1																																							
R ₁	0	0	1	1																																							
	R ₀	READ OUT CONTROL (OD)	Controls the IC4's data read output. "H" : No Read "L" : Read OK.																																								
	R ₁	READ/WRITE CONTROL	Controls the external memory (IC4). "H" : Read "L" : Write																																								
24	R ₂	TEST OSC ON/OFF	Provides the control signal for oscillating the TEST signal during the TEST mode. "H" : TEST OSC "ON" "L" : TEST OSC "OFF"																																								
25	R ₃	SAMPLE HOLD RESET	Discharges the condenser C65 that sample-holds the PB output that has been integrated. Note that this is done on a per-test basis. "H" : Reset																																								
26 27 28 29 30 31	R ₄ R ₅ R ₆ R ₇ R ₈ R ₉	DATA OUT I DATA OUT II DATA OUT III DATA OUT IV DATA OUT V DATA OUT VI	Provides 6 bit signals to generate 64 different step signals. The 64 signals are subjected to D/A conversion for tuning at each level.																																								
32	R ₁₀	PB LEVEL DATA INPUT	The PB output signal is detected and then compared with the reference Voltage. The inverted signal from the comparator (IC13) is supplied to the Mi-Com. Based on this signal, the PB level is detected for subsequent data processing by the Mi-Com.																																								
33	R ₁₁	$\overline{\text{INT}}$	Provides the pulse input (TAPE PULSE input) required to rewind back to the tuning start point.																																								
34 35 36	R ₁₂ R ₁₃ R ₁₄	LATCH I LATCH II LATCH III	Provides 3 bit signals to manipulate the 8 circuits switch (IC2) separately and route the D/A converted DATA OUT (Mi-Com outputs R ₄ ~ R ₉ 6 bits) through time sharing. $(\text{Bias}) + [(\text{Level}) + (\text{EQ H}) + (\text{EQ M})] \times (\text{L} + \text{R}) = 7$ <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td></td> <td>BIAS</td> <td colspan="2">EQ H</td> <td colspan="2">EQ M</td> <td colspan="2">LEVEL</td> </tr> <tr> <td></td> <td>R</td> <td>L</td> <td>R</td> <td>L</td> <td>R</td> <td>L</td> <td>R</td> </tr> <tr> <td>R₁₂</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>R₁₃</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>R₁₄</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> </table>		BIAS	EQ H		EQ M		LEVEL			R	L	R	L	R	L	R	R ₁₂	0	1	1	0	0	1	1	R ₁₃	0	0	0	1	1	1	1	R ₁₄	1	0	1	0	1	0	1
	BIAS	EQ H		EQ M		LEVEL																																					
	R	L	R	L	R	L	R																																				
R ₁₂	0	1	1	0	0	1	1																																				
R ₁₃	0	0	0	1	1	1	1																																				
R ₁₄	1	0	1	0	1	0	1																																				
37	R ₁₅	LATCH INHIBIT	Makes invalid all signals appearing at R ₁₂ ~ R ₁₄ and causes the switch (IC2) controlled by these signals to be opened.																																								
38 39 40 41	K ₀ K ₁ K ₂ K ₃	KEY INPUT I KEY INPUT II KEY INPUT III KEY INPUT IV	Key switch inputs. Type of tape and Dolby ON/OFF detection input.																																								

Pin No.	Port		Description
42	V _{CC}	V _{CC}	+5V Power Supply
16 17 18 19 20 34 35 36	O ₃ O ₄ O ₅ O ₆ O ₇ R ₁₂ R ₁₃ R ₁₄	} EXT MEMORY ADDRESS	} External memory addresses (IC4)

4. AUTO TUNING SYSTEM DESCRIPTION

The reference tape being used by AKAI has characteristics that are most common with tapes currently available on the market.

With due consideration given to the difference in characteristics between tapes, it has been found that correction of ± 9.6 dB can be made with reference to the center value by providing 64 steps (0.3 dB per step) and that a variety of tapes can be supported by performing tape tuning.

The auto tuning involves:

- 1) Level adjustment
- 2) Bias adjustment
- 3) Equalizer Middel (EQM) adjustment
- 4) Equalizer High (EQH) adjustment

The level and equalizer adjustments are made in 64 steps (0.3 dB per step).

4-1. Auto Tuning Procedure

- 1) Insert the tape.
- 2) Detect the pack and tape type (auto tape selector).
- 3) The TEST start switch ON.
- 4) Detect the auto tuning bias level.
- 5) Perform REC/PB for the reference signal and determine whether the portion of tape is leader tape or one coated with magnetic material.
 - (a) In the case of leader tape, the error detection is followed by 64-count FF before tuning is started (REC PLAY MODE).
 - (b) If the portion is coated with magnetic mate-

rial, tuning is started immediately (REC PLAY MODE).

- 6) Make a coarse adjustment of REC/PB level. (Lch & Rch)
- 7) Make bias adjustment. (Rch only)
- 8) Make a fine adjustment of REC/PB level. (Lch and Rch).
- 9) Adjust the equalizer. (Lch and Rch)
- 10) If the above adjustments have been made satisfactorily, then rewind the tape back to the start point and establish the "READY standby" state via Rec/Pause.
- 11) If an error occurs during the tuning procedure, first perform the FF operation and then repeat the adjustments in 6) through 9).
- 12) If an error still occurs, then rewind the tape back to the start point and establish the STOP mode with ERROR displayed.

4-2. After Tuning

With "READY" displayed, it is possible to perform REC/PLAY directly with the data associated with the test.

The READY state is not cancelled, whichever operation key is depressed, unless the tape is changed or the TEST key is depressed again.

The data associated with the test can be written into any of the channels (memory 1 through 4).

Because of use of CMOS RAM and Ni-Cd batteries, the memory contents can be preserved for more than 20 days even if the power is turned off.

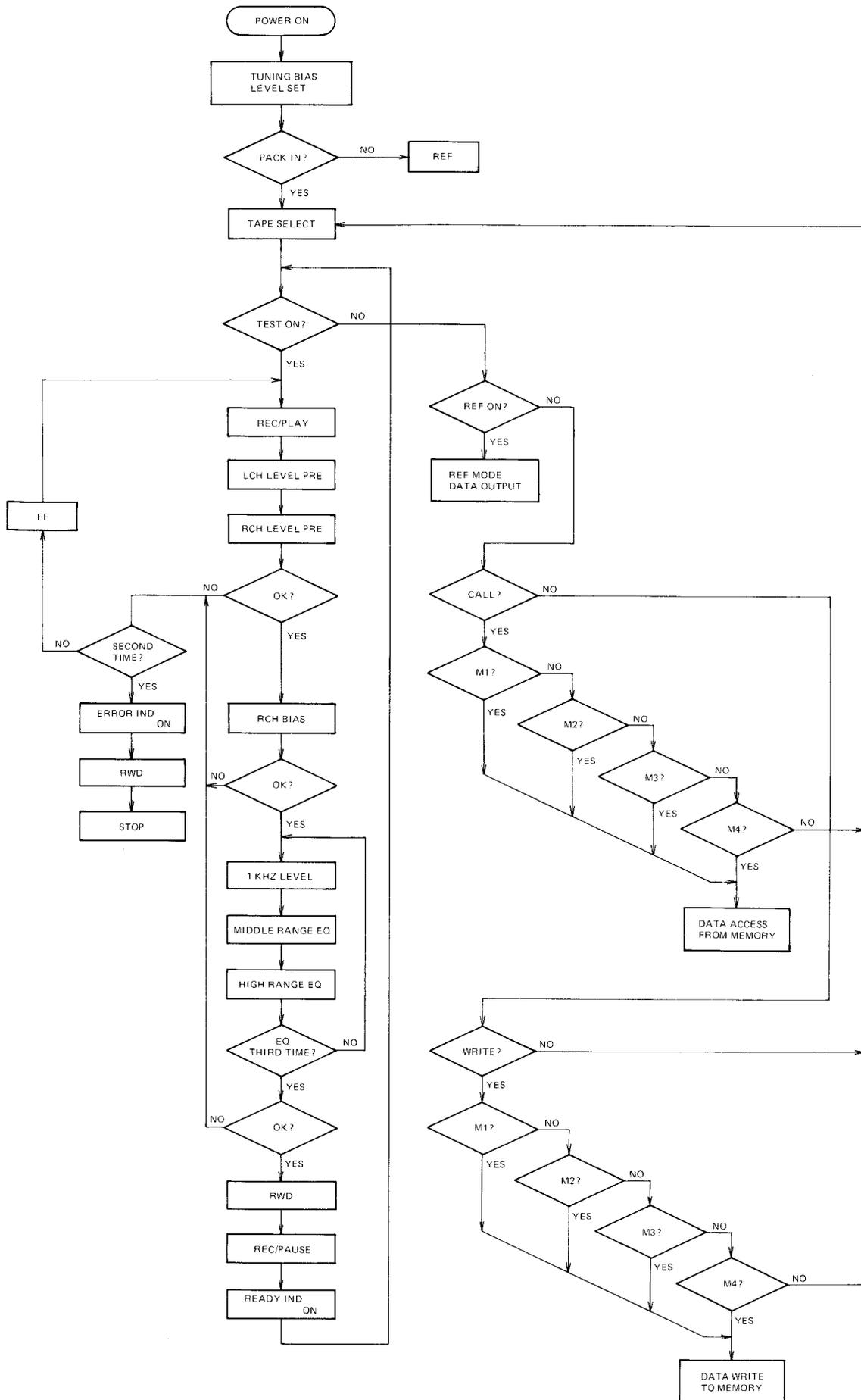


Fig. 1-5 Outline Flow Chart of Auto Tuning System

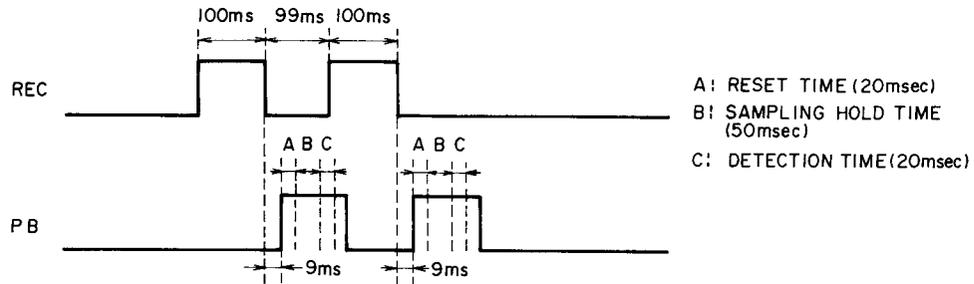


Fig. 1-6

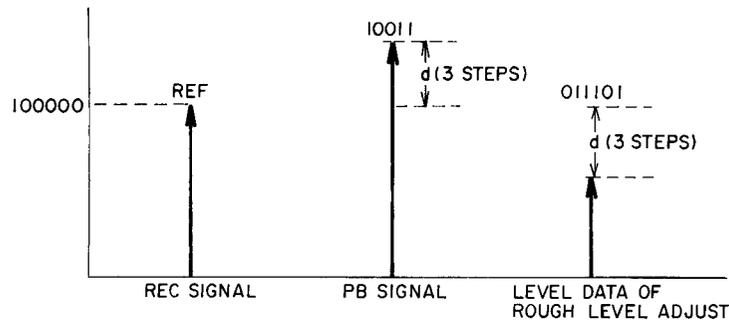


Fig. 1-7

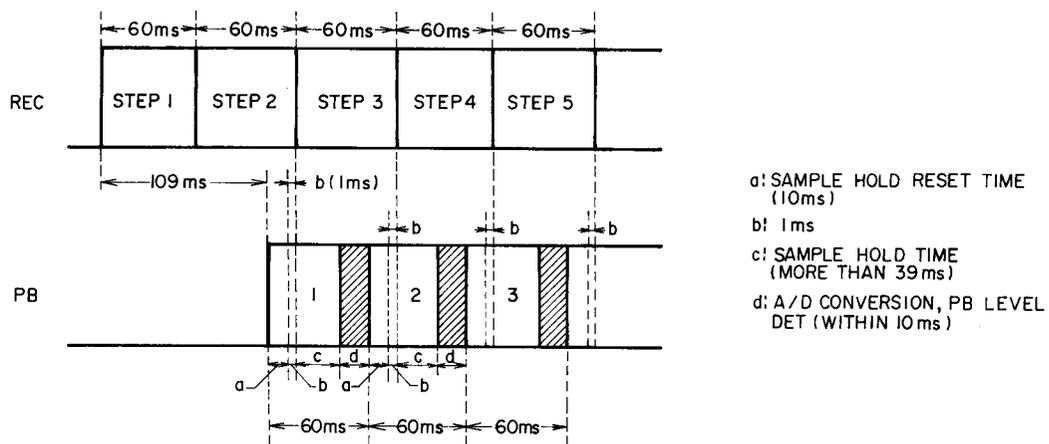


Fig. 1-8

4-3. Coarse Adjustment of REC/PB Levels (Refer to Figs. 1-6, 7)

The coarse level adjustment is made first on Lch and then on Rch.

A 1 kHz signal is recorded and played back with the standard REF value ($R_4 \sim R_9 : 100000, -27 \text{ VU}$), and the REC/PB level is subjected to A/D conversion and then compared with the REF value. The difference is then added to the REF value, the result of which is used as the REF value (level) for the next test. Figure 1-6 shows the REC/PB timing.

With the lapse of 109 msec after the recording, the PB output is made available. This output is compared in IC13 and then subjected to A/D conversion as test data to compute the difference (the number of steps) from 100000. For example, if the test data is 100011, the difference is 3 steps and thus it is necessary to set to the value (011101) which is the result of subtracting 3 (steps) from the recording

data. This data is routed via a switch (IC2) to IC11 to analog-hold it there. (See Figure 1-7.)

4-4. Bias Tuning (Refer to Figs. 1-8, 9, 10)

- 1) For bias tuning, a 1 kHz signal is recorded at a level obtained through the coarse level adjustment. The equalizer setting must be made with the reference data prior to recording.
- 2) For bias, continuous 16 step recording must be made at intervals of 4 steps, starting at 000000. One step takes 60 msec.
- 3) Figure 1-8 shows the REC/PB timing.

The REC bias data is switched 1 msec after the end of "a". The sample-holding of the PB signal takes place during "c". In "d", the PB level is subjected to A/D conversion, and the level associated with each step is determined within the Mi-Com.

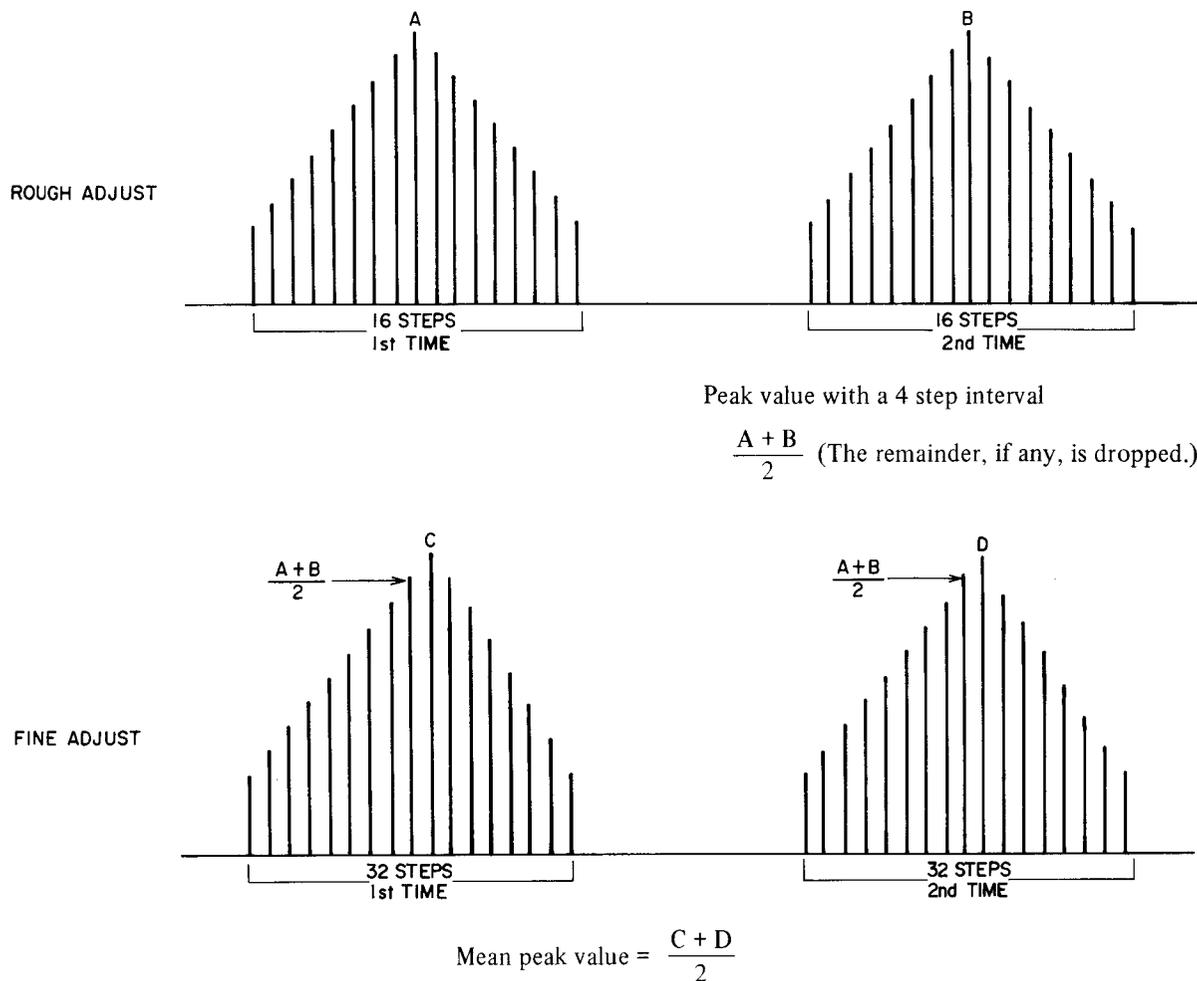


Fig. 1-9

- 4) The 16 step REC/PB is carried out twice and the average of the peak values is computed.
- 5) The range over which the amount of bias varies in ± 16 steps is determined, with the computed average value being at the center.
- 6) Recording and playback is made twice on a per-step basis, starting at the "lower" end of the variation range. Then, the average of the peak values in 32 steps is computed.
- 7) The value which is 4 steps higher than the data obtained by the fine adjustment is used as the bias setting.
- 8) Head Room adjustment system
The bias setting can be varied by means of the AT bias volume (VR 901) on the front panel. The AT bias set point is detected each time the test is started, thereby determining the number of excess steps. Figure 1-10 gives the change rate.

Change rate		Upon completion of tuning
Step	[%]	Step Over
+7	+21	10
+6	+18	9
+5	+15	8
+4	+12	7
+3	+9	6
+2	+6	5
+1	+3	4
0	0	4
-1	-3	4
-2	-6	3
-3	-9	2
-4	-12	1
-5	-15	0
-6	-18	-1
-7	-21	-2

If the change rate is 3% per step, then a change of $\pm 21\%$ can be achieved.

Fig. 1-10

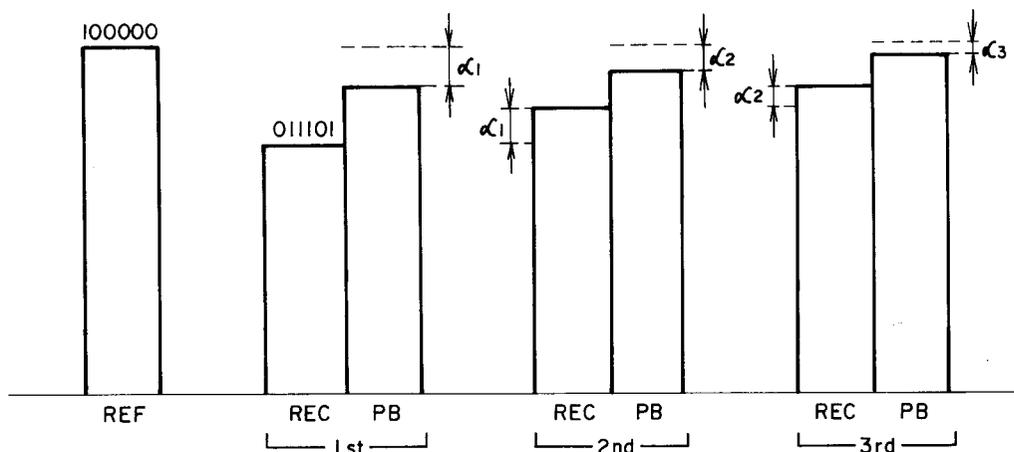


Fig. 1-11

4-5. Level Tuning (Refer to Fig. 1-11)

- 1) A 1 kHz signal is recorded and played back with the data (011101) obtained in the coarse level adjustment and the difference from the original REF value (100000) is determined, which is then added to the first recording level data. The result is then used as the second recording level data.
- 2) The same test is further repeated twice (i.e., a total of three tests are to be conducted.)
- 3) If after three tests the data obtained is outside the specified range, two additional tests need to be conducted.
- 4) If the data is still out of the specified range after the fifth recording/playback, an error is assumed.
- 5) If "Dolby ON" is detected, Δlevel is reduced to $1/2$, and $\Delta\text{level}/2$ is used as the amount of level correction (α).

4-6. Equalizer Tuning

- 1) The proper level must be set through recording and playback with 7 kHz (middle range), and 14 kHz (high range, with normal tape) or 15 kHz (high range, with CrO₂ or metal tape).

2) The REF value used is 100000.

3) In addition, the information in 4-5 "Level Tuning" also applies here.

4-7. Mute Circuit (During Tuning)

(Refer to Fig. 1-12)

When the test key is depressed, the Mi-Com enters the test mode with its pin ⑫ set to "H". This activates TR11 and TR12 on the meter drive PCB, which in turns on TR45 and TR47 (on the Pre Amp PCB) via D17 and D18, thereby causing the gates of TR44 and TR46 to be at negative voltage. As a result, both TAPE and SOURCE are shut off. Thus, the test signal is muted and therefore not made available at the LINE OUT during the test.

On the other hand, when pin ⑫ of Mi-Com goes to "H", TR1 of the Pre Amp is activated, causing the Rec input (Line/DIN) to go to ground. In addition, TR2 is turned on, deactivating TR3. As a result, the test signal from TEST OSC is supplied to the Rec Line Amp via R9.

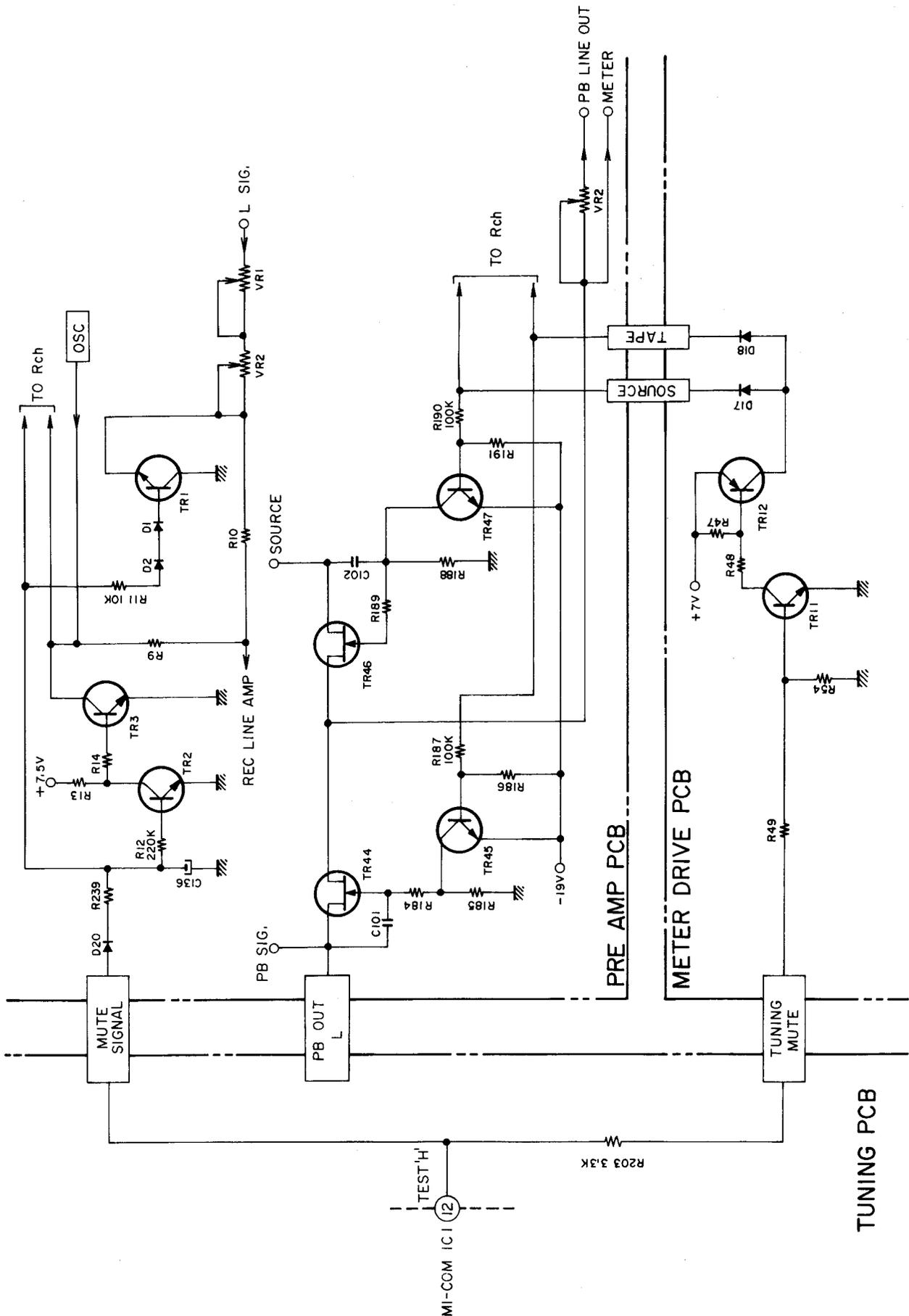


Fig. 1-12 Mute Circuit

4-8. Reference Signal Generation Circuit (Refer to Fig. 1-13)

This circuit generates the reference signals (1K, 7K, 13K and 15K) at the time of tuning. The oscillation frequency of the TEST signal is controlled by way of pins 22 and 23 (OSC, FRQ I and II) of the Mi-Com. The 2 bit signal is used to

generate 1K, 7K, 13K and 15K.

In the above truth table, "H" causes TRs 58, 61 and 62 to be activated.

13 kHz is used for NORMAL TEST, while 15 kHz is used for CrO₂ or METAL.

The reference oscillation output level is adjusted by VR9.

No.		OSC stopped	1 kHz	7 kHz	13 kHz	15 kHz		
24	OSC ON/OFF	L	H	H	H	H	⇨	
22	FRQ I		L	L	H	H		TR58
23	FRQ II		L	H	L	H		TR61 TR62

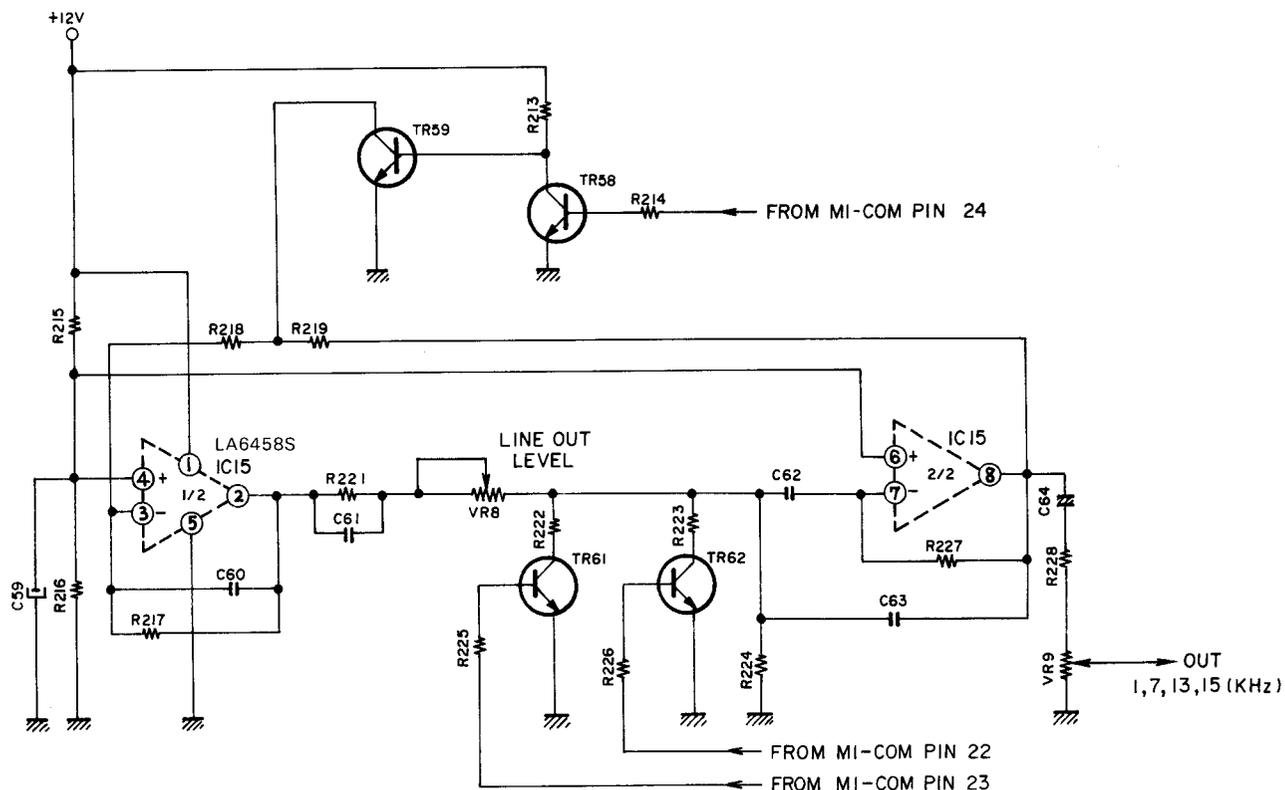


Fig. 1-13

4-9. A/D Conversion Circuit (Refer to Fig. 1-14)

The purpose of this circuit is to detect the REC/PB level at the time of auto tuning.

- 1) Switching between Lch and Rch is made by turning TR64 on/off by way of Mi-Com's pin 16 (L/R change-over SW control). (Lch : H ; Rch : L)
- 2) VR10 is for adjusting the A/D conversion level.

- 3) Pins ③ and ④ of IC5 are set to ON and the reference PB output level is supplied to pin ⑫ of the Mi-Com. Then, pins ⑧ and ⑨ of IC5 are set to ON and comparison is made with the previous data.
- 4) The PB output is integrated by the operation of TR63, and C65 is discharged for each test through resetting.

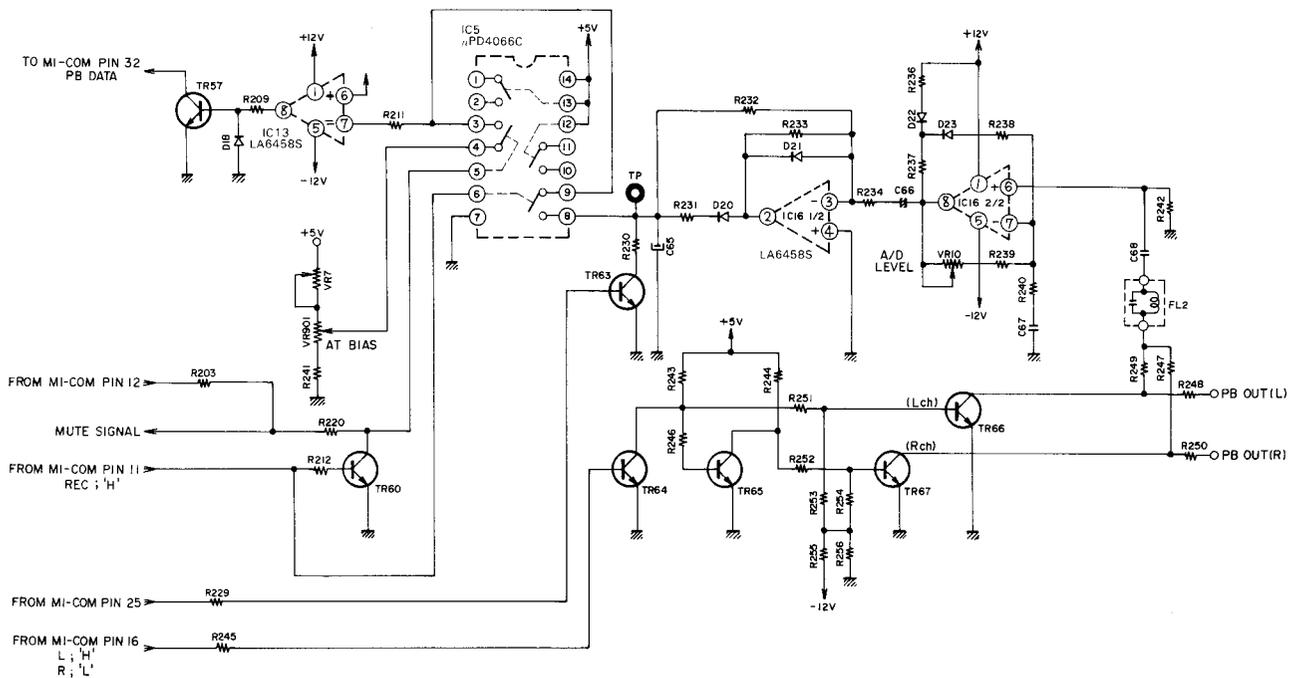


Fig. 1-14

4-10. Bias OSC Power Supply (Refer to Fig. 1-15)

The purpose of this circuit is to supply power to the bias OSC.

1) Bias

- (1) The AC component is removed by C50 and C51.
- (2) VR5 (METAL) and VR6 (CrO₂) are for adjusting the bias.
- (3) The output is killed by TR44. (OFF during REC mode)
- (4) Oscillator voltage is changed through control by TR43.

2) Erase head

- (1) Settings are made based on METAL. For NORMAL or CrO₂, voltage is changed by means of TR46 and TR48, respectively.
- (2) The output is killed by TR51. (OFF during REC mode)
- (3) Oscillator voltage is changed through control by TR50.

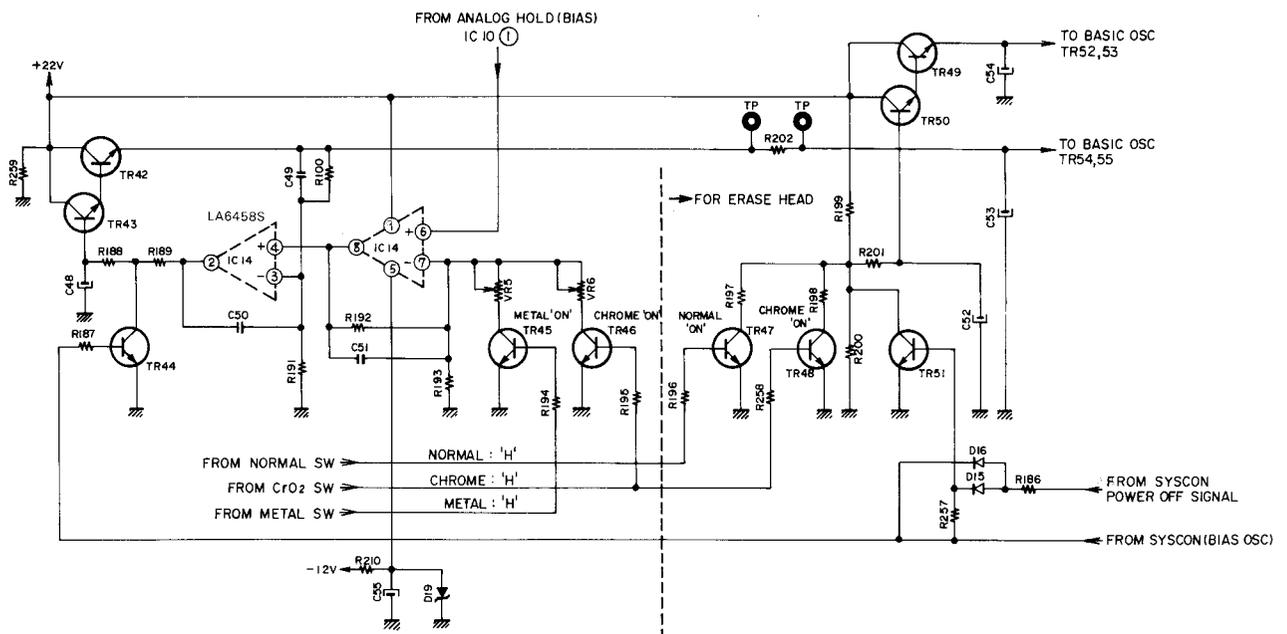


Fig. 1-15

III. AMPLIFIER

1. AMP BLOCK DIAGRAM

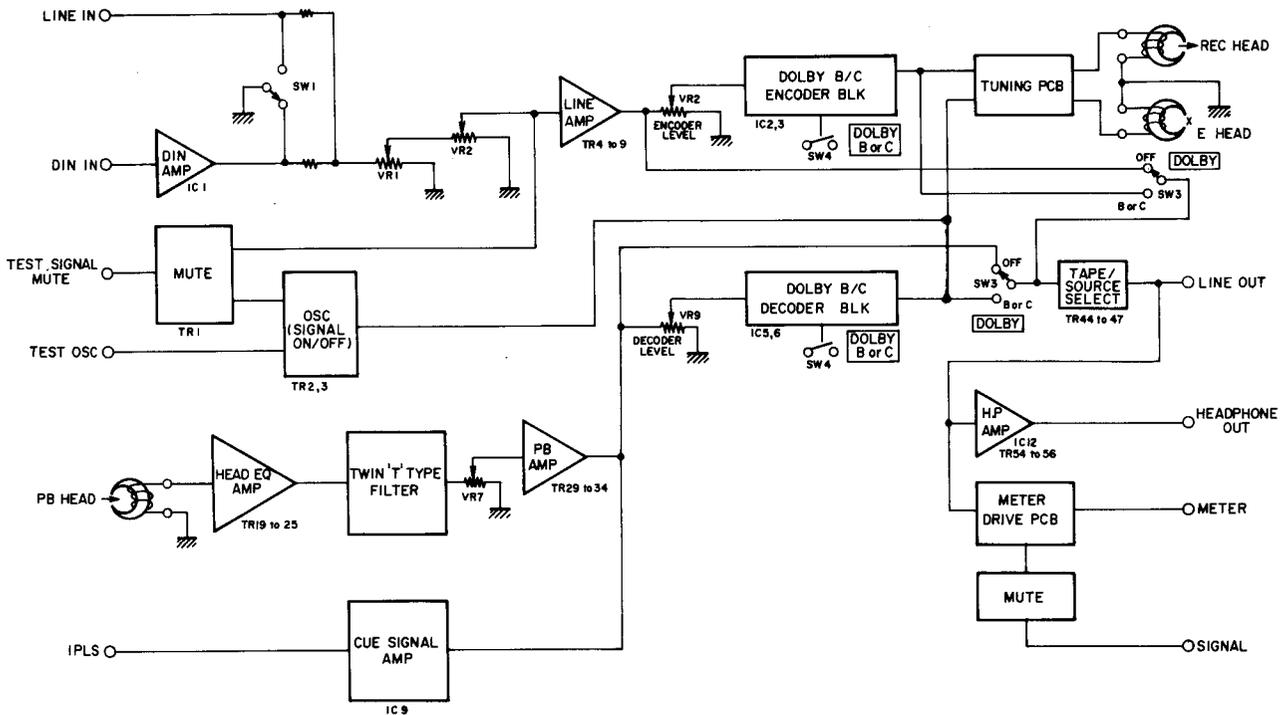


Fig. 1-16

2. PB HEAD EQ AMP (Fig. 1-17)

The PB signal from the PB head is amplified by AMP 1 (differential amp) and then make negative feed back through R103, R104, R106 and R95.

The amplified signal is subjected to DC balancing with VR4 (100B) of AMP 1. The DC balance of the entire AMP 1 is once again set up by VR6 on the "source" side of TR25.

Subsequently, the signal is routed to VR7 via a filter (R110, R111, R112, C52, C53, and C54). (With CrO₂ or METAL, TR27 is activated and the PB high-range EQ curve is changed to a 70 msec time constant with C55, R113 and R114.)

The signal is then adjusted by VR7 (PB LEVEL) before being sent to LINE OUT via AMP 2 (with Dolby IC or Dolby OFF). R134 and R126 of AMP2 provide NF.

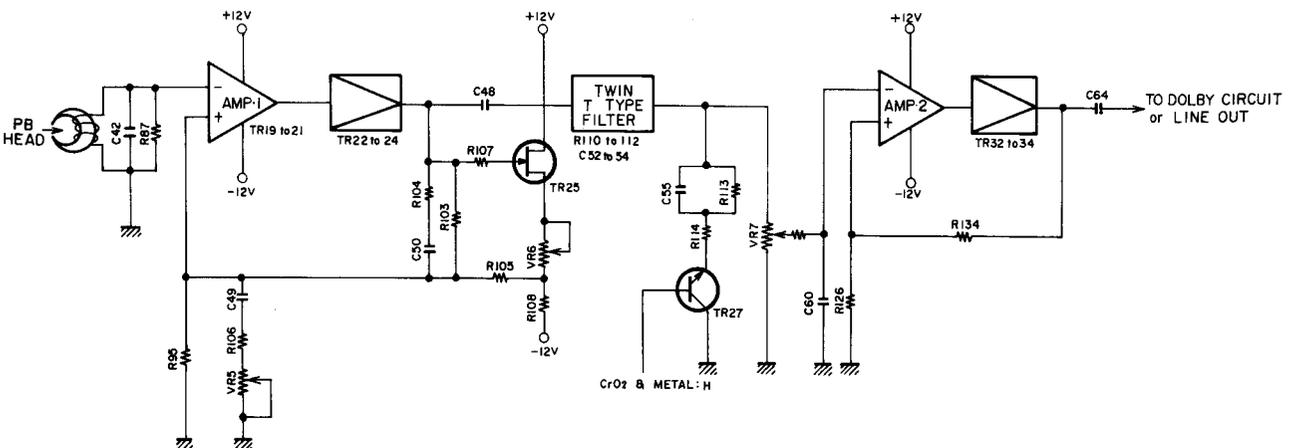
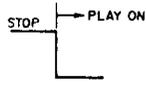


Fig. 1-17

3. TAPE/SOURCE MONITOR SWITCHING AND MUTE CIRCUITS (Refer to Fig. 1-18)

PB MUTE terminal :

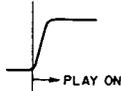
L' (PLAY only), H' (others),



causes TR2 OFF and TR1 OFF.

S (H) terminal "L", Pre amp, TR45 OFF, TR44 ON and PB ON.

PLAY terminal :



Signal (as determined by com-

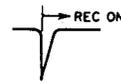
combined time constants of R58 and C13) activates TR15 and ⑥ of IC1 is set to "L".

Because of IC1 [NAND], ④ of IC1 → "H" and ③ of IC1 → "L".

Thus, TR17 OFF, and TR16 ON.

L' to SOURCE IND, and H' to TAPE IND.

Rec/PLAY terminal :



TR13 OFF, TR14 ON, ① of

IC1 → L', ③ of IC1 → H, TAPE IND → L, and SOURCE IND → H'.

Power ON MUTE :

TR3 ON { ⑨ of IC5 → H' and ⑩ → L' and then TAPE MONITOR comes on. MUTE on pre amp side via D33, D2 and D1, resulting in both TAPE and SOURCE being muted.

Power OFF MUTE :

At power OFF time, TR4 is activated by charging current (C2); MUTE on pre amp side via D1 and D2.

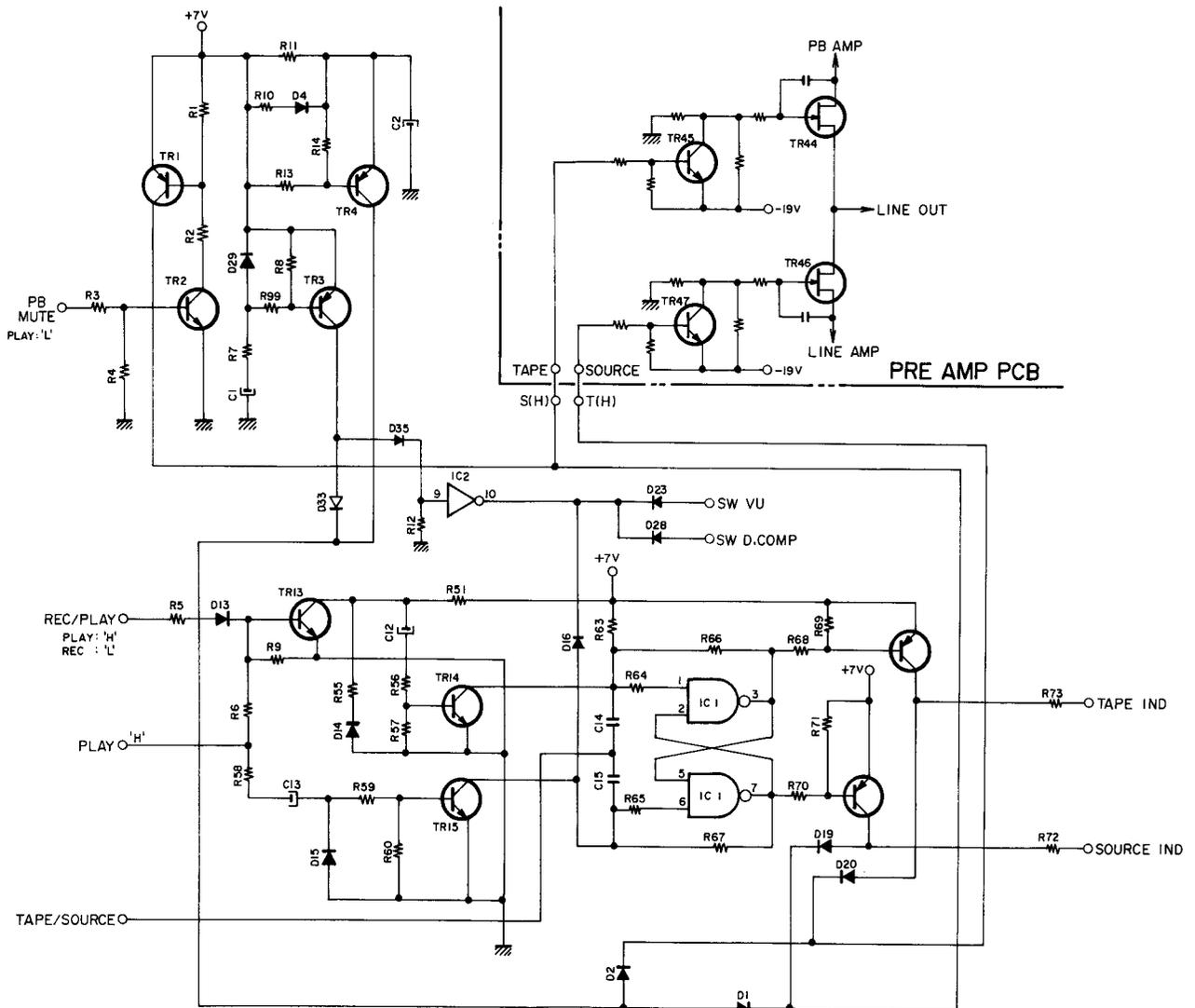


Fig. 1-18

