HITACHI

D-3300M (U,C,W,FS,BS,AU)

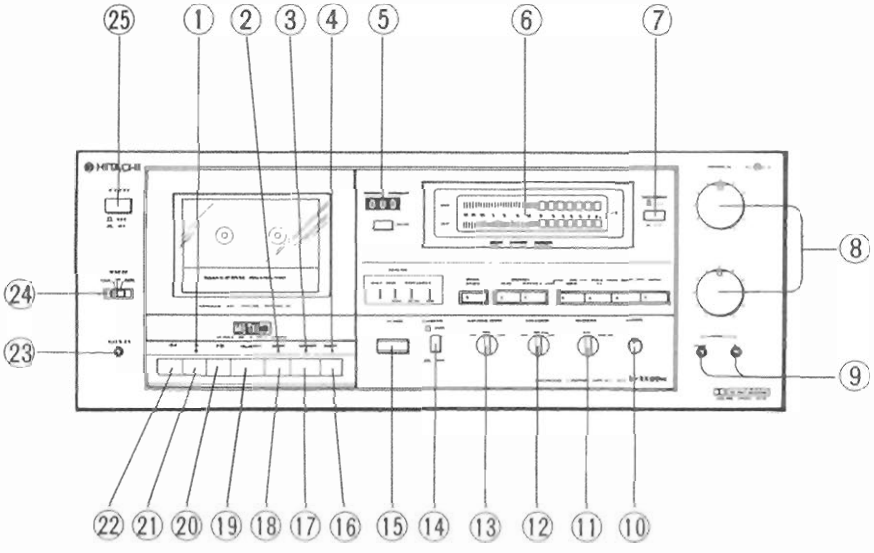
SERVICE MANUAL English No. 1302

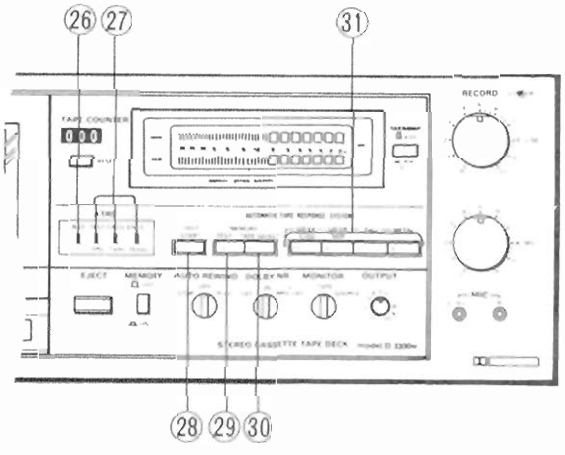
SAFETY PRECAUTION

The following precautions should be observed when servicing.

1. Since many parts in the unit have special safety related characteristics, always use genuine Hitachi's replacement parts. Especially critical parts in the power circuit block should not be replaced with other makes. Critical parts are marked with ⚠ in the schematic diagram and circuit board diagram.
2. Before returning a repaired unit to the customer, the service technician must thoroughly test the unit to ascertain that it is completely safe to operate without danger of electrical shock.

Note:
U ..... USA
C ..... Canada
FS ..... Switzerland and Scandinavia
BS..... Great Britain
AU..... Australia
W ..... General Area





KEY TO ILLUSTRATIONS

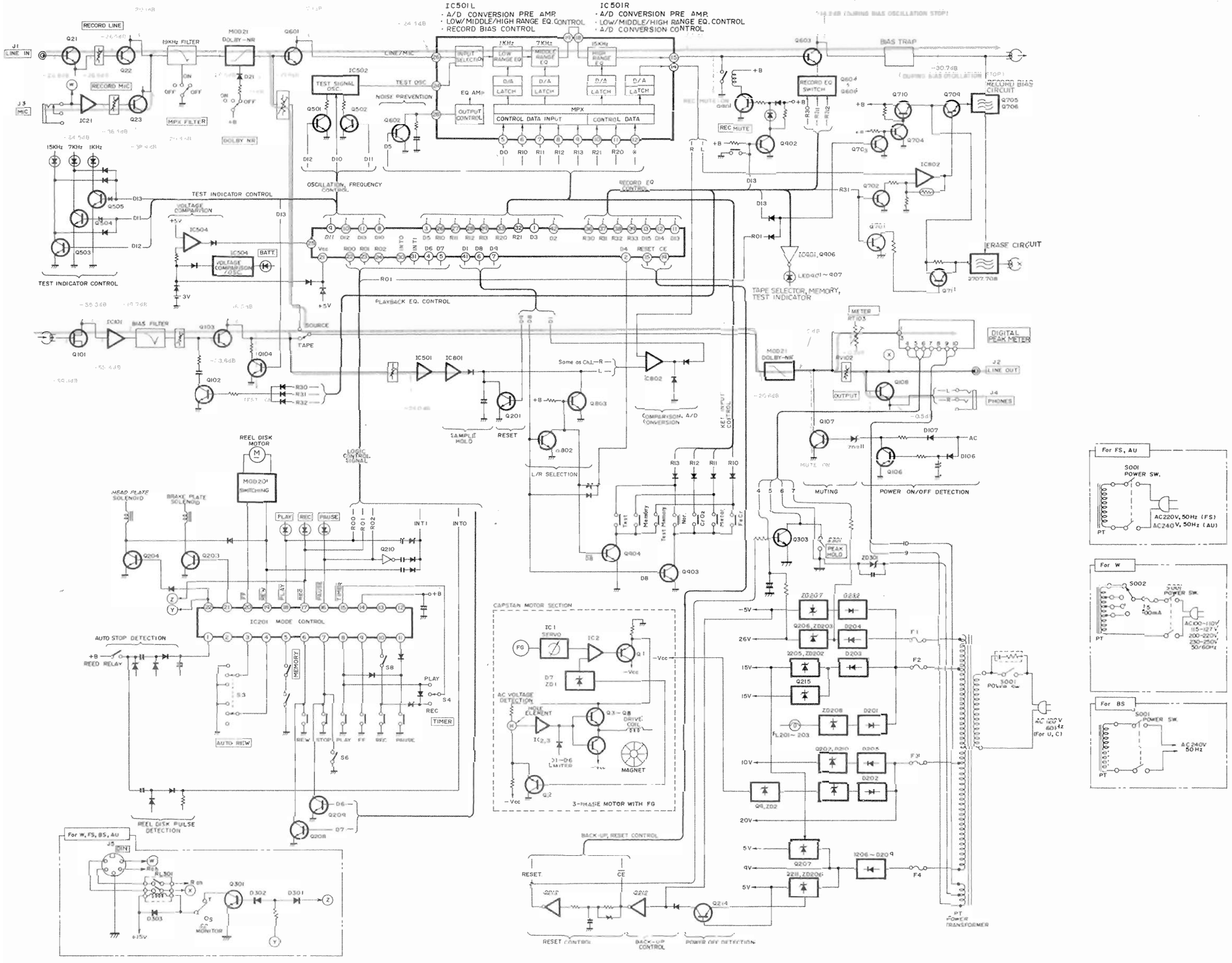
1. PLAYBACK INDICATOR
2. REC INDICATOR
3. PAUSE INDICATOR
4. REC MUTE INDICATOR
5. TAPE COUNTER (TAPE COUNTER)
6. DIGITAL PEAK LEVEL METER
7. PEAK HOLD SWITCH
8. RECORDING LEVEL CONTROLS (RECORD)
9. MIC JACKS (MIC)
10. OUTPUT LEVEL CONTROL (OUTPUT)
11. MONITOR SWITCH (MONITOR)
12. DOLBY NOISE REDUCTION SWITCH/MPX FILTER SWITCH (DOLBY NR)
13. AUTO-REWIND SWITCH
14. MEMORY SWITCH (MEMORY)
15. EJECT BUTTON (EJECT)
16. REC MUTE BUTTON (REC MUTE)
17. PAUSE BUTTON (PAUSE)
18. RECORD BUTTON (REC)
19. STOP BUTTON (STOP)
20. FAST-FORWARD BUTTON (▸▸)
21. PLAYBACK BUTTON (▸)
22. REWIND BUTTON (◂◂)
23. HEADPHONE JACK (PHONES)
24. TIMER SWITCH
25. POWER SWITCH
26. BATTERY INDICATOR (BATT)
27. TEST INDICATORS
28. TEST START BUTTON (TEST START)
29. TEST MEMORY BUTTON
30. TAPE SELECT MEMORY BUTTONS
31. TAPE SELECT BUTTONS

STEREO CASSETTE TAPE DECK

January 1980

CONTENTS

BLOCK DIAGRAM



SPECIFICATIONS

Semi-conductors:	
ICs:	20
Transistors:	71 (U, C) 72 (W, FS, BS, AU)
FETs:	2
Diodes:	85 (U, C) 87 (W, FS, BS, AU)
LEDs:	15
Varistors:	2 (U, C) 3 (W, FS, BS, AU)
Micro computer:	1
Track System:	4 track 2 channel stereo
Tape:	Cassette tape (C-30, 60, 90)
Tape Speed:	4.75 cm/s
Recording System and Bias Frequency:	AC bias, 105 kHz
Erasing System:	AC erase
Erase Ratio:	65 dB or more (at 1 kHz)
Frequency Response:	
Manual:	
UD-ER (NOR)	20 Hz - 20 kHz 30 Hz - 18 kHz (±3 dB) 20 Hz - 20 kHz*
UD-EX (CrO_2)	20 Hz - 22 kHz 30 Hz - 19 kHz (±3 dB) 20 Hz - 20 kHz*
FeCr	20 Hz - 20 kHz 30 Hz - 18 kHz (±3 dB) 20 Hz - 18 kHz*
Metal:	20 Hz - 22 kHz 30 Hz - 19 kHz (±3 dB) 20 Hz - 20 kHz*
ATRS:	The following performance is obtained with almost all tapes on the market at present.
UD-ER (NOR)	30 Hz - 18 kHz (±3 dB) 40 Hz - 15 kHz (±1.5 dB) 20 Hz - 20 kHz*
UD-EX (CrO_2)	30 Hz - 20 kHz (±3 dB) 40 Hz - 15 kHz (±1.5 dB) 20 Hz - 20 kHz*
FeCr	30 Hz - 18 kHz (±3 dB) 40 Hz - 15 kHz (±1.5 dB) 20 Hz - 20 kHz*
Metal:	30 Hz - 20 kHz (±3 dB) 40 Hz - 15 kHz (±1.5 dB) 20 Hz - 20 kHz*

S/N (Signal to Noise Ratio):	
Dolby NR OFF:	60 dB (Weighted A, Reference 3% THD Metal tape) 60 dB*
Dolby NR ON:	69 dB (Weighted A, Reference 3% THD Metal tape) 69 dB*
Wow and Flutter:	0.023% (WRMS) 0.075%*
Input Sensitivity and Impedance:	
Microphone:	0.5 mV, 300 ohms-5 kohms
Line in:	85 mV, 100 kohms or more
DIN (Record/Playback):	0.5 mV, 4.7 kohms
Output Level:	775 mV
Output Load Impedance:	
Line out:	50 kohms or more
DIN (Record/Playback):	50 kohms or more 470 kohms or more*
Headphone:	8 ohms- 2 kohms
Distortion:	1.0% (1 kHz 0 dB-3 dB)
Crosstalk:	
Between tracks:	60 dB (at 1 kHz)
Between channels:	30 dB (at 1 kHz)
Power Supply:	AC 120V, 60 Hz (U, C) AC 100–110V/115–127V/200–220V/230–250V, 50/60 Hz (W) AC 220V, 50 Hz (FS) AC 240V, 50 Hz (BS, AU)
Power Consumption:	37W
Dimensions:	165(H) x 435(W) x 256(D) mm
Weight:	8.7 kg
Motor:	Uni-Torque motor x 1 DC motor x 1
Heads:	New close gap Metal R & P heads (ferrite) Double-gap Metal erase head (Permalloy)
ATRS specifications:	Microcomputer used: 4-bit 1-chip microcomputer Bias variation steps: 32 Sensitivity & Equalization adjustment steps: 32each (variable by 0.25 dB per step) Batteries used (for memory protection): "IEC SR44" x 2

* According to DIN 45 500

TECHNICAL INFORMATION

1. Operation in various modes

	Mode of deck			Operation details of unit
1	Power OFF			• Only the RAM of the microprocessor is kept live by the battery to hold data.
2	Power ON	Just after power is turned ON		• Back-up mode is released and also the tape selector control data, immediately before power was turned OFF, is fed to latch circuit of IC501. The data output terminal operates as a key input terminal after that and the unit enters the watch-and-wait mode for key operation. • When data is not present in the memory selected, the memory indicator flashes.
3		Operations other than testing	PLAYBACK	• Key input "Watch-and-wait" mode. • Back-up battery voltage compared. Comparison and detection are always done when power is switched ON.
			RECORD	• Record using test memory data or tape select memory data.
4		Set for testing		• Test mode is set when the Test button is pressed and when the mode control IC output (PLAY, REC, PAUSE) of the mechanism is set to "001".
5		During testing		• Testing is performed according to the test items shown in Table 1.
6		Immediately after testing is complete		• Data obtained is fed to latch circuit of IC501 after testing is complete.

2. Back-up mode

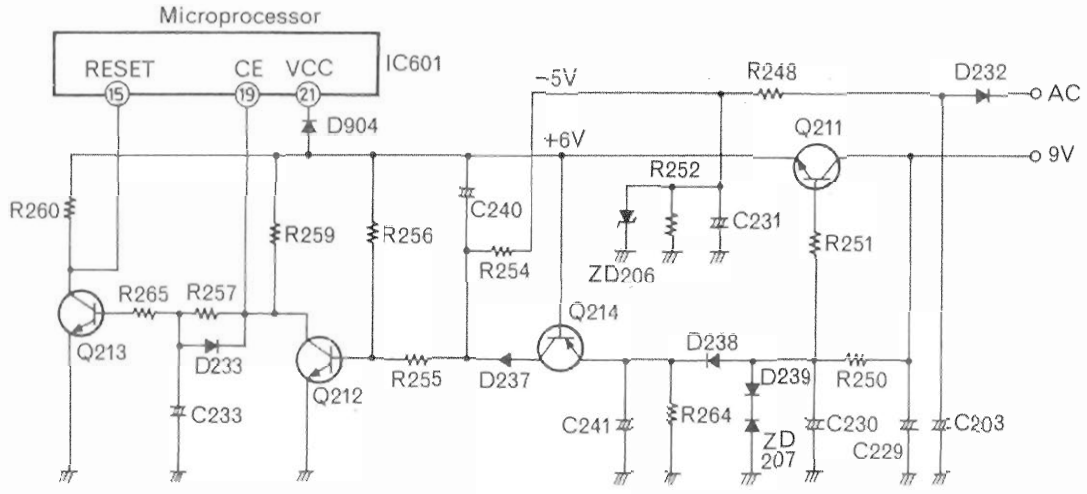


Fig. 1

When the power switch is set to OFF or when the power fails instantaneously, the microprocessor and memory (RAM) which stores the internal test data and memory data are kept active by the external power supply (silver oxide battery) while other circuits stop operation. In this mode, the power consumption is reduced and data is stored in the RAM when the power voltage (Vcc) drops to 2.0V. This function is called the back-up mode.

Operation of the back-up mode

Terminal (19) (CE) of IC601 shown in Fig. 1 is the back-up input terminal; when this terminal is set to Lo level, the unit enters the back-up mode. Terminal (15) (RESET) is the reset input terminal; when the power is turned on, the back-up mode is released, this terminal changes to Lo from Hi and the START program instruction is given.

The time sequence, shown in Fig. 2, is required for setting and releasing the back-up mode.

That is:

To release the back-up mode, CE terminal should be set to Hi more than 100 μs after the power switch was turned ON and the power voltage (Vcc) has been stabilized at +5V. RESET terminal should be set to Lo after a further 100 μs or more has elapsed.

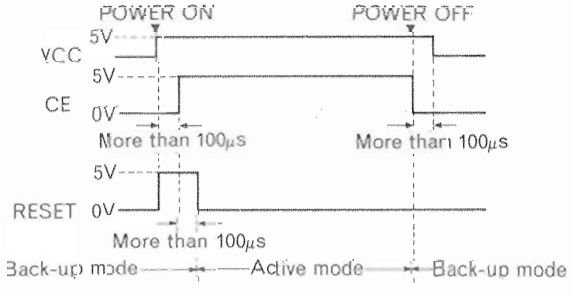


Fig. 2

To enter the back-up mode, CE terminal should be set to Lo immediately after the power switch is turned OFF and the power voltage should be kept at +4.5V for more than 100 μs. The lowest power voltage which can hold data is 2V. The following circuit operation is performed in this time sequence.

When the power switch is set to ON, +9V power supply is applied to the power terminal (21) of the microprocessor via the +6V constant voltage circuit which is composed of Q211, ZD207. Simultaneously, Q212 is activated and Q213 is turned OFF, so CE terminal is set to Lo, and RESET terminal set to Hi.

Approx. 100 ms after the rise of the +6V power supply, negative voltage rectified through D232 rises to the voltage to cancel normal bias of Q212, so Q212 is OFF and CE terminal becomes Hi. After a further 100 ms, the charging voltage of C233 rises to the operation point of Q213, so Q213 is activated and RESET terminal is set to Lo.

When the power switch is set to OFF, the +6V and −5V power supply voltages drop. However, the charge of C241 cannot flow in reverse because of D238, so it is held. Accordingly, when the +6V power supply voltage drops to 5.4V, Q214 is normally biased, so Q214 is activated, the charge of C241 is applied to the base of Q211 via Q214, D237 and R255, Q211 is activated and CE terminal is set to Lo potential. Simultaneously, the charge of C233 is rapidly discharged via D233 and Q212 to make the reset operation certain in case there is an instantaneous power failure and restoration or power switch OFF/ON operation.

3. Back-up voltage detection/alarm circuit

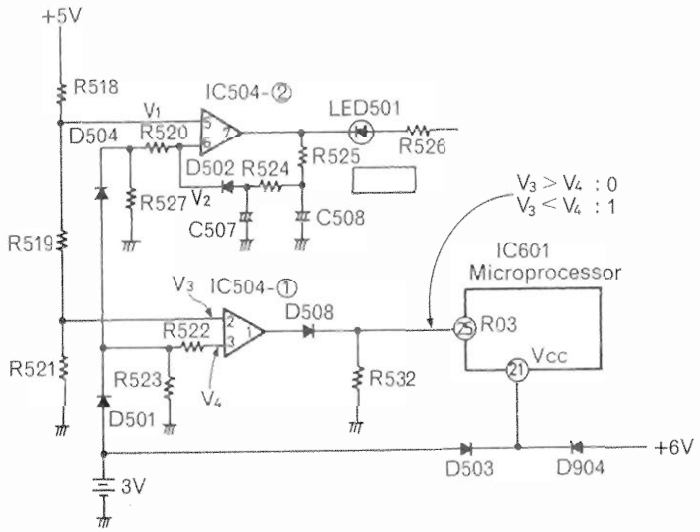


Fig. 3

The back-up voltage detection/alarm circuit shown in Fig. 3 is provided to indicate the residual charge of the back-up battery and presence/absence of memory data.

IC504–② and peripheral circuits compose the blocking oscillation circuit; when the power switch is turned ON, assuming the +5V constant voltage power supply is used as reference voltage (V_1), it compares this voltage with the back-up battery voltage (V_2), and when V_2 drops to T_1 shown in Fig. 4 and V_2 is smaller than V_1, this circuit starts oscillations. Battery alarm indicator LED501 starts flashing due to these oscillations. IC504–① and peripheral circuits detect the back-up battery voltage as well.

When the back-up voltage drops to T_2 (power voltage which can hold data) shown in Fig. 4, immediately after this circuit clears data in the memory (RAM) inside the microprocessor, the power switch is turned ON, making 4 tape select indicators flash to warn that no data is held and it inhibits mechanical operation. Pressing one of the 4 tape select buttons releases the mechanical operation inhibition mode. This operation stops the flashing of the 4 tape select indicators and the indicator corresponding to the pressed tape select button flashes. At the same time, the tape select memory indicator starts flashing to warn of the absence of data in the memories.

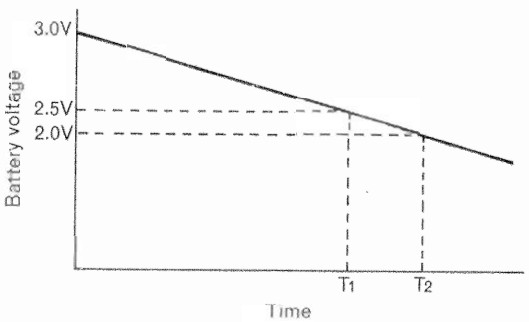


Fig. 4

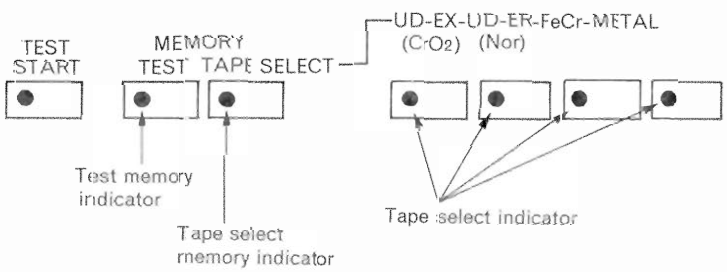


Fig. 5

4. ATRS circuit

(1) Outline of ATRS circuit

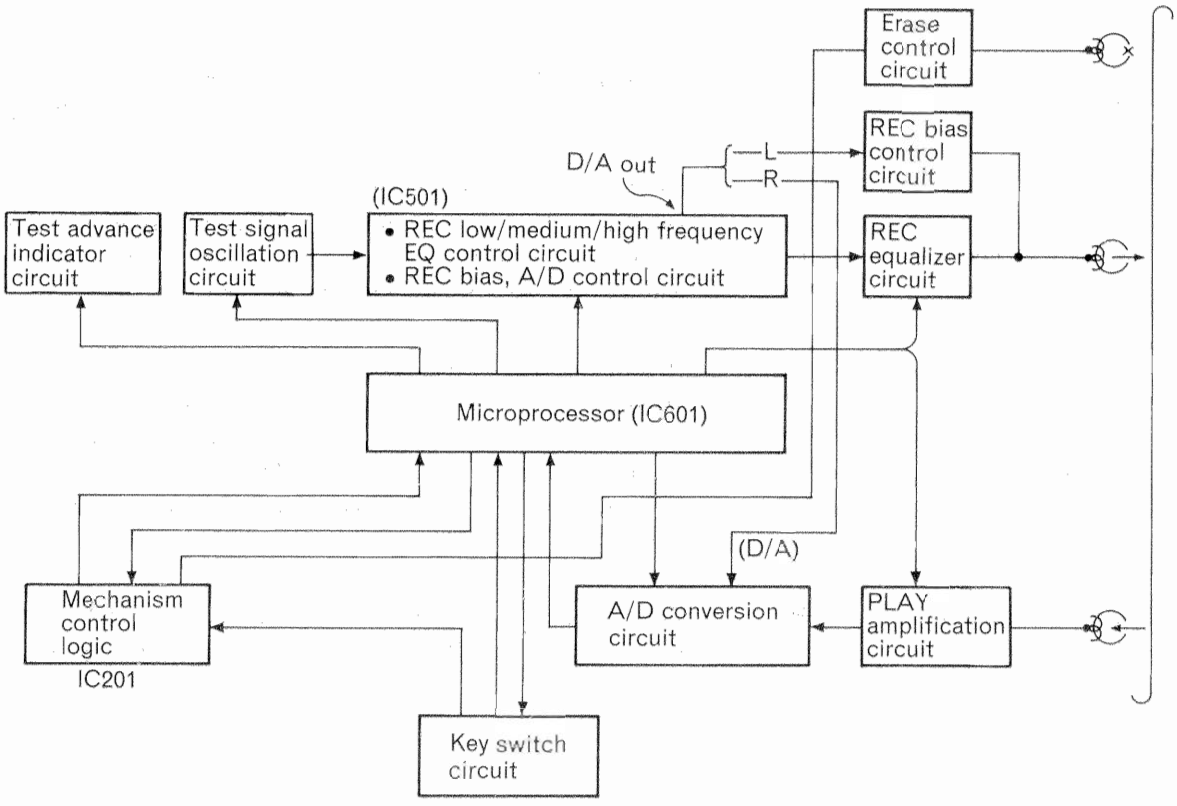


Fig. 6

Fig. 6 is a block diagram of the ATRS circuit.
When testing starts, the microprocessor controls the oscillation operation and the frequency of the test signal oscillation circuit, and in addition supplies control data to the REC low/medium/high frequency EQ circuit and REC bias circuit to the record and play back calibration signals. PLAY gain at that time is detected and calculated to obtain optimum REC equalization & bias control data so that frequency response is flat and distortion in the range of 40 Hz - 15 kHz is minimized for almost any cassette tape at present on sale. At the same time, it controls the test indicator to give information of the test conditions. Furthermore, it detects the number of revolutions of the reel disc and controls the mechanism control logic to rewind the tape to the test start point after the testing is complete. Table 1 shows the test procedure, items and details. Fig. 7 shows L channel REC/PLAY output and testing time during testing with cassette tape HITACHI UD-ER.

Sequence	Test items	Test signal oscillation frequency	Details of test
1.	REC sensitivity	1 kHz	Roughly adjusts REC sensitivity with control data from low/medium/high frequency REC equalizer & REC bias circuit set to "10000".
2.	Error detection	1 kHz	Checks whether or not the test tape is faulty, or the leader tape section is recorded and played back. When the test tape is faulty or leader tape is recorded/played back, it stops testing, instructs the mechanism to stop and starts the test memory indicator flashing.
3.	UP direction REC bias test	1 kHz	Records and plays back 1 kHz reference signal and obtains the bias value when the PLAY level is max. with the REC bias current varied from min. to max. Then, in the same way, obtains the bias value when PLAY level is a max. with REC bias current varied from Max. to Min. Obtains average of these 2 bias values and outputs data with bias value 1 step more than this value.
4.	DOWN direction REC bias test	1 kHz	
5.	Low freq. EQ test	1 kHz	Determines control data so that REC/PLAY output at 7 kHz and 15 kHz is within ±0.5 dB of REC/PLAY output at 1 kHz through testing 3 times.
6.	Medium freq. EQ test	7 kHz	
7.	High freq. EQ test	15 kHz	
8.	Low freq. EQ test	1 kHz	
9.	Medium freq. EQ test	7 kHz	
10.	High freq. EQ test	15 kHz	
11.	Low freq. EQ test	1 kHz	
12.	Medium freq. EQ test	7 kHz	
13.	High freq. EQ test	15 kHz	
14.	Error detection	1 kHz	Checks whether or not the tested section is the leader tape section. When it is the leader tape section, it stops testing, clears obtained data, instructs mechanism to stop operation and starts the test memory indicator flashing.
15.	Rewind up to test start point		REW signal & STOP signal are given to mechanism to rewind the tape to the start point.

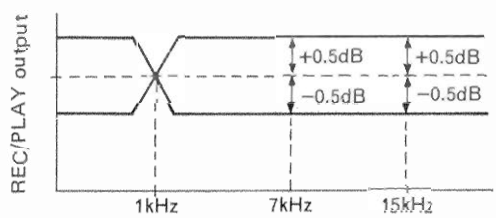


Table 1

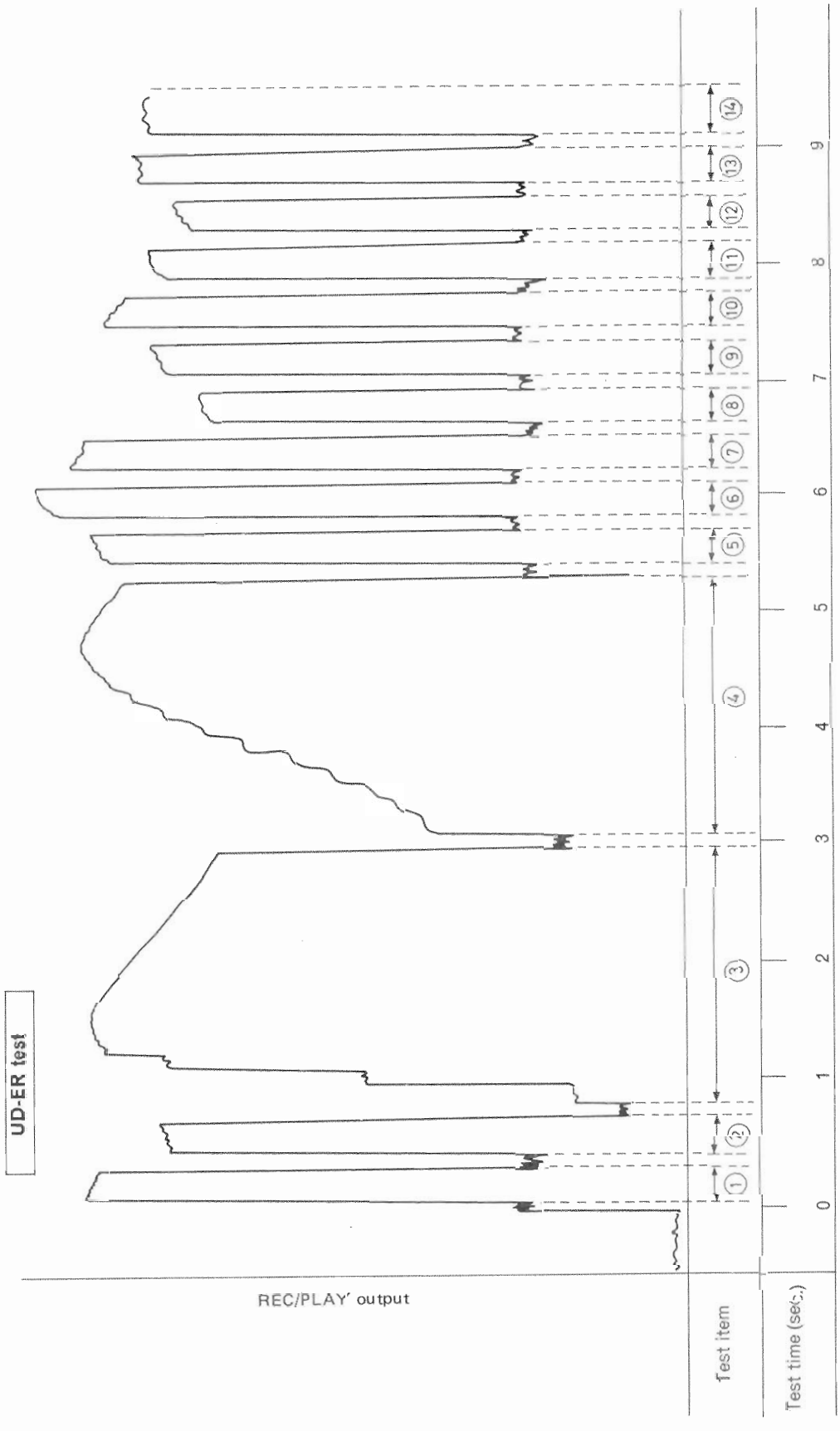

UD-ER test
REC/PLAY' output
Test item
Test time (sec.)
0
1
2
3
4
5
6
7
8
9
①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩
⑪
⑫
⑬
⑭

Fig. 7

(2) Circuit operation

1) Test signal oscillation circuit

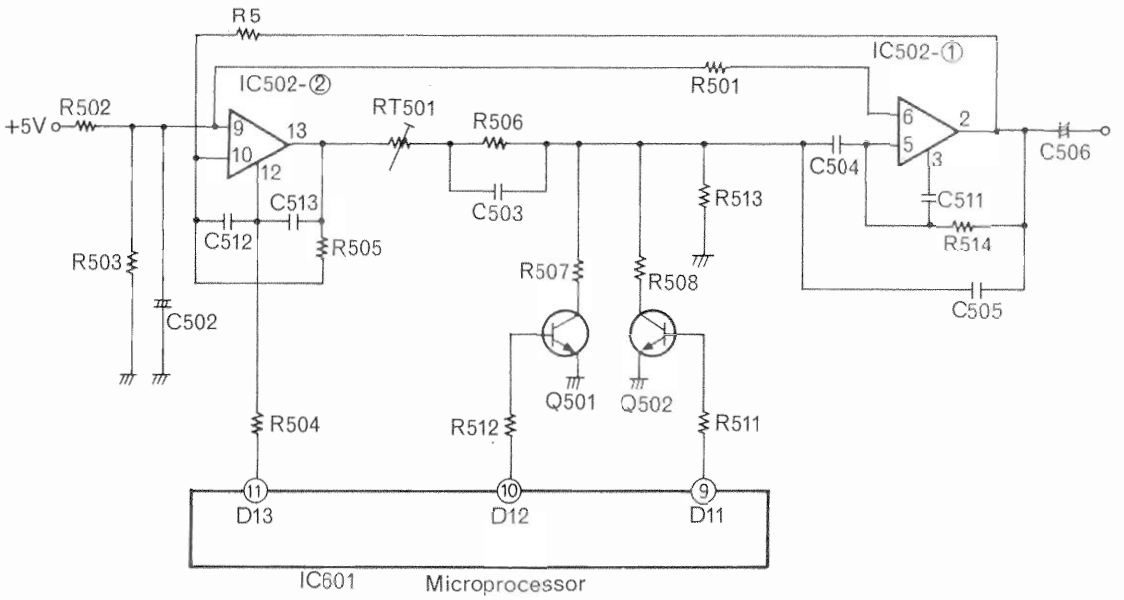


Fig. 8

The test signals required for test items shown in Table 1 are obtained from the test signal oscillation circuits in IC502, shown in Fig. 8.
The principles for the oscillation are the same as D-5500, so they are omitted. Table 2 shows the oscillation operation of the microprocessor and the oscillation select control output data.

Oscillation condition		Oscillation operation control (D13)	Oscillation frequency control	
			D12	D11
Oscillation stops		0	–	–
During oscillation operation	1 kHz	1	0	0
	7 kHz	1	0	1
	15 kHz	1	1	1

Table 2

2) REC equalizer control circuit

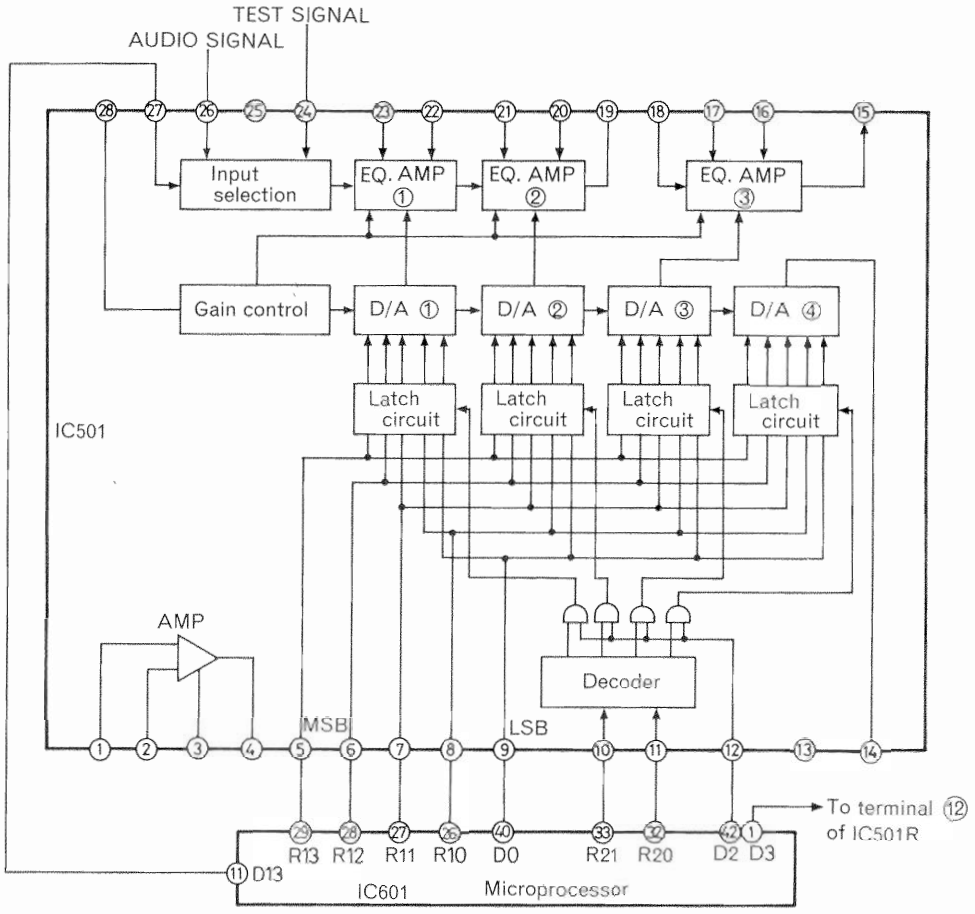


Fig. 9

A single IC is used for the discrete low/medium/high frequency EQ circuits, latch circuits, MPX circuits, the D/A converters for REC bias control/PLAY gain detection and Amp.for playback output amplification used in the D-5500. Fig. 9 shows the internal structure of the IC. The output signal of the test oscillation circuit is input to terminal ㉔ , and audio signal of line-in, mic, etc. to terminal ㉖ .

These input signals select the test signal during testing and the audio signal in other modes, by means of the test mode signal supplied to terminal ㉗ from the microprocessor, to supply them to the next EQ amp.

EQ. AMP ① — EQ. AMP ③ are gain varying amps. which determine the band width of low/medium/high frequency band by capacitors, resistors and coils connected to terminals ⑯ , ⑰ , ⑳ — ㉓ , and control the gain with 5-bit data at terminals ⑤–⑨ .

The 5-bit data input to terminals ⑤—⑨ for gain control is D/A converted through D/A converters (D/A ① — D/A ③) to control the gain. D/A converter D/A ④ is used for the signal which controls the external REC bias circuit and PLAY gain detection circuit; the REC bias circuit is controlled by IC501L, and the PLAY gain detection circuit by IC501R.

Data applied to the D/A converters for the total of 8 circuits (both L/R channels) requires a total of 40 bits; to minimize the number of input/output terminals, data is given by selecting the circuit by a time sharing system, and when data is not changed it is held by the latch circuit. Selection of the latch circuit to which the 5-bit data is applied is determined by the 2-bit EQ selection signal (terminals ⑩ , ⑪) which selects 1 latch circuit among the 4 in 1 chip, and by 1-bit channel selection signal (terminal ⑫) which selects IC501L or IC501R and concurrently provides data entry timing.

Table 3 shows the latch circuits and selected data corresponding to each of the 4 latch circuits.

Terminal (28) of IC501 shown in Figs. 9 & 10 sets the output level change during single step variation of overall variation amount (32 steps) of the control data. To reduce selection noise generated when data is changed due to changing the tape selector, etc., Q602 is cut off by the selection noise preventive control output (Terminal ③) of the microprocessor to minimize the voltage drop at both ends of R902 and the output level change in a single step until the tape position control data is transferred. After the data transfer is complete, the voltage is gradually increased to the set voltage for a single step variation by means of the charging time constant of C606.

The control data is output from the microprocessor in the cases mentioned below. In other modes, the control data is held by the latch circuit inside IC501. The data output terminals of the microprocessor operates as key input terminals during data holding.

1) Immediately after the power switch is set to ON
2) Immediately after the tape selector is changed
3) During testing
4) Immediately after testing is complete

Fig. 11 shows the data transfer timing chart for the total of 8 circuits of both L & R channels.

Stored memory		Control data			
		Channel selection		Equalization selection	
		D2	D3	R20	R21
L ch (IC501L)	Low freq. EQ AMP	0→1	0	0	0
	Medium freq. EQ AMP	0→1	0	1	0
	High freq. EQ AMP	0→1	0	0	1
	REC bias D/A	0→1	0	1	1
R ch (IC501R)	Low freq. EQ AMP	0	0→1	0	0
	Medium freq. EQ AMP	0	0→1	1	0
	High freq. EQ AMP	0	0→1	0	1
	PLAY gain detection D/A	0	0→1	1	1

Table 3

0→1: When data changes from 0 to 1, data is entered to the memory. When it is "0", data is in the latch mode.

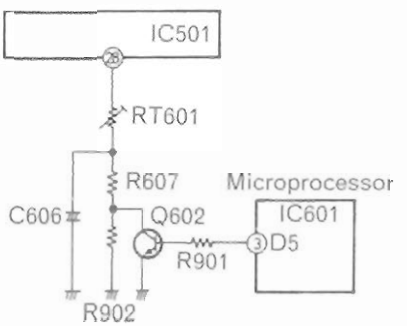


Fig. 10

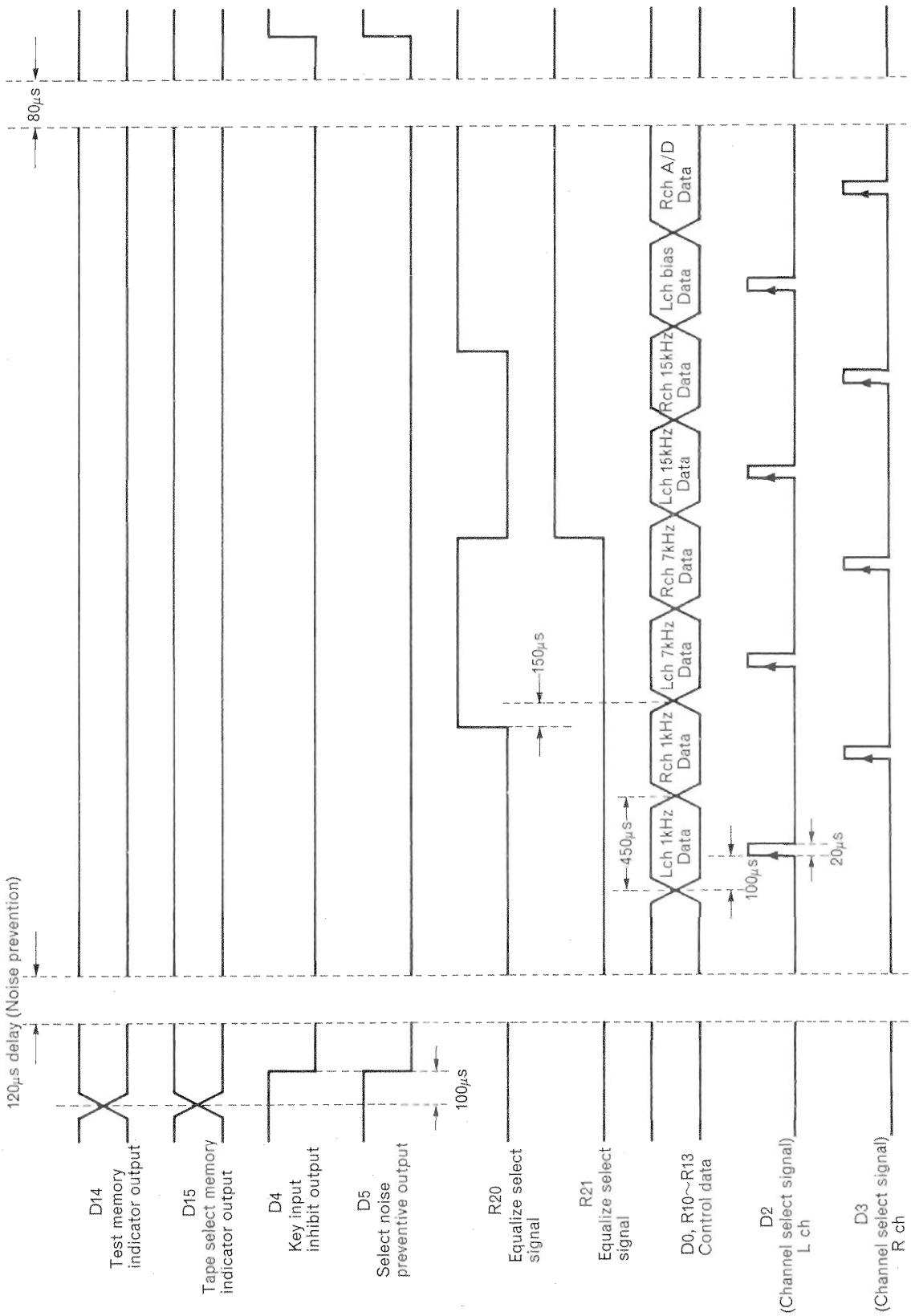

120μs delay (Noise prevention)
80μs
D14
Test memory
indicator output
D15
Tape select memory
indicator output
D4
Key input
inhibit output
D5
Select noise
preventive output
100μs
R20
Equalize select
signal
150μs
R21
Equalize select
signal
450μs
D0, R10~R13
Control data
Lch 1kHz Data
Rch 1kHz Data
Lch 7kHz Data
Rch 7kHz Data
Lch 15kHz Data
Rch 15kHz Data
Lch bias Data
Rch A/D Data
100μs
20μs
D2
(Channel select signal)
L ch
D3
(Channel select signal)
R ch

Fig. 11

3) REC bias/Erase circuit

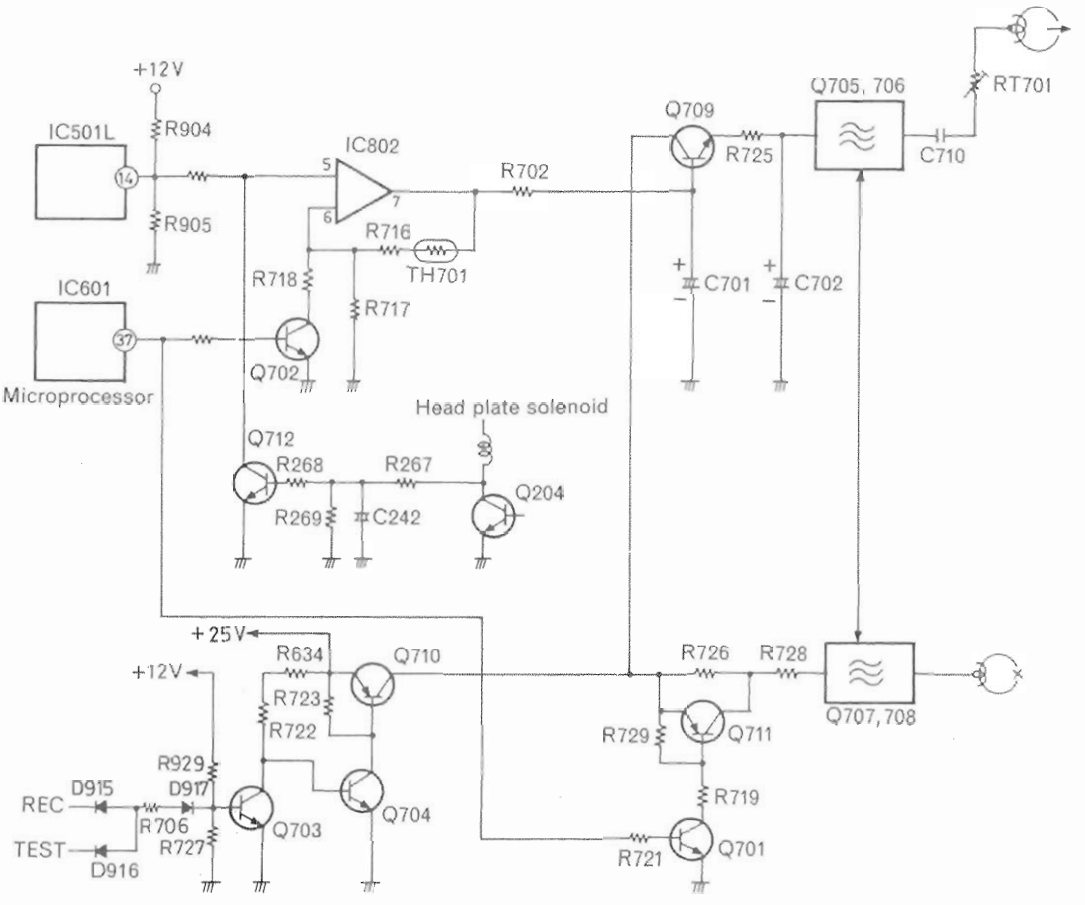


Fig. 12

The erase head is driven by the erase oscillator circuit composed of Q707, Q708; power to the oscillation circuit is increased to obtain the high demagnetization effect needed with Metal Tape. That is, Q711 shown in Fig. 12 is activated to minimize the voltage drop of R726.

Erase oscillator output is supplied to the base of Q705 and Q706 of the REC bias circuit to perform oscillations while synchronizing the erase oscillator circuit and REC bias circuit. As a result beats between the 2 oscillation circuits do not occur and variations in the output of the REC bias circuit do not effect the erase oscillator circuit, so completely stable erasure can be obtained.

The REC bias control D/A output obtained from terminal ⑭ of IC501L as REC bias control is supplied to terminal ⑤ of IC802. Output from terminal ⑦ of IC802 is divided by thermistor (TH701), R716, R717, and the voltage drop across R717 is applied to the negative feedback input terminal of IC802. Thermistor (TH701) increases REC bias as the temperature drops, to compensate for the temperature characteristics of the head. V_B of Q709 is controlled by the output of IC802 to vary the power voltage of the REC bias circuit. Q702 is activated and negative feedback to IC802 is minimized to increase the REC bias during the use of Metal Tape.

The erase circuit continues operation and only the REC bias circuit stops operation to reduce noise during the REC/PAUSE mode. That is, REC bias control signal muting transistor (Q712) is controlled by the collector potential of the head plate control transistor (Q204). In the PAUSE mode, the head plate solenoid does not operate, so Q204 is OFF. Q712 is activated by the collector potential Hi of Q204 at that time, so REC bias control output of IC802 drops to around 0V, Q709 is cut off and only the REC bias circuit stops operation.

4) Key input circuit/key input inhibit circuit

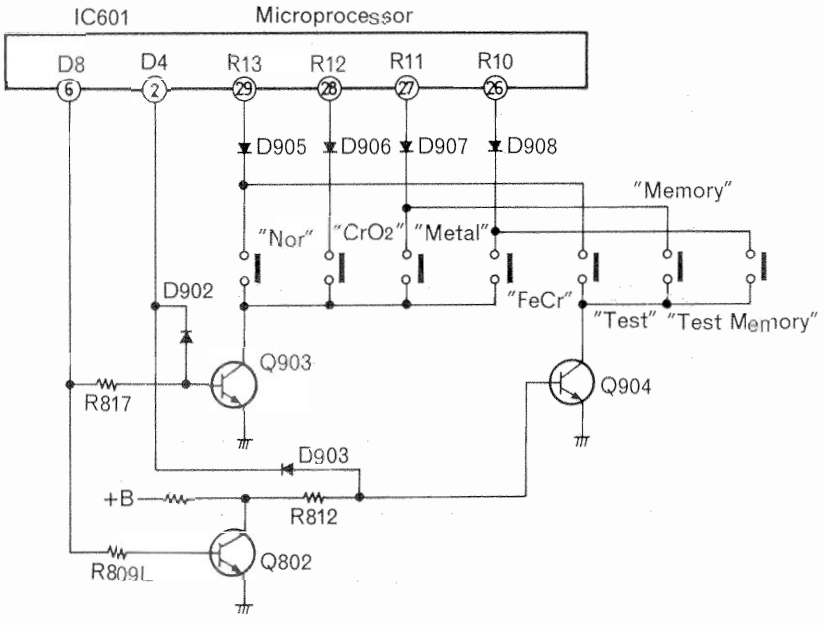


Fig. 13

Key input

The relationship between the 7 types of key input and 4-bit key input from the microprocessor are shown in Table 4. They are obtained by synchronizing the L/R selection signal output from D8 of the microprocessor. That is, L/R selection signal is inverted every 20 ms, and Q903, shown in Fig.13, is activated at Hi potential, so the key input shown inTable 4 (Item (1) — (4)) is detected. At Lo potential, Q904 is activated, so the key input shown in Table 4 (Item (5) — (7)) is detected. Q903 and Q904 operate in opposite ways so key input does not overlap. When there are 2 or more key inputs to the 4-bit input, operations are ignored.

Key input inhibit

Key input terminals R10 — R13 are concurrently used as REC equalizer/bias & A/D control data output terminals; key input during output of data is inhibited. Output terminal ② of IC601 shown in Fig. 13 is set to Lo potential during output of data from terminals R10 - R13, Q903 and Q904 are cut off and key input is inhibited.

Item	Type of key input	L/R output	Key input code			
		D8	R13	R12	R11	R10
1	Normal	1	0	1	1	1
2	CrO_2	1	1	0	1	1
3	Metal	1	1	1	0	1
4	FeCr	1	1	1	1	0
5	Test	0	0	1	1	1
6	Test Memory	0	1	1	0	1
7	Memory	0	1	1	1	0

Table 4

5) Test signal indicator

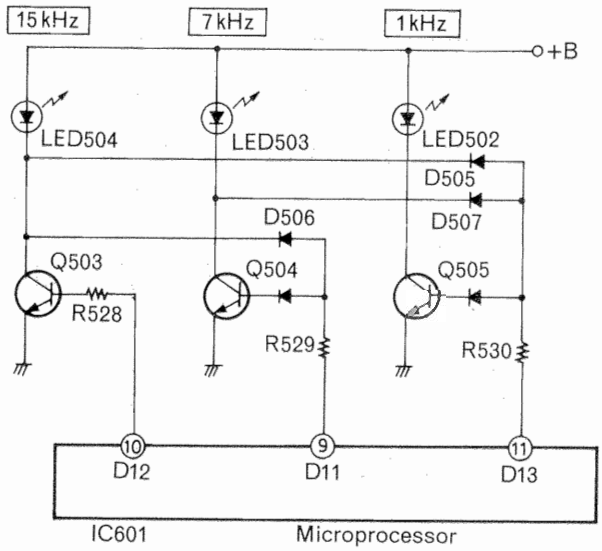


Fig. 14

Progression for testing Items (1) - (13) shown in Table 1 is indicated externally by the test progress indicators (1 kHz, 7 kHz, 15 kHz). A 3-bit signal is obtained from the microprocessor, as shown in Table 5, to control the test progress indicators, shown in Fig. 14.

Test indicators	Control data		
	D13	D11	D12
1 kHz	1	0	0
7 kHz	1	1	0
15 kHz	1	1	1

Table 5

When the control data shown in Table 5 is set to "1", the indicator (LED) corresponding to that output lights up; one indicator on the higher frequency side lights first and the lighting of other indicator on lower frequency side is prevented.

That is, the 1 kHz indicator lights when D13 output signal of the microprocessor is "1" but D13 output data must also be "1" to light the 7 kHz or 15 kHz indicators, so, to prevent the 1 kHz indicator from lighting at that time, "1" output is set to "0" via D507, Q504 to light the 7 kHz indicator and via D505, Q503 to light the 15 kHz indicator to cut Q505 off.

By the same operational principle, the 7 kHz indicator control signal D11 is also prevented from lighting during the lighting of the 15 kHz indicator.

6) Mechanism input/output control during testing

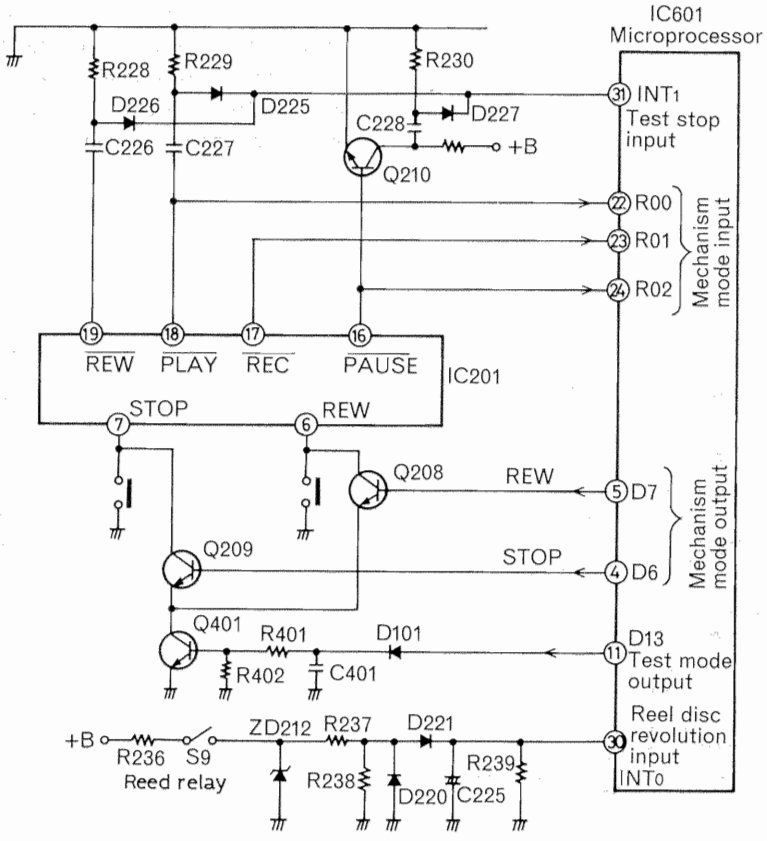


Fig. 15

① Mechanism mode input

The mechanism condition is detected by the mode output ($\overline{\text{PLAY}}$, $\overline{\text{REC}}$, $\overline{\text{PAUSE}}$) of IC201 shown in Fig. 15 when testing starts; when the circuit is in the REC mode or tape running mode, the test mode is set. Mechanism mode input at this time results in the data shown below:

R00 ($\overline{\text{PLAY}}$): 0

R01 ($\overline{\text{REC}}$): 0

R02 ($\overline{\text{PAUSE}}$): 1

② Detection of reel disc rotation pulses

Revolutions of the reel disc generate pulses via the reel disc revolution detection reed relay and the time constant circuit; they are supplied to terminal (30) of the microprocessor to perform interruption processing during testing and are counted.

By this, the tape distance during testing is detected; this is assumed to be the distance to be rewound to the test start position after testing is complete.

③ Test stop input

This input stops the test mode when any of the REW button, STOP button and PAUSE button is pressed during testing.

Mode of Deck	IC201 mode output		
	$\overline{\text{PLAY}}$	$\overline{\text{REW}}$	$\overline{\text{PAUSE}}$*
During testing	0	1	0
When STOP button is pressed during testing	0→1	1	0
When REW button is pressed during testing	0→1	1→0	0
When PAUSE button is pressed during testing	0→1	1	0→1

Table 6

* Values inverted by Q210 before being supplied to the differential circuit are shown.

The REW, STOP, or PAUSE mode output of IC201 shown in Fig. 15 is supplied to the differential circuit composed of R228 — R230, C226 — C228, and the output from each differential circuit is set to AND-logic using D225 – D227, and supplied to INT1 of the microprocessor.

Table 6 shows the output variation when the STOP, REW or PAUSE button is pressed during testing.

A positive pulse is generated at the terminal the output of which changes from 0 to 1 and this pulse stops the test mode.

④ **Mechanism control output**

This applies REW & STOP instruction at the test start position when testing is complete. Q401 is activated only when test mode output terminal ⑪ of the microprocessor is set to Hi potential, that is only during testing, and grounds the emitters of Q208 and Q209 to prevent mis-operation when static electricity pulses enter Q208, Q209.

7) Key indicators

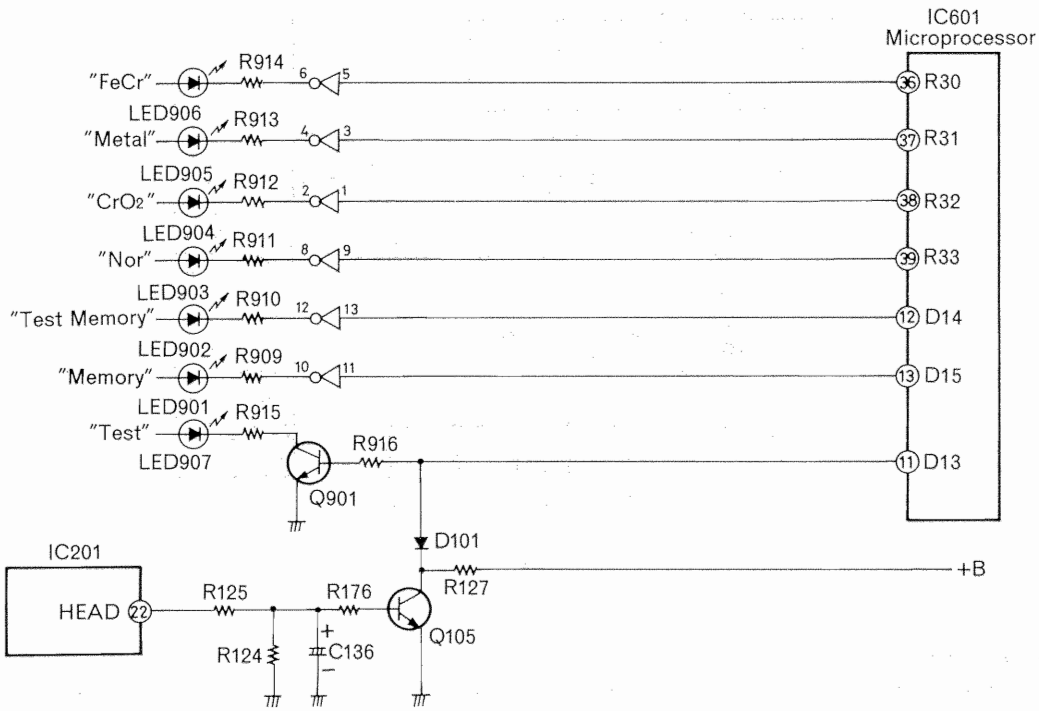


Fig. 16

Fig. 16 shows the key indicator circuit corresponding to key input. FeCr, Metal and CrO_2 outputs of terminals ㊱–㊳ of IC601 become REC, PLAY equalizer and REC bias circuit selection signals as well as indicator control signals.

The TEST mode output signal is set to Hi potential until the head plate solenoid stops after testing starts. Q105 detects head plate solenoid control output and controls test mode output.

8) PLAY gain detection circuit

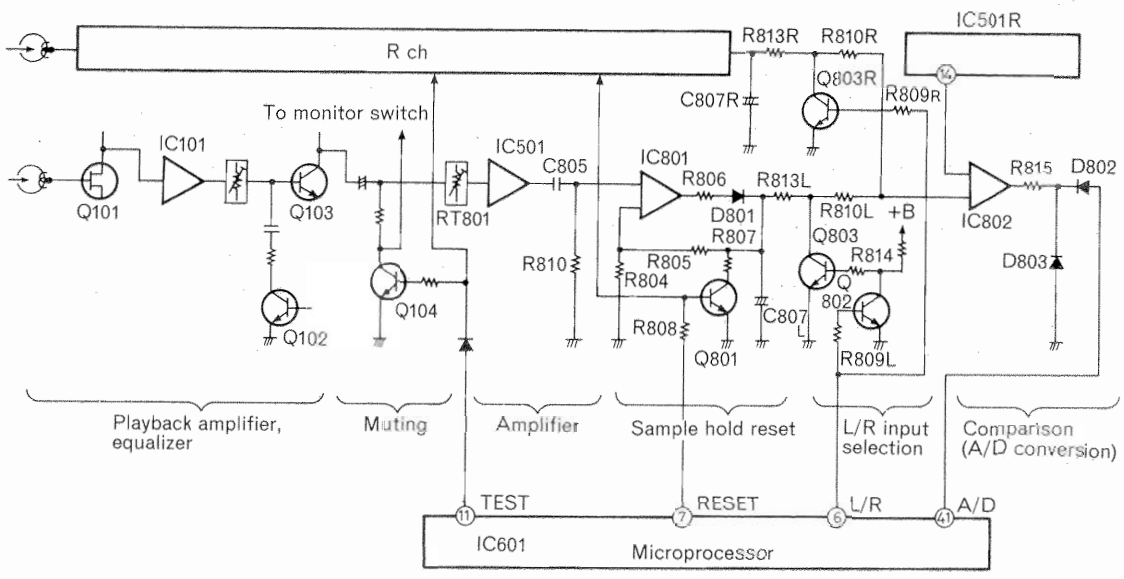


Fig. 17

The play gain detection circuit supplies control data to the REC equalization and REC bias circuits to record the test signal, it detects PLAY output at this time and converts the analog signal to a digital signal. Fig. 17 shows the PLAY gain detection circuit. The circuit is composed of an amplifier circuit, sample hold circuit, L/R input selection circuit and comparison circuit (A/D conversion), and the following control is performed by the microprocessor.

① Muting monitor signal

Activates Q104 during testing and mutes monitor signal.

② Resetting sample hold circuit

Charge held by C807 is discharged by activating Q801 before testing items (1) — (14) shown in Table 1. R806 prevents oscillations during resetting.

③ L/R input selection

Input selection of the comparison circuit is performed to detect PLAY output of both L/R channels by one comparison circuit. That is, the L/R selection signal of IC601 is inverted by inverter Q802, controls the L channel PLAY output muting transistor (Q803L). R channel PLAY output muting transistor (Q803R) is directly controlled by the L/R selection signal.

Accordingly, Q803L and Q803R operate oppositely; when the L/R selection signal is "1", PLAY output of L channel is selected, and when the L/R selection signal is "0", PLAY output of R channel is selected. Assuming the charge held in C807L is V_{1L}, L channel comparison input voltage (V_{OL}) is obtained from the following formula.

$$V_{OL} = V_{1L} \times \frac{R810R}{R813 + R810L + R810R}$$

R channel comparison input voltage is obtained in the same way.

④ D/A control

5-bit data is supplied to IC501R to form a programmable comparison voltage to PLAY input signal of comparator (IC801), and D/A converted DC output is supplied to the comparator through terminal ⑭. The comparison output between PLAY input and D/A is read every time the 5-bit data increases by 1 step. Data is added until both input voltages shown in Fig. 18 coincide, the comparison output is set to Lo potential and then reaches Hi potential again.

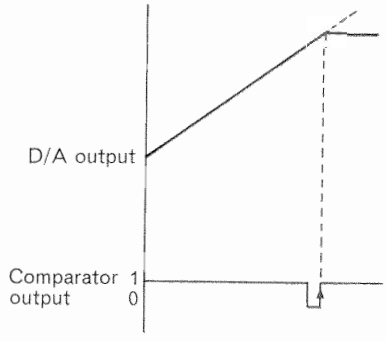


Fig. 18

5. Three-phase uni-torque motor

(1) Outline of construction

Fig. 19 shows the outline of the three-phase uni-torque motor. The rotor is composed of a main body to give it a moment of inertia, and a disc magnet split into 8-poles. The stator is composed of a yoke to complete the magnetic circuit, a stator coil, a base board to hold the stator coil, a support and a top plate. In addition, there is a shaft to connect the rotor and stator with bearing, thrust and speed detection FG gears. The stator coil is composed of ball-shaped coils connected in series, with three-phase-Y-connection. Hall elements are used for position detection of the rotor; 3 Hall elements are incorporated in the coil.

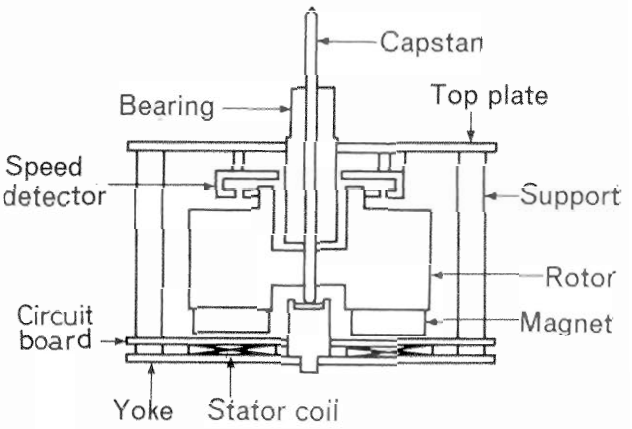


Fig. 19 Construction of three-phase uni-torque motor

(2) Motor drive circuit

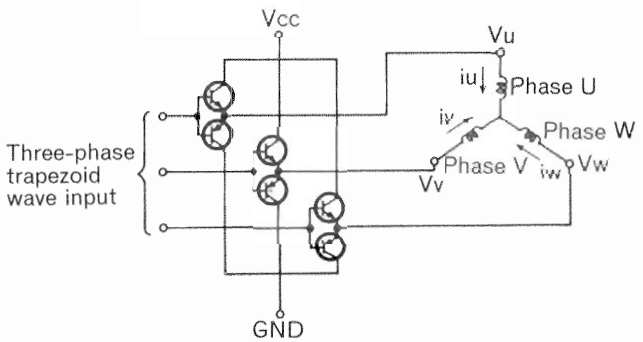


Fig. 20

The drive system connects one end of the three-phase stator coil in star-connection and the other end with three-phase-y-connection which drives using the transistor shown in Fig. 20 to apply power in both directions from a single power supply.

With this system, driving using a sine wave is best from the point of view of torque ripple and external disturbances (noise or vibration) during the selection of current. The unevenness of sensitivity of the rotor position detection Hall element and the effect of offset of the output voltage are large, however, so the sine wave position detection signal obtained from the position detection Hall element is sliced through both upper and lower reference potentials as shown in Figs. 22, 23 to produce a trapezoid wave which is supplied to the stator coil. Since the bias current of the Hall element is supplied by the 2 (upper/lower) reference currents, the position signal proportional to the difference between the two reference potentials can be obtained. As a result, the waveform does not change when the potential difference changes and the amplitude of the trapezoid wave applied to the stator coil changes. Selection of drive current is not done so rapidly, so external disturbances such as noise or vibration, etc. are small. The three-phase drive voltage is sliced at the common reference potential, the amplitude is uniform and it is not affected by unevenness in the sensitivity of the Hall element.

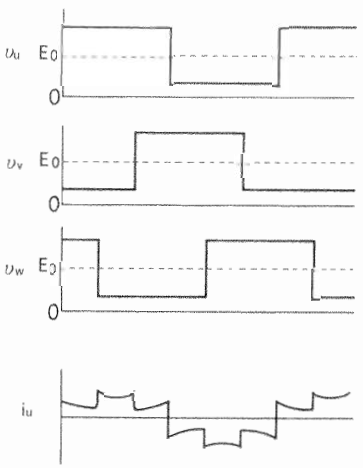


Fig. 21 Three-phase trapezoid wave and current applied to drive circuit

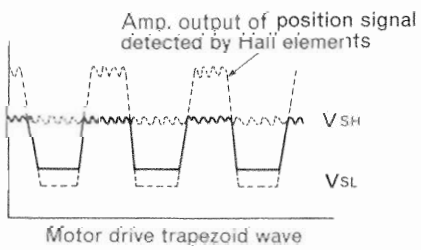


Fig. 22 Actual drive trapezoid wave

The lower reference potential is fixed using zener diode and the upper side reference potential is varied by means of the control signal. The neutral potential of the trapezoid wave varies depending on the variation of the control signal but the potential of the output terminal of the Hall element always changes to this neutral potential, so the selection position of the current does not change.

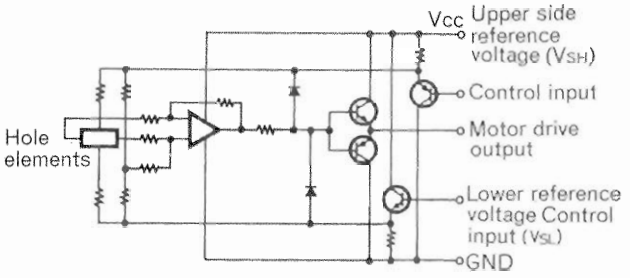


Fig. 23 Position detection of phase and drive circuit

(3) Speed control

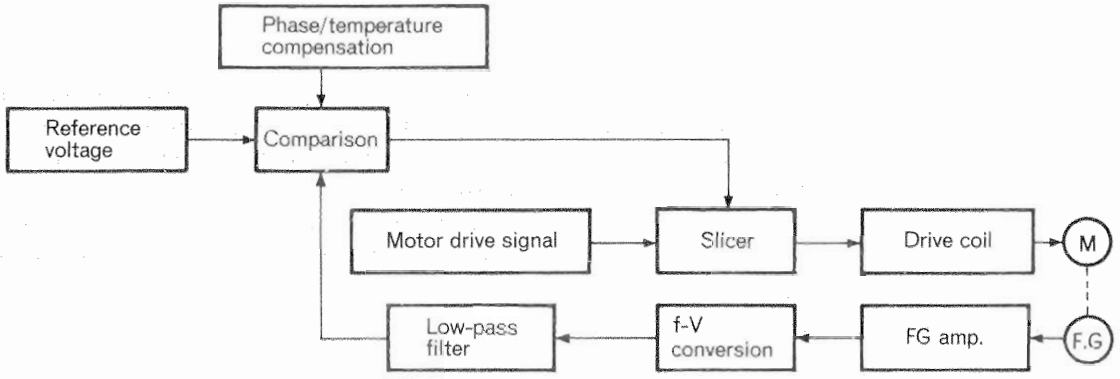


Fig. 24

1) Speed detection

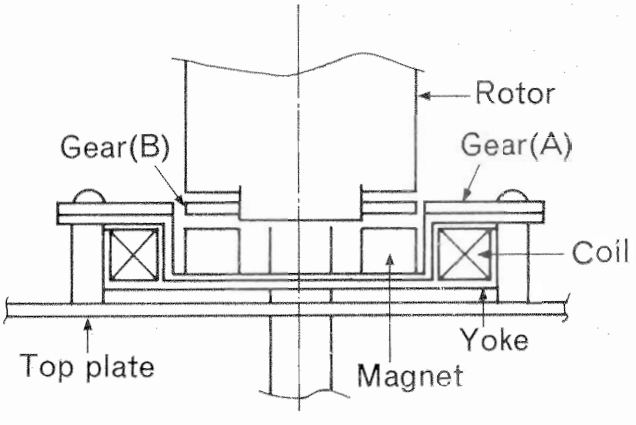


Fig. 25

A detection system which uses the coil to detect variations of magnetic resistance due to combinations of gears is employed for speed detection. That is, magnetic force generated by the magnet shown in Fig. 25 flows to gear (B) fixed to the rotor, gear (A) fixed to top plate and yoke in sequence. Magnetic resistance is generated at that time due to the gap between gear (A) and gear (B).

When gear (A) and gear (B) are positioned at point Ⓐ shown in Fig. 26, the gap is minimized, so magnetic resistance decreases. When they are positioned at Ⓑ, the gap is larger and magnetic resistance increases. Since the number of teeth of the gear is set at 68, magnetism varies 68 time per 1 turn of the rotor; this variation of magnetism is 412 Hz at the rated speed which is detected by the coil.

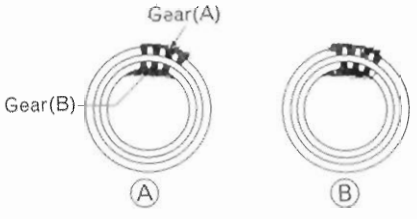


Fig. 26

2) f-v conversion

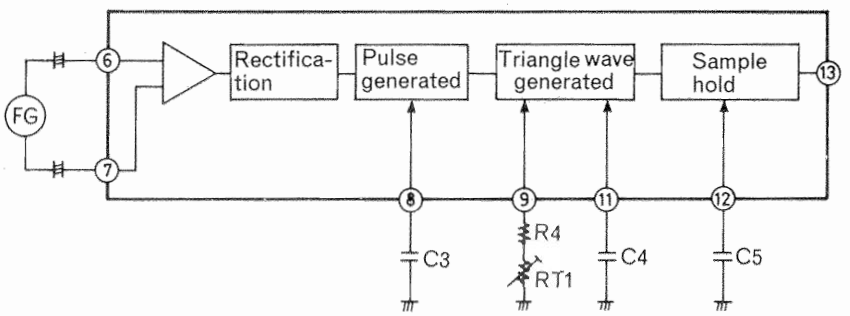


Fig. 27

FG signal detected by the coil is supplied to Servo control IC HA-11713, amplified and rectified, and produces the next triangular wave generating pulse through the pulse generator. Discharge pulse width is determined by the resistor connected to terminal ⑨ and the capacitor connected to terminal ⑪.

After resetting the next triangular wave generation circuit by means of the discharge pulse, the capacitor connected to terminal ⑪ is charged until the next discharge pulse is input. So, charging/discharging is repeated every time a discharge pulse is input and the triangular wave voltage is generated.

This triangular wave voltage is held by the next sample hold circuit and the held voltage is output through terminal ⑬.

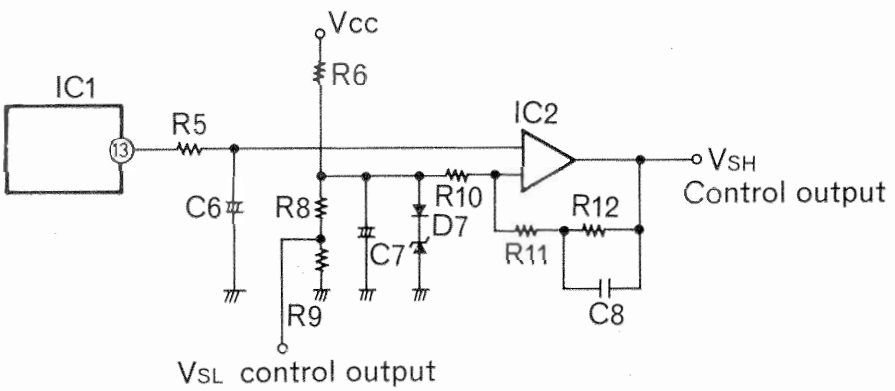


Fig. 28

3) Comparison

The f-v converted signal obtained from terminal ⑬ of IC1 passes through the low-pass filter composed of R5 and C6 shown in Fig. 28, and then compared after phase & temperature compensation by the next differential amp.

The reference voltage is stabilized by Zener diode (ZD1), while diode (D7) is inserted for temperature compensation. For phase compensation, the Amp. (IC2)'s frequency response is determined by R11, R12, C8, the cut-off frequency of the closed loop is set to approx. 25 Hz and loop gain is made larger while minimizing the gain at the speed detection frequency, 412 Hz, using delay compensation.

The upper side sliced section of the position signal, detected and amplified by the Hall elements shown in Fig. 22, is determined by this output (V_{SH}). The reference voltage is further divided by R8 and R9, and voltage drop (V_{SL}) across R9 is assumed to be the sliced section on the lower side.

<table>
<tr><th rowspan="2">Terminal No.</th><th rowspan="2">Terminal symbol</th><th rowspan="2">Terminal name</th><th colspan="2">Terminal functions</th></tr>
<tr><th>Operation other than testing</th><th>During testing</th></tr>
<tr><td>1
42

32
33</td><td>D3
D2

R20
R21</td><td>Channel selection and data writing signal output

Equalizer selection signal output</td><td>Output only when Tape selector changed-over.</td><td>Writing positions to IC501 for 8 types of data (Low/medium/high frequency EQ data x 2 ch, Bias data, A/D data) output from terminals ㉖ – ㉙ , ㊵ are determined by R20, R21, and writing to IC501 of both L/R CHs is selected by D3(R CH), D2(L CH). Writing is performed when D3 or D2 changes from 0 to 1.
<table>
<tr><th colspan="2" rowspan="2">Type of output data</th><th colspan="4">Control data</th></tr>
<tr><th colspan="2">Channel select data</th><th colspan="2">Equalizer select data</th></tr>
<tr><th></th><th></th><th>D2</th><th>D3</th><th>R20</th><th>R21</th></tr>
<tr><td rowspan="4">L CH</td><td>Low freq. EQ</td><td>0→1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Medium freq. EQ</td><td>0→1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>High freq. EQ</td><td>0→1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Bias</td><td>0→1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td rowspan="4">R CH</td><td>Low freq. EQ</td><td>0</td><td>0→1</td><td>0</td><td>0</td></tr>
<tr><td>Medium freq. EQ</td><td>0</td><td>0→1</td><td>1</td><td>0</td></tr>
<tr><td>High freq. EQ</td><td>0</td><td>0→1</td><td>0</td><td>1</td></tr>
<tr><td>A/D</td><td>0</td><td>0→1</td><td>1</td><td>1</td></tr>
</table>
0→1 : Writing is performed at the point where 0 changes to 1.</td></tr>
<tr><td>2</td><td>D4</td><td>Key input inhibition output</td><td></td><td>Inhibits change of Test, Memory, Tape selector, etc. during Test operation (0: INHIBIT)</td></tr>
<tr><td>3</td><td>D5</td><td>Data change noise preventive output</td><td>Prevents noise generated in latch of IC501 when data is changed during testing or when tape selector is changed.
(1: Change-over noise prevention)</td><td>Same as on left.</td></tr>
<tr><td>4</td><td>D6</td><td>STOP signal output</td><td></td><td>Outputs STOP signal to Logic IC to inhibit mechanism operation when the tape is rewound, to Test Start position or when power is switched ON with back-up battery voltage less than specified value (R03 is 0 potential). (1: STOP)</td></tr>
</table>

Terminal No.	Terminal symbol	Terminal name	Terminal functions	
			Operation other than testing	During testing
5	D7	REW signal output		Outputs REW signal to Logic IC to rewind tape to Test Start position when EQ, Bias tests complete. (1: REW)
6	D8	L/R select output		Selects input of L CH and R CH during PLAY gain detection. 1: L CH 0: R CH
7	D9	A/D reset output		Resets SAMPLE HOLD of PLAY gain detection circuit before testing low/medium/high frequency EQ and Bias during testing. (1: Reset)
8	D10	Test oscillation control output		Controls operation of test oscillation circuit. (1: Oscillation, 0: Oscillation stop)
9 10	D11 D12	Test oscillation frequency control output		Varies test oscillation frequency according to tested circuit. Oscillation frequency / Control data D11 D12: 1 kHz: 0 0 7 kHz: 1 0 15 kHz: 1 1
11	D13	Test mode output		Outputs test mode signal from test start time until rewind completed. (1: Test mode)
12	D14	Test memory indicator output	Outputs 1 when Test memory button is pressed and Test data corresponding to the type of tape selected at that time is present.	Outputs 1 after test starts.
13	D15	Memory indicator output	Outputs whether the Test data is present or not in the memory of the tape selector when it is pressed. If the data is not present, the indicator flashes.	
14	DNC			
15	RESET	Reset input	Input showing start of program when power (+5V) is applied to microprocessor or back-up of the battery is released. (1→0: Reset operation)	

Terminal No.	Terminal symbol	Terminal name	Terminal functions	
			Operation other than testing	During testing
16	GND			
17 18	OSC 1 OSC 2	Clock oscillation frequency setting input	Clock oscillation frequency built into the microprocessor is determined by resistor (91kΩ) connected between these terminals. Oscillation frequency: 400 kHz	
19	CE	Memory back-up mode input	Input which signals back-up mode, hold memory data or the condition before power is OFF, when the power switch is set to OFF. (0: Back-up mode)	
20	$\overline{\text{TEST}}$		Always connected to Vcc.	
21	Vcc	Power input		
22 23 24	R00 R01 R02	PLAY mode input REC mode input PAUSE mode input	PLAY: R00 = 0 REC: R01 = 0 PAUSE: R02 = 0	TEST can be executed when input is as shown below. R00: 0 R01: 0 } Recording tape running mode R02: 1
25	R03	Memory back-up voltage input	Compares the memory back-up battery voltage with the reference voltage when power is set to ON. Inputs 1 when the battery voltage is higher than the reference voltage and inputs 0 when it is lower.	
26 27 28 29 40	R10 R11 R12 R13 D0	EQ, Bias data output & key input	8 types of test or memory data are output synchronized with select signals from terminals ①, ㊷, ㉜, ㉝ when the power switch is set to ON or the tape selector is changed. After data output is complete, they become key input shown in the table below, synchronized with L/R select signal of terminal ⑥.	8 types of test data are output synchronized with select signals from terminals ①, ㊷, ㉜, ㉝.

(Cont'd.)

			<table><tr><td rowspan="2">Type of key input</td><td>L/R output</td><td colspan="4">Key input code</td></tr><tr><td>Terminal ⑥</td><td>Terminal ㉙</td><td>Terminal ㉘</td><td>Terminal ㉗</td><td>Terminal ㉖</td></tr><tr><td>Nor</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>CrO_2</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>FeCr</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr><tr><td>Metal</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>Test</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>Test memory</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>Memory</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr></table>	
30	INT0	Reel disc pulse input		Revolutions of reel disc are detected and input using a reed relay to detect tape running distance from test start position up to completion of test of EQ and Bias.
31	INT1	Test stop input		Operation input which stops test operation when STOP, PAUSE or REW is operated during test operation.
34 35	R22 R23	Not used		
36 37 38 39	R30 R31 R32 R33	FeCr output Metal output CrO_2 output Nor. output	Output according to type of tape	
41	D1	A/D conversion	0 or 1	Inputs 1 when A/D conversion is complete.

SERVICE POINTS

Cautions on handling

This unit performs back-up using a silver oxide battery to keep RAM of the C-MOS microprocessor live to maintain the test data and the condition just before the power was turned OFF, when the power switch is set to OFF. When the voltage of the back-up battery drops to less than the specified value, the data held in the RAM is lost when the power switch is set to OFF; and when the power switch is set to ON again, the operation of the mechanism is inhibited. The 4 tape indicators flash in this inhibition mode.

Perform the operation shown below when the mechanism operation is inhibited.

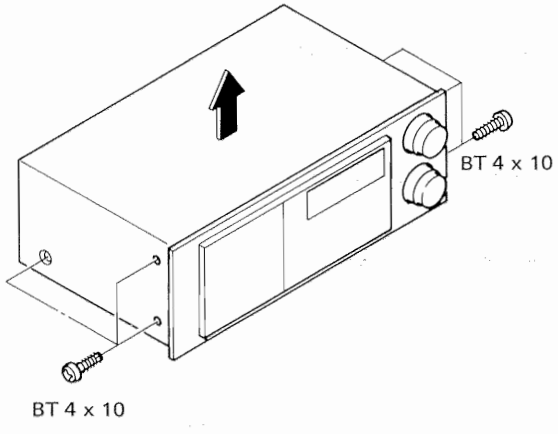
1) Select a tape selector
   This releases the inhibition mode of the mechanism. However, no test data is present in the RAM as it it, so perform testing.
2) Replace battery
   Replace battery with the power switch set to ON. When the battery is replaced with the power switch set to OFF, normal operation may not be possible. In this case, remove the battery with the power switch set to OFF then reinsert the battery after setting the power switch to ON.
3) This unit is adjusted so that $(01011)_2$ data is output to the recording equalizer and bias controller of the ATRS circuit when the "NOR" tape selector button is pressed and optimum recording is possible using HITACHI UD-ER tape.
   This $(01011)_2$ data can easily be set during service checking, so use this data for troubleshooting of overall frequency response, etc. (Refer to Item 8 of adjustment).

Cautions on using MOS IC

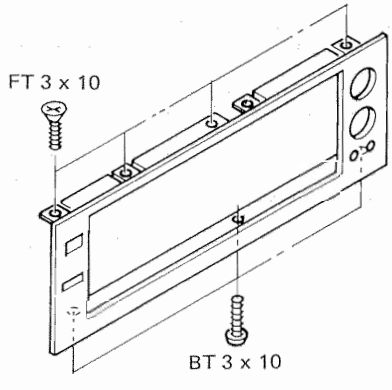
1. The MOS ICs are inserted into a black sponge for shipment. This sponge is conductive and is used to prevent destruction by short-circuiting between leads. Do not remove the IC from this sponge during storage. Avoid removing ICs from the sponge and do not place on plastic which is likely to be charged with static electricity or insert it into styrofoam.
2. Be sure to ground the soldering iron or use a low voltage soldering iron for soldering because a high voltage may be applied due to a leakage from the soldering iron.
3. The worker should be grounded during work because the human body, clothes made from synthetic fibres, nylon gloves. etc., may be charged with several thousand volts of static electricity.
4. Be sure to ground measuring instruments such as oscilloscopes, VTVMs, etc. when they are used.

DISASSEMBLY

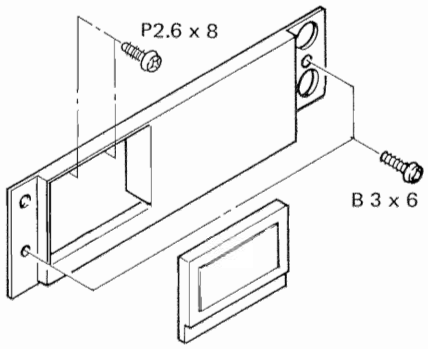
1. Top Cover



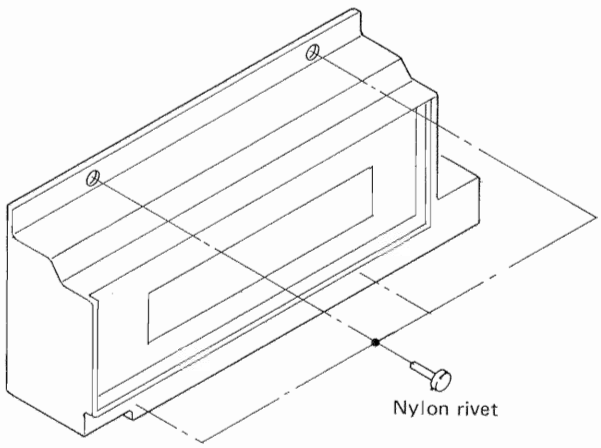
2. Front Panel



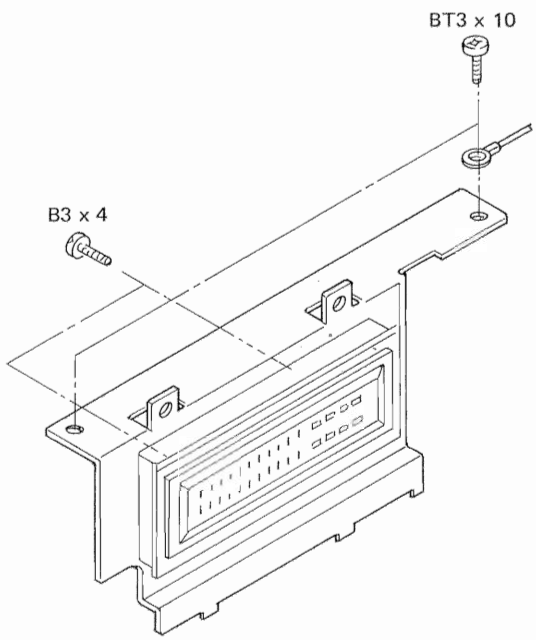
3. Sub Panel



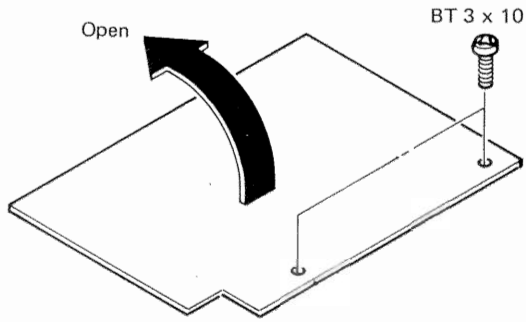
4. Peak Level Meter Cover



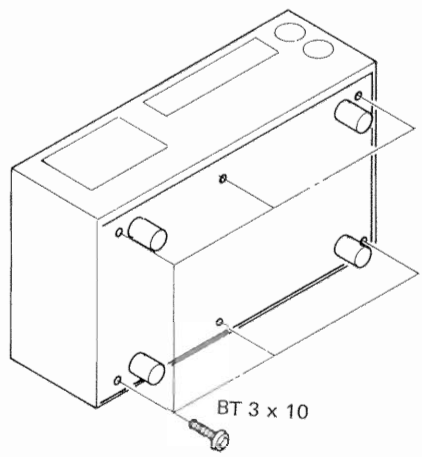
5. Peak Level Meter



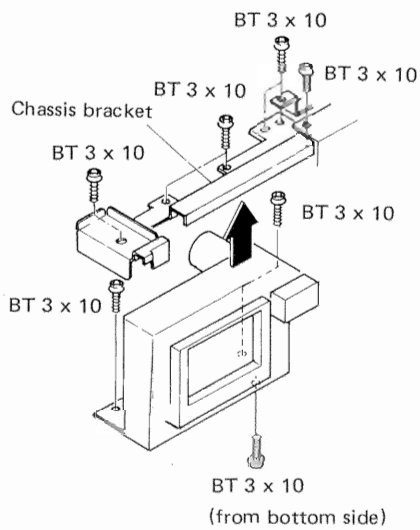
6. ATRS PC Board



7. Bottom Cover

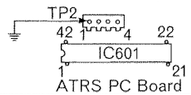
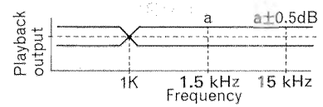


8. Cassette Chassis



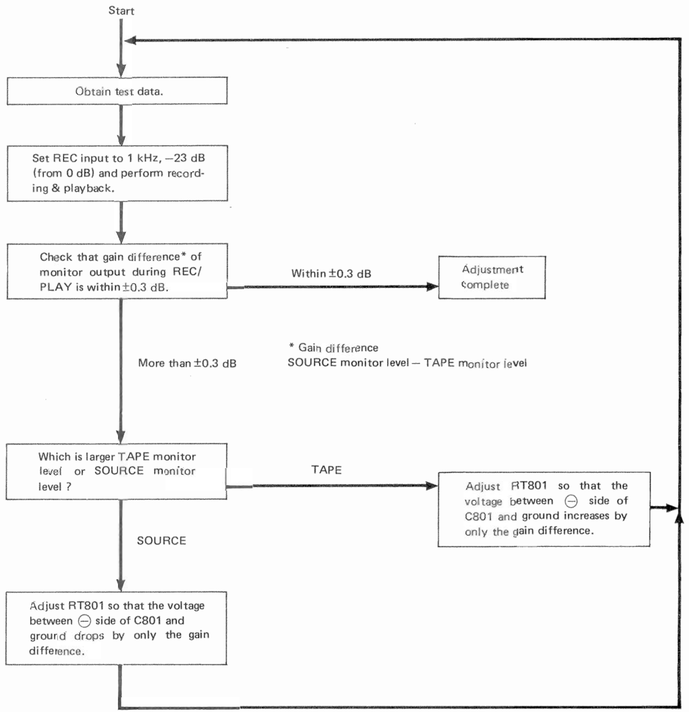
ADJUSTMENT

* According to DIN 45 500.

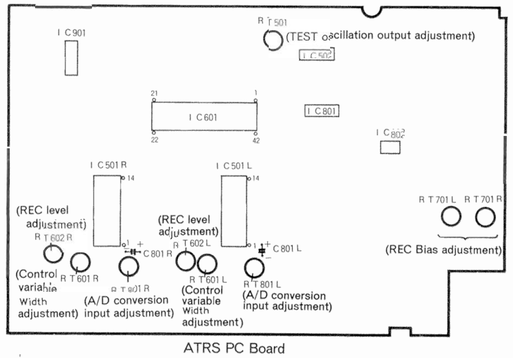
Item	Adjustments		Measuring instrument & connection: Measuring instrument	Input terminal	Output terminal	Tape used/check tape	Condition of set	Adjusted position	Adjusted value	Remarks
1	Cleaning		Cleaning head, capstan, pressure roller, etc.							
2	Setting of switches & knobs		Set switches & knobs as shown in table below when otherwise not specified. RECORD (LINE): MAX. / OUTPUT: MAX. / DOLBY NR: OFF / AUTO REW: OFF / MEMORY: OFF RECORD (MIC): MIN. / MONITOR: TAPE / TAPE SELECT: NOR. / TIMER: OFF							
3	Tape speed		• Frequency counter	——	LINE OUT	MTT-111 (3,000 Hz) (3150 Hz*)	PLAY	RT1	3000 Hz + 20 Hz (3,150 Hz*) −5 Hz	Adjust within 1 minute after heat-running for more than 20 minutes.
4	Record/ playback head	Height	• Head adjusting jig	——	——	——	——	——	——	Refer to "head adjusting jig manual" for details.
		Tilt								
		Azimuth	• V.T.V.M.	——	LINE OUT	MTT-114 (10 kHz)	PLAY	Azimuth adjusting screw	Output max.	When max. output points differ between L & R channels, set to mid-point of both channels.
5	Source monitor level		• Audio oscillator (400 Hz) • V.T.V.M	LINE IN	Terminals ⑫, ⑤ of MOD21L, R	——	PLAY/PAUSE	RT21L, R	0.775V	Adjust Record level (LINE) so that level at terminal ⑫ of MOD21L, R is 0.775V, and then set the monitor switch to source and adjust RT21L, R so that level at terminal ⑤ is 0.775V.
6	Digital peak meter		• Audio oscillator (400 Hz) • V.T.V.M	LINE IN	Terminal ⑤ of MOD21L,R	——	PLAY/PAUSE	RT103L, R	0 dB	Digital peak meter should indicate 0 dB when level at terminal ⑤ of MOD21L, R is 0.775V.
7	PLAY gain		• V.T.V.M	——	Terminal ⑤ of MOD21L,R	MTT-150 (400 Hz, 20 n Maxwell)	PLAY	RT101L,R	0.775V	
8	Setting control data		•This unit can supply "NOR" tape position control data $(01011)_2$ to the equalizer/bias circuits by the following procedure. Adjust as follows so that frequency response is within the specification while this data is applied.  Setting procedures: 1) With the power switch set to OFF connect the terminal ① of TP2 (4P plug) to the chassis or ground pattern of PC Board and turn the power ON from OFF. 2) Remove the connection between TP2 terminal ① and chassis or ground pattern. 3) Check that the "NOR" tape select indicator and Tape select memory indicator are lit. When they are not lit, repeat from Item 1).							
9	Control variable width	IC501L (Bias control output)	• V.T.V.M.	——	Terminal ⑭ of IC501L	——	PLAY	RT601L	0.56V ± 0.02V	
		IC501R (A/D control output)	• V.T.V.M.	——	Terminal ⑭ of IC501R	——	PLAY	RT601R	0.47V ± 0.01V	
10	REC bias adjustment		• Audio oscillator (1.5 kHz/15 kHz) • V.T.V.M	LINE IN	LINE OUT	HITACHI UD-ER(C-90)	REC/PLAY	RT701L,R	Output difference of 1.5 kHz/15 kHz are within ± 0.5 dB.	Record and playback with REC input level set to −23dB from 0dB and adjust REC Bias, REC level so that characteristics shown below are obtained.  a: REC/PLAY output at 1.5 kHz
11	REC level adjustment		• Audio oscillator (1 kHz) • V.T.V.M	LINE IN	LINE OUT	HITACHI UD-ER(C-90)	REC/PLAY	RT602L,R	Adjust the level so that TAPE (Monitor switch) is +2dB with respect to SOURCE.	
12	TEST oscillation output		•Synchroscope	——	Between ⊖ side of C506 & ground	——	REC/PLAY	RT501	Just after waveform during 1 kHz oscillation is clipped.	Adjust while 1 kHz indicator lights during testing. (Adjust during REC Bias test (approx. 5 sec from Test start).)
13	A/D Conversion circuit input adjustment is to adjust input level of A/D conversion circuit so that data obtained from the test coincides with the control data $(01011)_2$.									
	Input of A/D conversion circuit	Rough adjustment	• Audio oscillator (1 kHz) • V.T.V.M	LINE IN	Between ⊖ side of C801L,R & ground	HITACHI UD-ER (C-90)	REC/PLAY	RT801L, R	5mV ± 0.2mV	Set REC input to 1 kHz, −23dB (from 0dB), after REC level is adjusted, and perform rough adjustment
		Precise adjustment								Refer to "A/D conversion circuit input precise adjustment procedure".

A/D CONVERSION CIRCUIT INPUT PRECISE ADJUSTMENT PROCEDURE

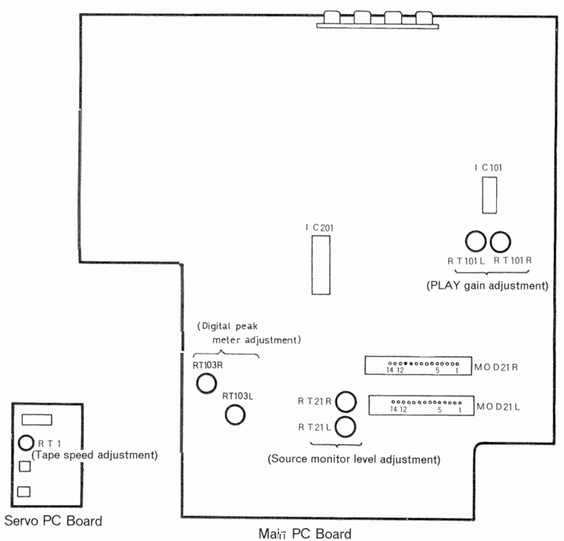
Adjust L CH, R CH respectively by the following procedure.



ADJUSTMENT PARTS LOCATION



ATRS PC Board

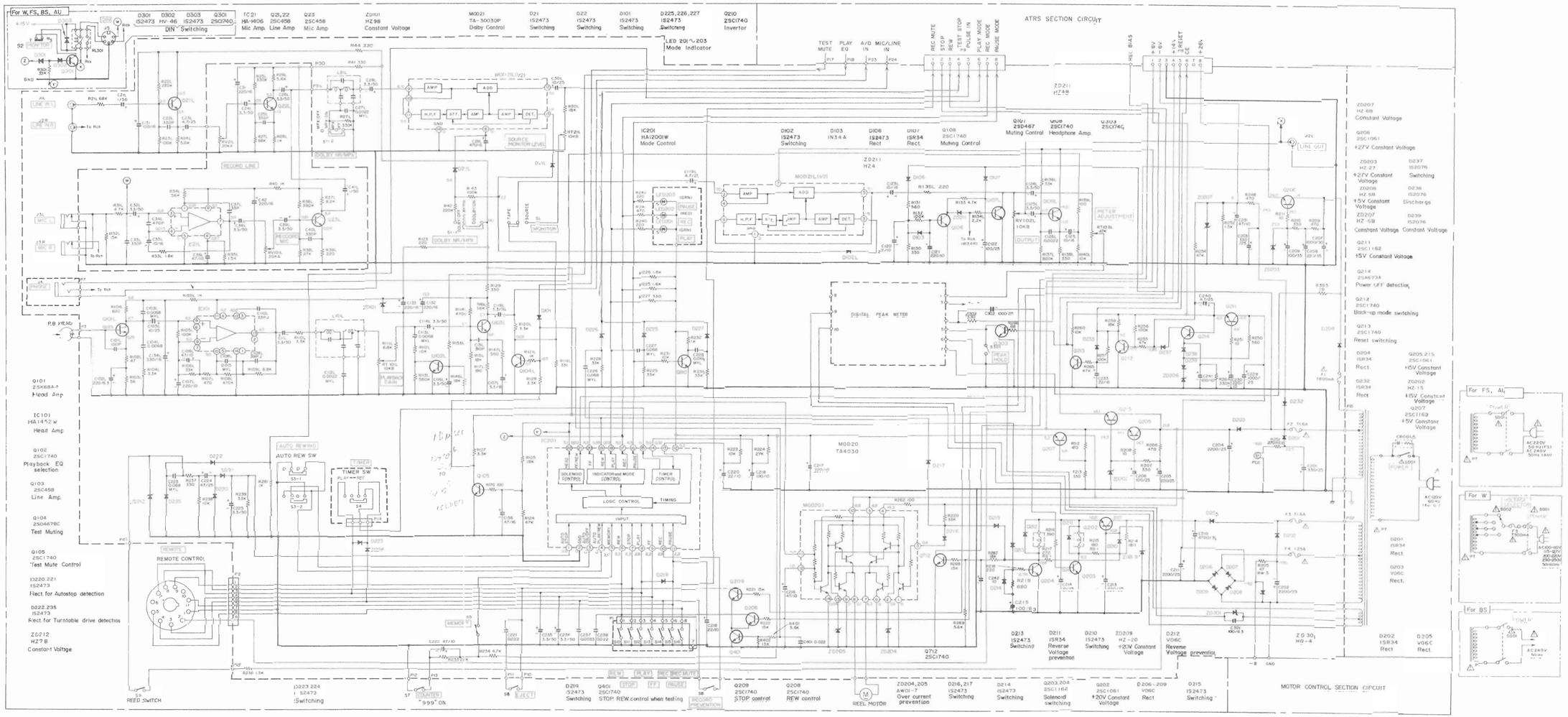


Servo PC Board

Main PC Board

— MEMO —

SCHEMATIC DIAGRAM (Main Section)



Note

1. Voltage measured at base of chassis with minimum volume control and no signal.
2. Nomenclature of Resistors and Capacitors.

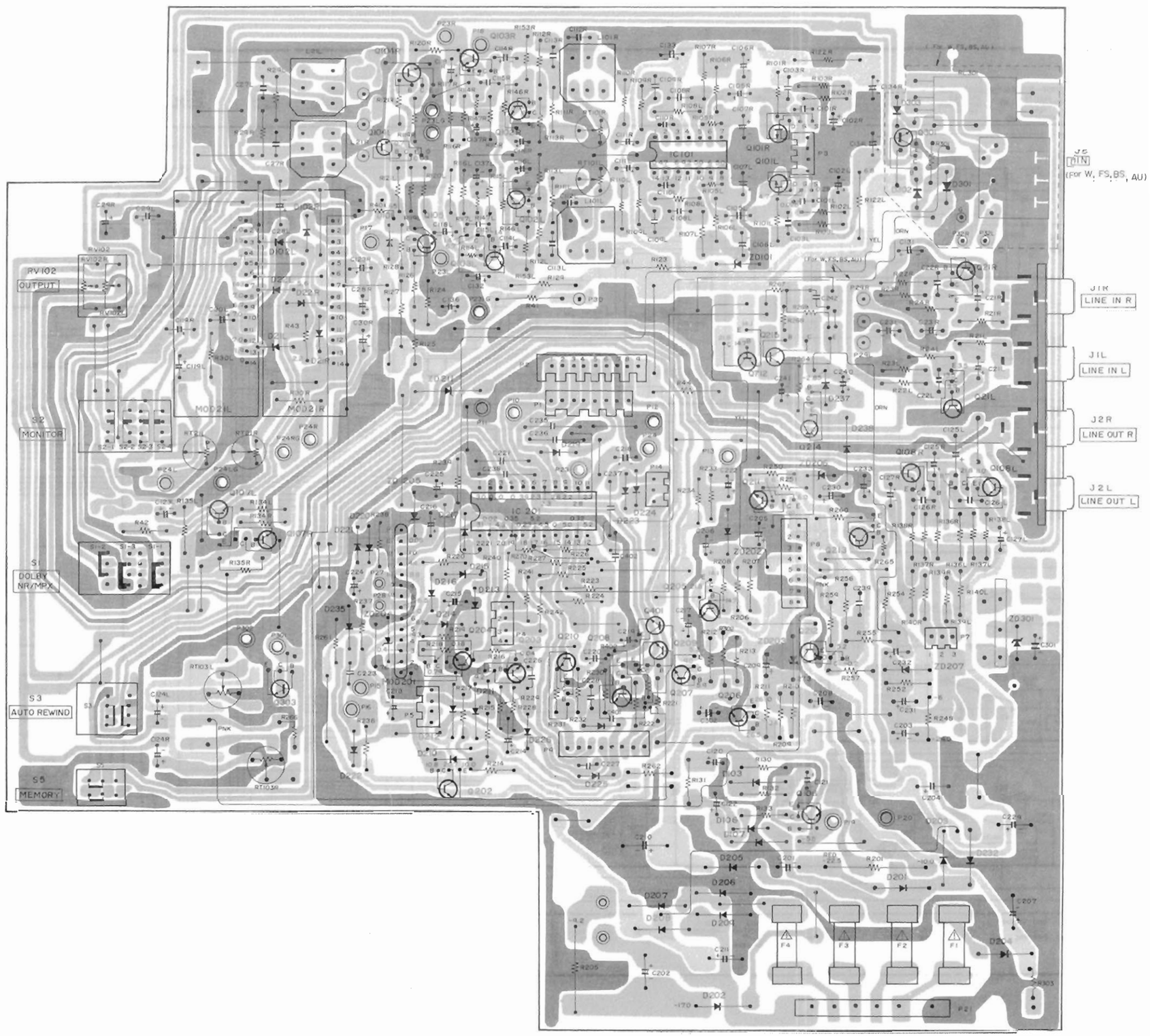
	Circuit No.	
R101 150-RS-1-K-	Value	No indicated Ω (Ohm) M : 1000 kΩ
	Tolerance	No indicated ±5% K : ±10% M : ±20%
	Wattage	No indicated ¼W
	Sort	No indicated Carbon film RC : Composition RW : Wire wound RS : Oxide metal film RN : Fixed metal film

	Circuit No.	
C101 0.001-B	Value	No indicated μF P : PF
	Tolerance	No indicated ±10% J : ± 5% M : ±20% Z : +80%, −20% D : ±0.5pF C : ±0.25pF
	Sort	Ceramic
		Electrolitic
		Mylar
		Polyester
		Styrol
C102 0.1/16-	Voltage	No indicated 50WV

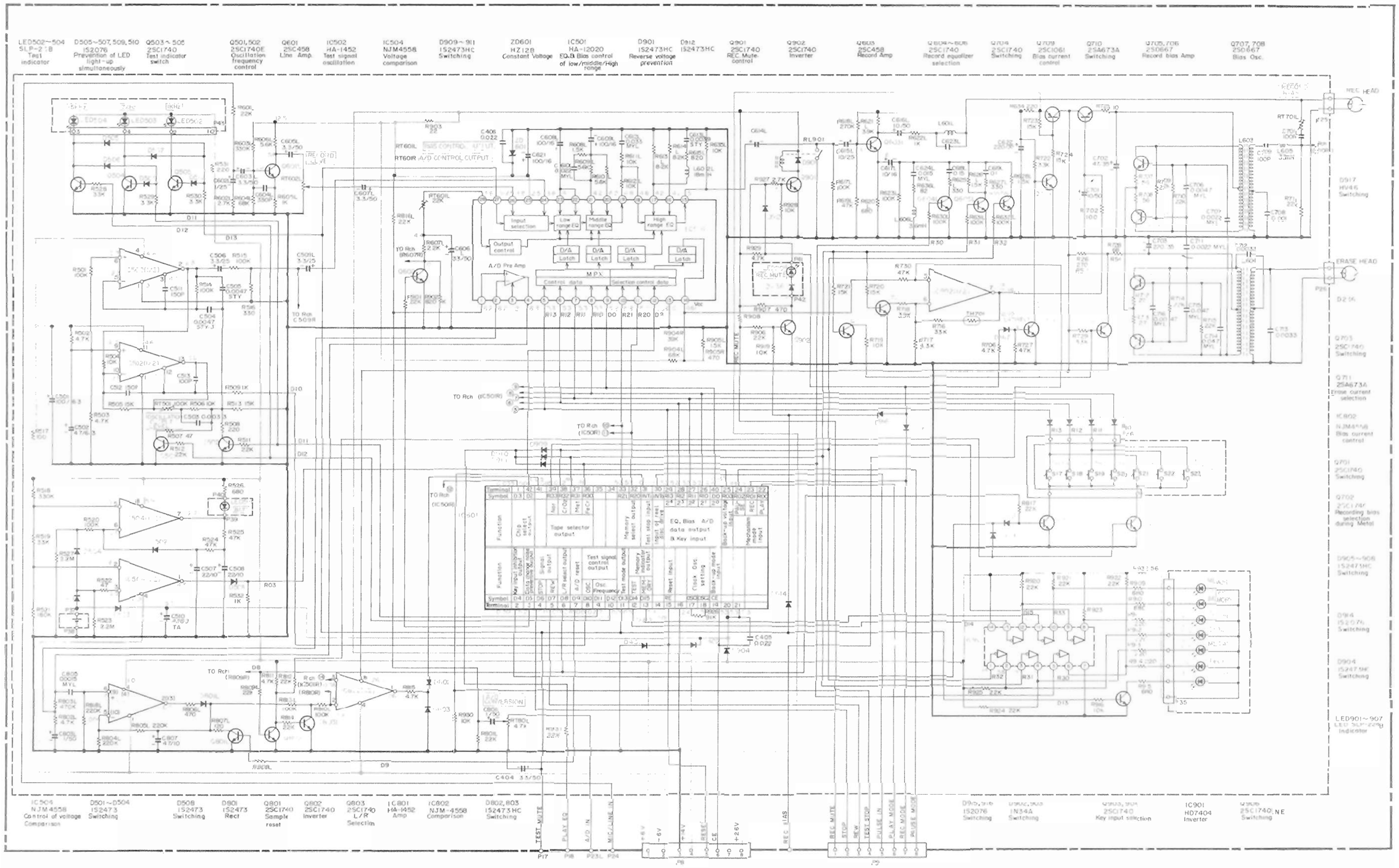
3. Be sure to make your orders of resistors and capacitors with value, voltage, tolerance and sort.
4. When replacing capacitors marked with ⊕, use specified ones stated on parts list since required temperature characteristics.

CIRCUIT BOARD DIAGRAM (Main PC Board)

: +B : Ground : Signal, others

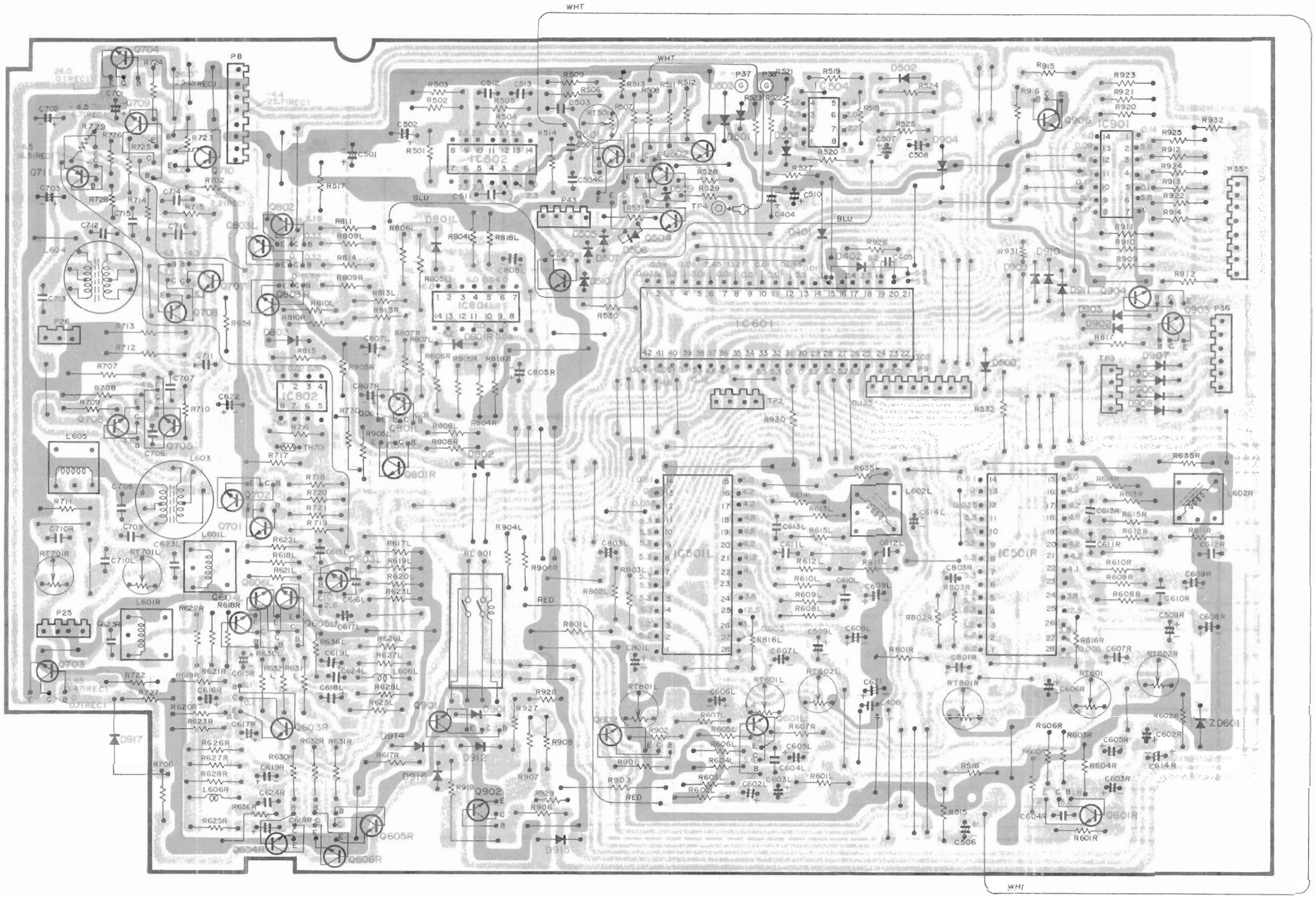


SCHEMATIC DIAGRAM (ATRS Section)

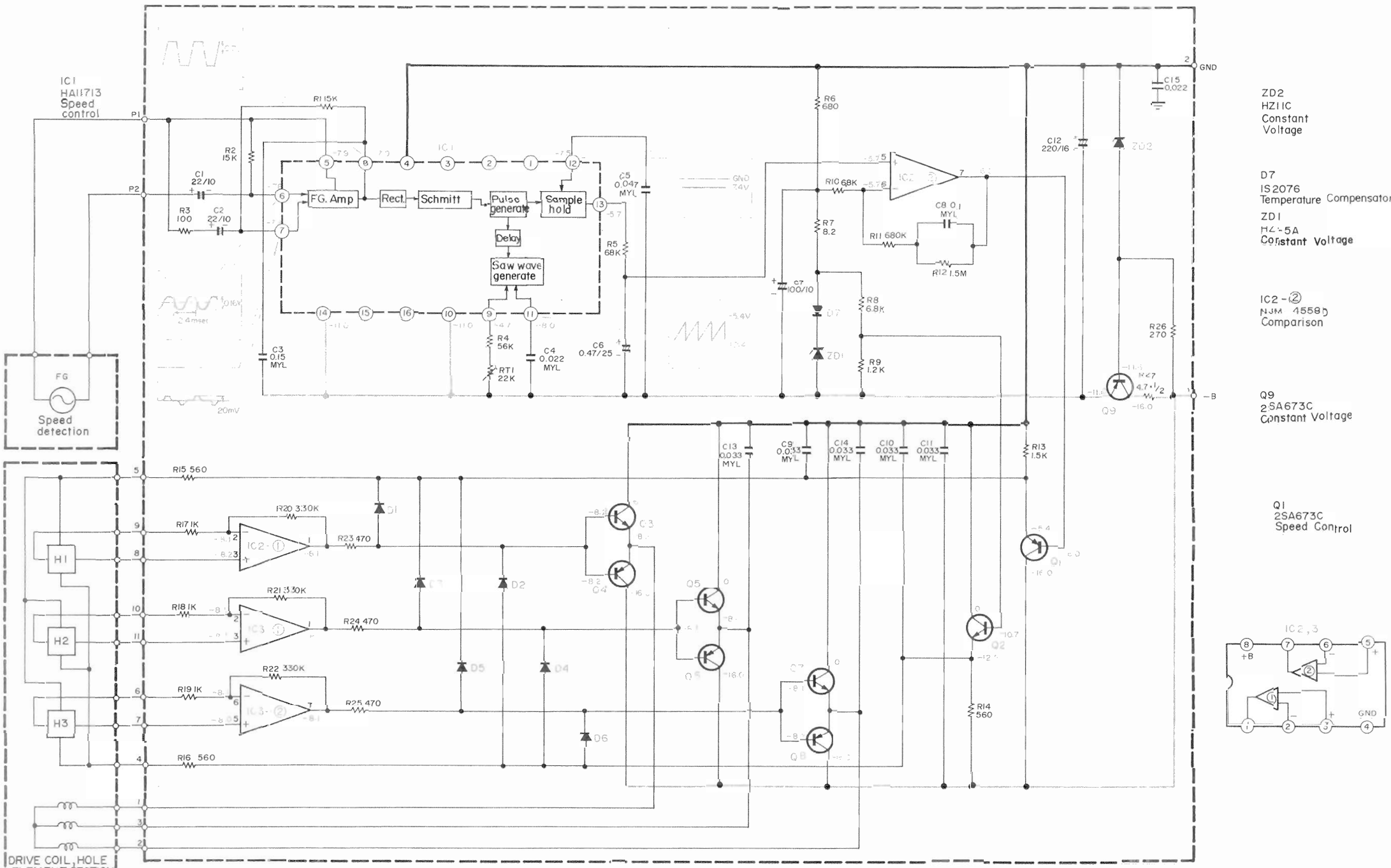


CIRCUIT BOARD DIAGRAM (ATRS Section)

: +B : Ground : Signal, others



SCHEMATIC DIAGRAM (Motor Control Section)



ZD2
HZ11C
Constant Voltage

D7
IS2076
Temperature Compensator

ZD1
HZ-5A
Constant Voltage

IC2-②
NJM 4558D
Comparison

Q9
2SA673C
Constant Voltage

Q1
2SA673C
Speed Control

IC2-①, IC3-①,②
NJM4558D
3-Phase Amp.

D1~D6
IS2076
Rect.

Q3,Q5,Q7
2SD468C
Driver

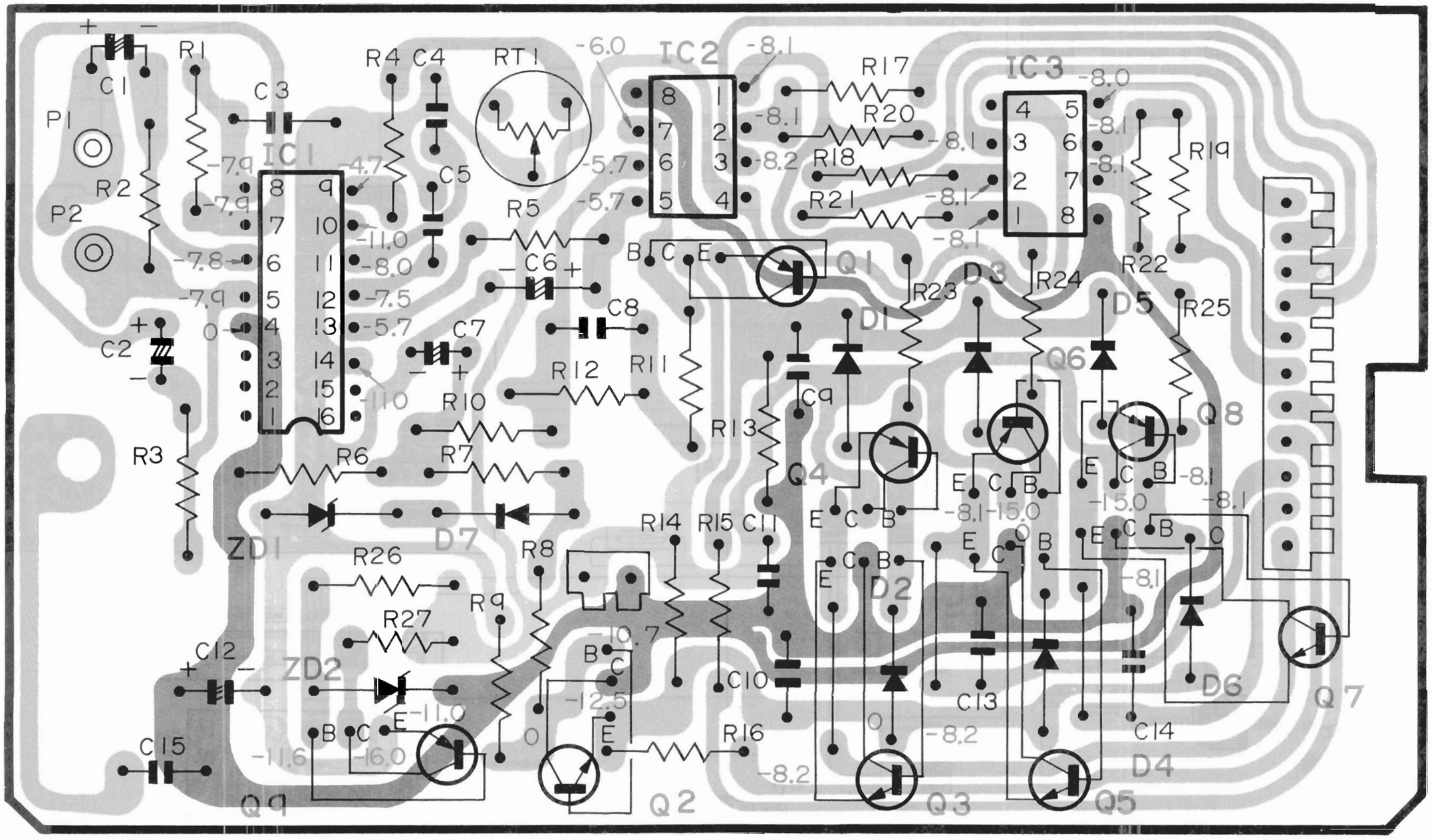
Q4,Q6,Q8
2SB562C
Driver

Q2
2SC458C
Refference Voltage setting

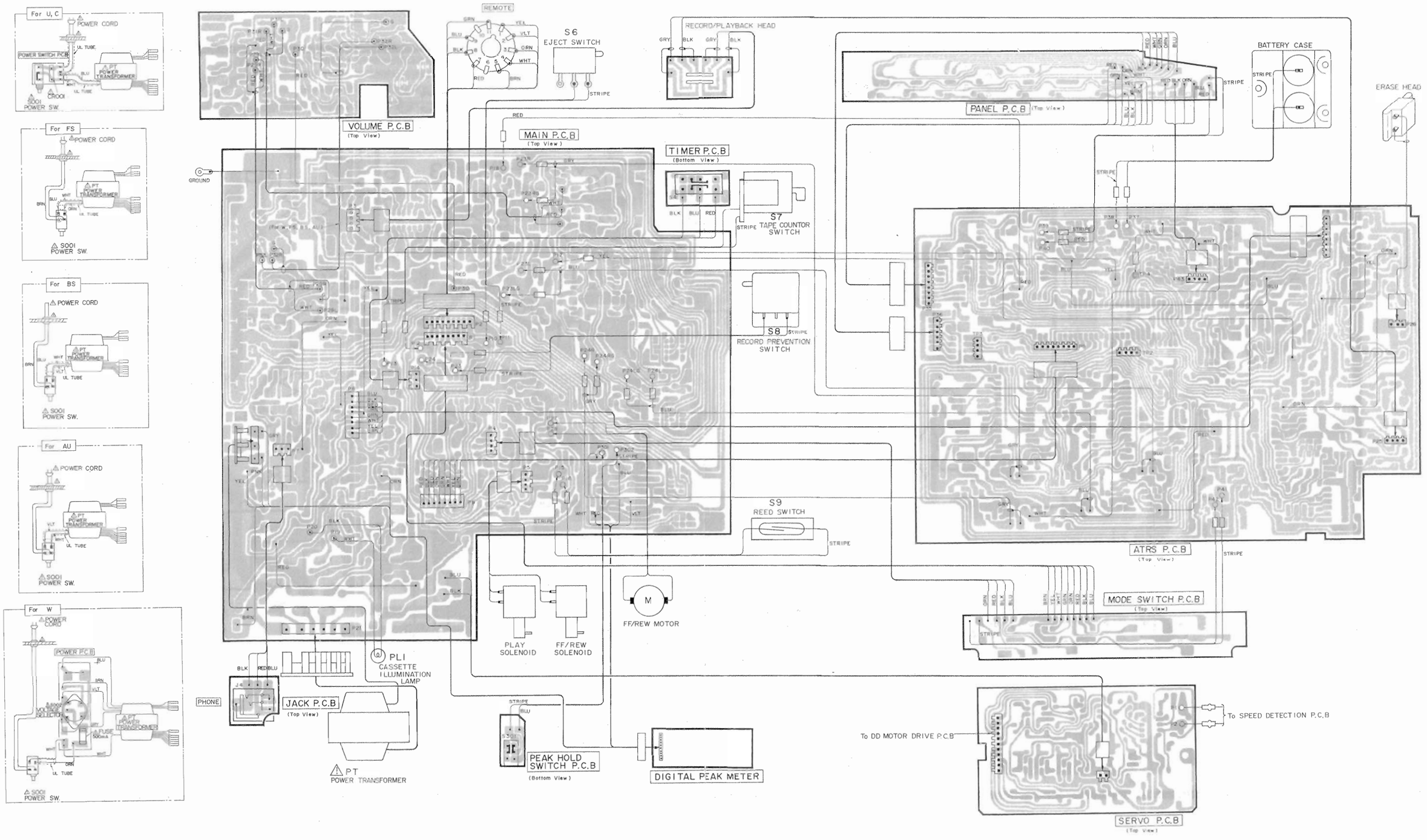
D-3300M	D-3300M

CIRCUIT BOARD DIAGRAM (Motor Control Section)

: –B : Ground : Signal, others

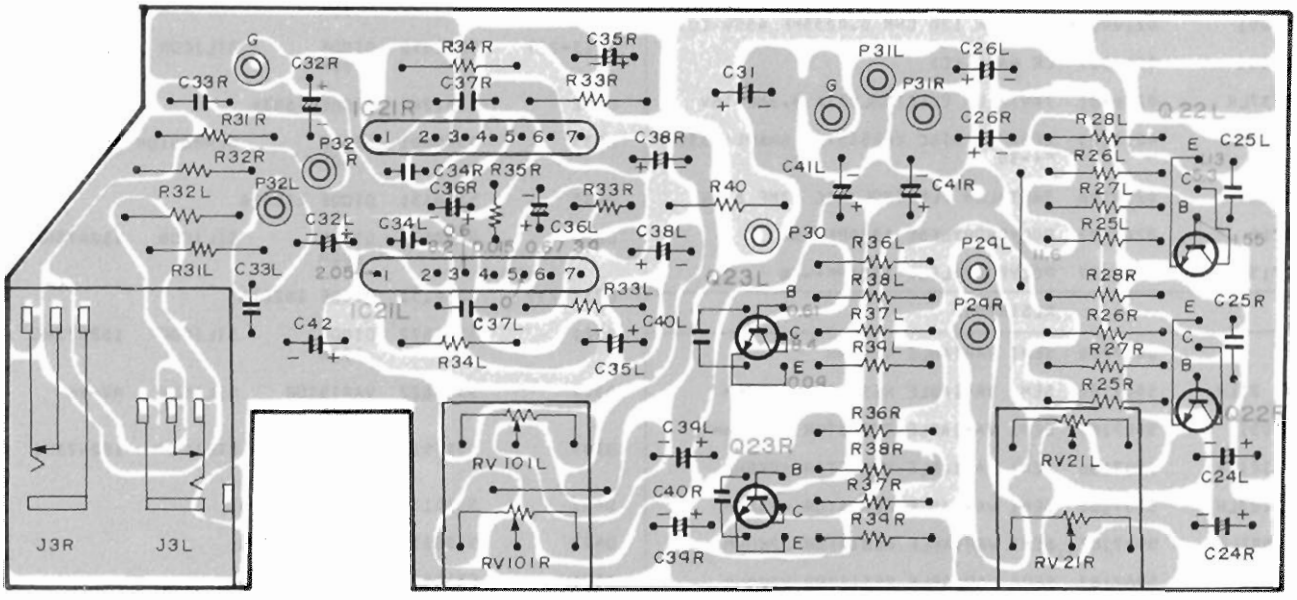


WIRING DIAGRAM



: +B : GROUND : Signal, others

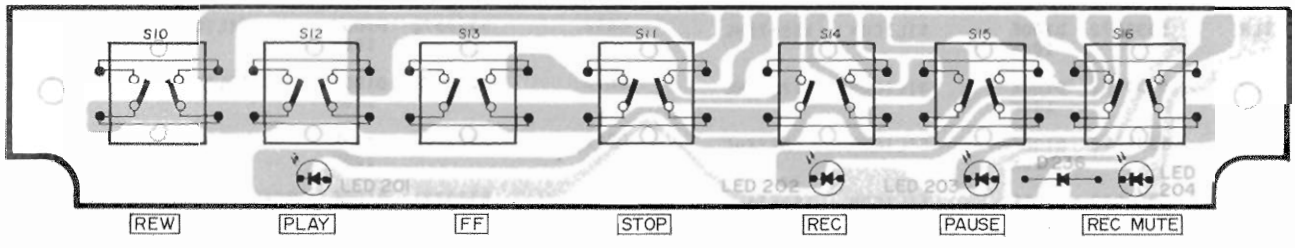
Volume PC Board

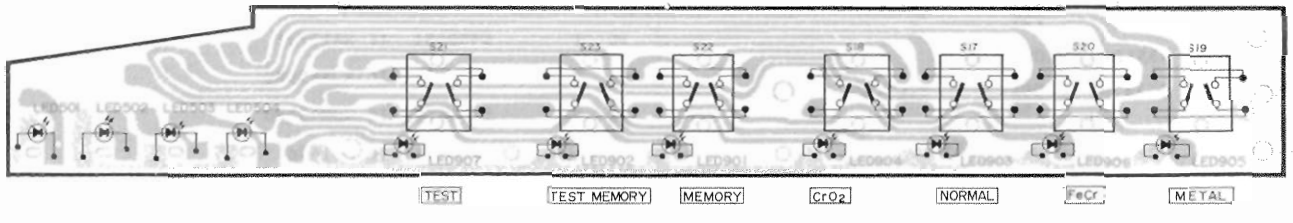


J 3 | RV 101 | RV 21

MIC | RECORD MIC | RECORD LINE

Mode Switch PC Board





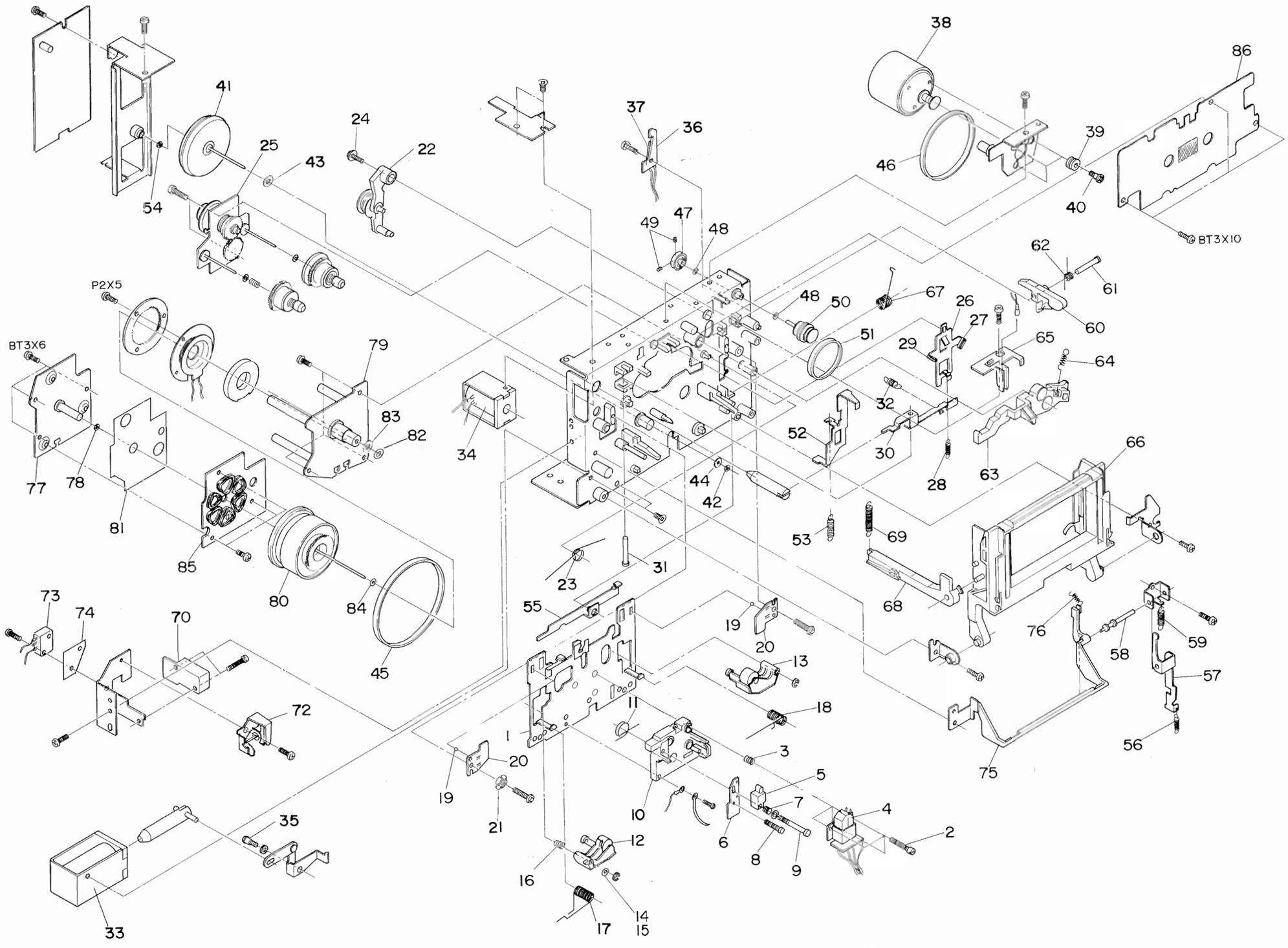
REPLACEMENT PARTS LIST

SYMBOL-NO	P-NO	DESCRIPTION
		CAPACITORS
⚠ CR001	0219902	CR PACK 120 OHM 0.0033MF 450V (U)
⚠ CR001	0219907	CR PACK (C)
C137LR	0256381	TANTALUM ELECTROLYTIC 3.3MF 16V
C237	0209023	CERAMIC DISC (RESISTOR SHAPE) 3300P F+-30
C510	0256396	TANTALUM ELECTROLYTIC 47MF 6.3V
C712	0268427	POLYPROPYLENE 3300PF+-5%
C713	0268427	POLYPROPYLENE 3300PF+-5%
		RESISTORS
RT 1	5007226	SEMI VARIABLE 47KOHM
RT 21LR	5007186	SEMI VARIABLE RESISTOR 10KOHM
RT051	5007189	SEMI VARIABLE RESISTOR 100KOHM
RT101LR	5007186	SEMI VARIABLE RESISTOR 10KOHM
RT103LR	5007188	SEMI VARIABLE RESISTOR 47KOHM
RT601LR	5007187	SEMI VARIABLE RESISTOR 22KOHM
RT602LR	5007187	SEMI VARIABLE RESISTOR 22KOHM
RT701LR	5007189	SEMI VARIABLE RESISTOR 100KOHM
RT801LR	5007186	SEMI VARIABLE RESISTOR 10KOHM
RV 21	5000558	VARIABLE RESISTOR 20KOHM(A)
RV101	5000558	VARIABLE RESISTOR 20KOHM(A)
RV102	5000145	VARIABLE 10KOHM(B)
R205	0169113	WINDING RESISTOR 47OHM+-5% 5W
R303	0170407	FUSE RESISTOR 10OHM+-5% 1/2W
		SEMI-CONDUCTORS
D 1-7	5330131	DIODE 1S2076
D 21LR	5330572	DIODE 100M SILICON 1S2473HC
D 22LR	5330572	DIODE 100M SILICON 1S2473HC
D101	5330572	DIODE 100M SILICON 1S2473HC
D102LR	5330572	DIODE 100M SILICON 1S2473HC
D103	5330721	DIODE GERMANIUM 1N34A 10MHZ 50MW
D106	5330572	DIODE 100M SILICON 1S2473HC
D107	5331241	DIODE 1SR34
D201	5331241	DIODE 1SR34
D202	5331241	DIODE 1SR34
D203	5330101	DIODE 15K SILICON V06C
D204	5331241	DIODE 1SR34
D205	5330101	DIODE 15K SILICON V06C
D206-208	5331241	DIODE 1SR34
D209	5330101	DIODE 15K SILICON V06C
D210	5330572	DIODE 100M SILICON 1S2473HC
D211	5331241	DIODE 1SR34
D212	5330101	DIODE 15K SILICON V06C
D213-227	5330572	DIODE 100M SILICON 1S2473HC
D232	5331241	DIODE 1SR34
D233	0575001	DIODE 10M GERMANIUM 1N34A
D235	5330131	DIODE 1S2076
D236	5330572	DIODE 100M SILICON 1S2473HC
D237-239	5330131	DIODE 1S2076
D301	5330572	DIODE 100M SILICON 1S2473HC
D302	5340022	VARISTOR 10K SILICON HV-46
D303	5330572	DIODE 100M SILICON 1S2473HC
D401	5330131	DIODE 1S2076
D402	5330131	DIODE 1S2076
D501	5330571	DIODE 1S2473VE
D502	5330572	DIODE 100M SILICON 1S2473HC
D503	5330572	DIODE 100M SILICON 1S2473HC
D504-507	5330571	DIODE 1S2473VE
D508	5330572	DIODE 100M SILICON 1S2473HC
D509	5330131	DIODE 1S2076
D510	5330131	DIODE 1S2076
D801LR	5330572	DIODE 100M SILICON 1S2473HC
D802	5330572	DIODE 100M SILICON 1S2473HC
D803	5330572	DIODE 100M SILICON 1S2473HC
D901	5330572	DIODE 100M SILICON 1S2473HC
D902	5330721	DIODE GERMANIUM 1N34A 10MHZ 50MW
D903	5330721	DIODE GERMANIUM 1N34A 10MHZ 50MW
D904-912	5330572	DIODE 100M SILICON 1S2473HC
D914	5330131	DIODE 1S2076
D915	5330572	DIODE 100M SILICON 1S2473HC
D916	5330131	DIODE 1S2076
D917	5340022	VARISTOR 10K SILICON HV-46
IC 1	5352101	IC HA11713
IC 2	5350601	IC NJM4558D
IC 3	5350601	IC NJM4558D
IC 21LR	5350251	IC HA1406
IC101	5350301	IC HA-1452
IC201	5350852	IC HA12001
IC501LR	5352271	IC HA12020
IC502	5350301	IC HA-1452

SYMBOL-NO	P-NO	DESCRIPTION
		SEMI-CONDUCTORS
IC504	5350601	IC NJM4558D
IC601	5359853	IC HD44750A16
IC801	5350301	IC HA-1452
IC802	5350601	IC NJM4558D
IC901	5359471	IC HD7404P
LED201	5380242	LED GL 3PG1
LED202	5380241	LED GL 3PR1
LED203	5380242	LED GL 3PG1
LED204	5380241	LED GL 3PR1
LED501-504	5380101	LED SLP-24B
LED901-904	5380112	LED SLP224B
LED905-907	5380101	LED SLP-24B
MOD 21LR	5356834	MODULE TA3003DR
MOD201	5356982	MODULE TA4030
Q 1	5320593	TRANSISTOR SILICON 2SA673C 80M
Q 2	0573481	TRANSISTOR SILICON 2SC458 230M
Q 3	5321213	TRANSISTOR 2SD468C 190MHZ 0.9MW
Q 4	5321203	TRANSISTOR SILICON 2SB562C 350MHZ 0.9W
Q 5	5321213	TRANSISTOR 2SD468C 190MHZ 0.9MW
Q 6	5321203	TRANSISTOR SILICON 2SB562C 350MHZ 0.9W
Q 7	5321213	TRANSISTOR 2SD468C 190MHZ 0.9MW
Q 8	5321203	TRANSISTOR SILICON 2SB562C 350MHZ 0.9W
Q 9	5320593	TRANSISTOR SILICON 2SA673C 80M
Q 21LR	5320024	TRANSISTOR SILICON 2SC458DLG 230M
Q 22LR	5320024	TRANSISTOR SILICON 2SC458DLG 230M
Q 23LR	5320024	TRANSISTOR SILICON 2SC458DLG 230M
Q101LR	5321506	TRANSISTOR 2SK68A-N
Q102LR	5321295	TRANSISTOR 2SC1740E
Q103LR	5320024	TRANSISTOR SILICON 2SC458DLG 230M
Q104LR	5321194	TRANSISTOR 2SD467BC
Q105	5321295	TRANSISTOR 2SC1740E
Q106	5321295	TRANSISTOR 2SC1740E
Q107LR	5321194	TRANSISTOR 2SD467BC
Q108LR	5321295	TRANSISTOR 2SC1740E
Q202	5320671	TRANSISTOR SILICON 2SC1061B 5M
Q203	5320643	TRANSISTOR SILICON 2SC1162 150M
Q204	5320643	TRANSISTOR SILICON 2SC1162 150M
Q205	5320671	TRANSISTOR SILICON 2SC1061B 5M
Q206	5320671	TRANSISTOR SILICON 2SC1061B 5M
Q207	5320643	TRANSISTOR SILICON 2SC1162 150M
Q208-210	5321295	TRANSISTOR 2SC1740E
Q211	5320643	TRANSISTOR SILICON 2SC1162 150M
Q212	5321295	TRANSISTOR 2SC1740E
Q213	5321295	TRANSISTOR 2SC1740E
Q214	5320603	TRANSISTOR SILICON 2SA673A-C 80MHZ 400MW
Q215	5320671	TRANSISTOR SILICON 2SC1061B 5M
Q301	5321295	TRANSISTOR 2SC1740E
Q501-505	5321295	TRANSISTOR 2SC1740E
Q601LR	5320024	TRANSISTOR SILICON 2SC458DLG 230M
Q602	5321295	TRANSISTOR 2SC1740E
Q603LR	5320024	TRANSISTOR SILICON 2SC458DLG 230M
Q604LR	5321295	TRANSISTOR 2SC1740E
Q605LR	5321295	TRANSISTOR 2SC1740E
Q606LR	5321295	TRANSISTOR 2SC1740E
Q701-704	5321295	TRANSISTOR 2SC1740E
Q705	5322651	TRANSISTOR 2SD667C
Q706	5322651	TRANSISTOR 2SD667C
Q707	5320651	TRANSISTOR SILICON 2SC454 230M
Q708	5320651	TRANSISTOR SILICON 2SC454 230M
Q709	5320671	TRANSISTOR SILICON 2SC1061B 5M
Q710	5320603	TRANSISTOR SILICON 2SA673A-C 80MHZ 400MW
Q711	5320603	TRANSISTOR SILICON 2SA673A-C 80MHZ 400MW
Q712	5321295	TRANSISTOR 2SC1740E
Q801LR	5321295	TRANSISTOR 2SC1740E
Q802	5321295	TRANSISTOR 2SC1740E
Q803LR	5321295	TRANSISTOR 2SC1740E
Q901-904	5321295	TRANSISTOR 2SC1740E
Q906	5321295	TRANSISTOR 2SC1740E
TH701	5340231	THERMISTER 112302-2
ZD 1	5331014	ZENER DIODE HZ5A
ZD 2	5330553	ZENER DIODE HZ11C
ZD101	5330322	ZENER DIODE SILICON TR-9S 10K
ZD202	5330541	ZENER DIODE HZ-15
ZD203	5330981	ZENER DIODE HZ27
ZD204	5330483	ZENER DIODE AW01-7
ZD205	5330483	ZENER DIODE AW01-7
ZD206	5330392	ZENER DIODE SILICON HZ6B 1MHZ 400MW
ZD207	5330392	ZENER DIODE SILICON HZ6B 1MHZ 400MW

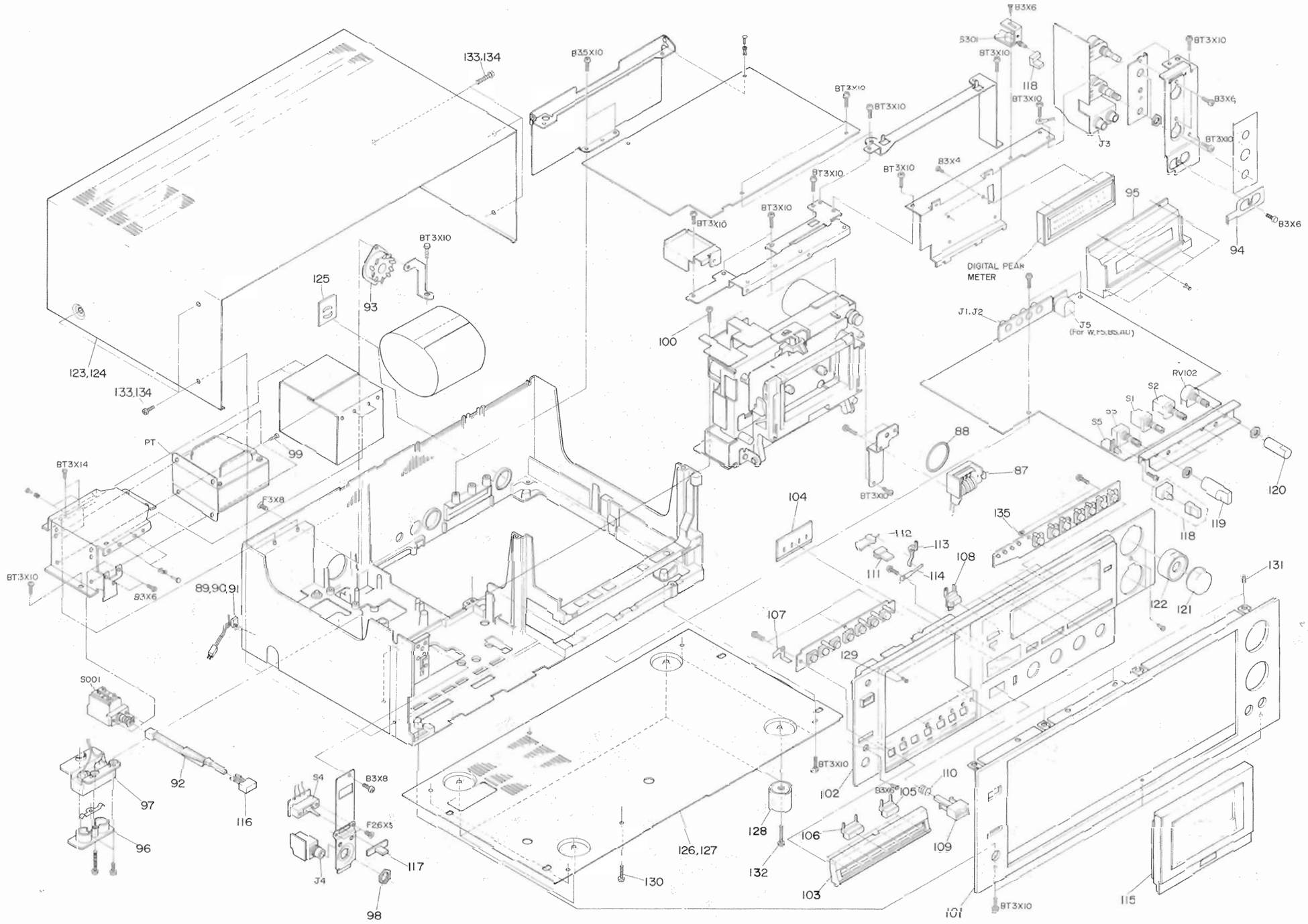
SYMBOL-NO	P-NO	DESCRIPTION
		SEMI-CONDUCTORS
ZD209	5330056	ZENER DIODE AW01-20
ZD210	5330602	ZENER DIODE AW01-16
ZD211	5330711	ZENER DIODE HZ4BC
ZD212	5330312	ZENER DIODE SILICON
ZD301	5330711	ZENER DIODE HZ4BC
ZD601	5330532	DIODE SILICON HZ-12B 1.0M
		TRANSFORMERS
⚠ PT	5212791	POWER TRANSFORMER (FS)
⚠ PT	5212792	POWER TRANSFORMER (BS)
⚠ PT	5212793	POWER TRANSFORMER (AU)
⚠ PT	5212794	POWER TRANSFORMER (W)
⚠ PT	5212801	POWER TRANSFORMER (U,C)
		COILS
L 21LR	5161663	DOLBY FILTER
L101LR	5161663	DOLBY FILTER
L201	0333151	PEAKING COIL 36MH
L601LR	5260215	TRAP COIL 33HH
L602LR	5260361	CHOKE COIL 33MH
L603	5260022	OSCILLATOR COIL
L604	5260022	OSCILLATOR COIL
L605	5260215	TRAP COIL 33HH
L606LR	0333151	PEAKING COIL 36MH
		MISCELLANEOUS
	5310431	DIGITAL PEAK METER
	5351011	HALL ELEMENT
⚠ F1	5720175	FUSE 0.8A
⚠ F2	5721061	FUSE 1.6A
⚠ F3	5721061	FUSE 1.6A
⚠ F4	5721063	FUSE 1.25AT
⚠ F5	5720175	FUSE 800MA (W)
J1LR	5676082	PIN JACK (LINE IN)
J2LR	5676082	PIN JACK (LINE OUT)
J3LR	5674211	MIC JACK
J4	5674191	JACK (PHONE)
J5	5651141	5P DIN SOCKET (W, FS, BS, AU)
PL1	5762036	PILOT LAMP
RL301	5641141	REED RELAY
RL901	5641141	REED RELAY
S 1	5612291	ROTARY SWITCH-DOLBY NR/MPX
S 2	5612295	ROTARY SWITCH-MONITOR
S 3	5612292	ROTARY SWITCH-AUTO REWIND
S 4	5620852	SLIDE SWITCH-TIMER
S 5	5633313	PUSH SWITCH-MEMORY
S 10- 16	5633352	PUSH SWITCH-PLAY, REC, STOP, FF, REW, PAUSE REC MUTE
S 17- 23	5633352	PUSH SWITCH-NOR, FeCr, CrO_2, METAL, TEST, MEMORY, TEST MEMORY
⚠ S001	5633482	PUSH SWITCH-POWER (U,C)
⚠ S001	5633541	PUSH SWITCH-POWER (W, FS, BS, AU)
⚠ S002	5605081	ROTARY SWITCH-VOLTAGE SELECTOR (W)
S301	5633313	PUSH SWITCH-PEAK HOLD
⚠	5746442	POWER CORD (U,C)
⚠	5746157	POWER CORD (W,FS)
⚠	5746342	POWER CORD (BS)
⚠	5746571	POWER CORD (AU)
		FOR ACCESSORIES
⚠	5662021	SOCKET ADAPTER (W)
	7740321	HEAD CLEANING STICK
	5894163	PATCH CORD
		FOR CASSETTE DECK ASSEMBLY (A)
1	7320481	HEAD PLATE ASSEMBLY
2	7781751	SPECIAL SCREW
3	6321243	HEAD SPRING
4	5444861	RECORD PLAYBACK HEAD
5	5445312	ERASE HEAD
6	7320531	ADJUST PLATE FOR ERASE HEAD
7	6321192	SPRING
8	7780554	SCREW
9	7781921	PAN HEAD SCREW-2MMDX25MM
10	6973092	HEAD BASE
11	6545321	SPRING
12	6383281	PRESSURE ROLLER ARM ASSEMBLY
13	6383315	PRESSURE ROLLER ARM ASSEMBLY
14	7786215	POLYSLIDER WASHER
15	7786216	POLYSLIDER WASHER
16	6304721	ADJUST SPRING
17	6308571	SPRING
18	6308563	SPRING
19	6998275	BALL
20	7300112	BALL PRESS
21	7189545	LOCKING WASHER
22	6413032	TAKE UP ARM ASSEMBLY
23	6308553	SPRING
24	7781132	BT SCREW
25	6412753	TURNTABLE HOLDER ASSEMBLY
26	7300124	BRAKE PLATE
27	6586003	BRAKE RUBBER
28	6300181	SPRING
29	6586002	BRAKE RUBBER
30	7300134	FR LEVER
31	7543424	LEVER SHAFT
32	6302062	SPRING

EXPLODED VIEW (Cassette Chassis)



Note:
Components marked without numbers in this drawing are not specified as replacement parts.

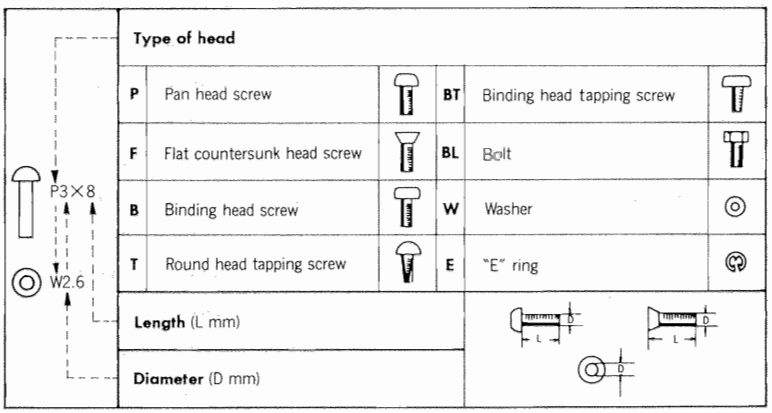
EXPLODED VIEW (Cabinet)



Note:
Components marked without numbers in this drawing are not specified as replacement parts.

SYMBOL-NO	P-NO	DESCRIPTION
		FOR CASSETTE DECK ASSEMBLY (A)
33	5642394	SOLENOID ASSEMBLY
34	5642382	SOLENOID ASSEMBLY
35	7781591	BT SCREW-2.6MMD
36	5909221	REED RELAY P.C.B
37	5641301	REED RELAY
38	5572791	MOTOR ASSEMBLY
39	6576084	RUBBER PLATE
40	7539002	SCREW FOR MOTOR MOUNTING
41	6373501	FLYWHEEL ASSEMBLY
42	7786623	POLYSLIDER WASHER
43	7778848	POLYSLIDER WASHER
44	7779811	WASHER
45	6357302	FLYWHEEL BELT
46	6357293	FR BELT
47	7109653	MAGNET ASSEMBLY
48	7778852	POLYESTER WASHER
49	0638564	MOTOR PULLEY HOLDING SCREW
50	6421741	COUNTER PULLEY
51	6354381	SENSING BELT
52	7307943	RECORD SLIDER
53	6301011	LOCK LEVER SPRING
54	7768686	THRUST SUPPORT
55	7301083	HEAD PLATE RETURN LEVER
56	6302376	SPRING
57	7301604	EJECT LEVER
58	7544021	LEVER SHAFT
59	6302821	SPRING FOR EJECT LEVER
60	6748564	LOCK ARM
61	7543429	LEVER SHAFT
62	6308983	SPRING
63	6752012	CASSETTE HOLDER ARM
64	6302811	SPRING
65	6748653	LAMP HOLDER
66	6091721	CASSETTE TRAY ASSEMBLY
67	6308932	SPRING
68	6748803	DAMPER ARM ASSEMBLY
69	6302602	SPRING FOR DAMPER ARM
70	5601121	MICRO SWITCH
71	7768683	THRUST SUPPORT
72	7290501	GOVERNOR
73	5633361	PUSH SWITCH
74	7763811	INSULATING FIBER
75	6750021	EJECTER ASSEMBLY
76	6302576	EJECTER SPRING
77	7321902	STATOR YOKE ASSEMBLY
78	7768686	THRUST SUPPORT
79	7041291	MOTOR HOLDER ASSEMBLY
80	6373481	ROTOR ASSEMBLY
81	7745432	INSULATION SHEET
82	7779811	WASHER
83	7786623	POLYSLIDER WASHER
84	7786219	POLYESTER WASHER
85	5978131	COIL P.C.B ASSEMBLY
		FOR CASSETTE DECK ASSEMBLY (B)
86	6630995	CASSETTE METAL ASSEMBLY
87	5559182	MEMORY COUNTER
88	6354631	COUNTER BELT
⚠ 89	6711351	BUSHING (BS)
⚠ 90	6794081	BUSHING (U.C.AU)
⚠ 91	6794141	BUSHING (W.FS)
92	6757752	SWITCH LEVER
93	5650801	11P MOULD SOCKET
94	6533382	EARTH SPRING
95	6203911	METER FILTER ASSEMBLY
96	6488361	BATTERY COVER ASSEMBLY
97	6488372	BATTERY CASE ASSEMBLY
98	7772951	NUT
99	8699610	BT BIND SCREW-4MMDX10MM
100	8699410	BT BIND HEAD SCREW-3MMDX10MM (BLACK)
		MISCELLANEOUS
101	6671772	FRONT PANEL
102	6223322	SUB PANEL ASSEMBLY
103	6757831	FUNCTION METAL ASSEMBLY
104	6223342	LED FRAME ASSEMBLY
105	6257721	FUNCTION BUTTON ASSEMBLY
106	6257722	FUNCTION BUTTON ASSEMBLY (STOP)
107	6533371	EARTH SPRING
108	6052751	PUSH BUTTON ASSEMBLY
109	6052721	EJECT BUTTON ASSEMBLY
110	6320873	SPRING
111	6152741	RESET BUTTON
112	6158091	RESET LEVER (A)
113	6158102	RESET LEVER (B)
114	6533392	RESET SPRING
115	6192511	CASSETTE DOOR ASSEMBLY
116	6152761	PUSH BUTTON ASSEMBLY (POWER)
117	6196701	KNOB (TIMER)
118	6152731	BUTTON ASSEMBLY (MEMORY,PEAK HOLD)
119	6469781	FUNCTION KNOB
120	6469771	KNOB (OUTPUT)
121	6287592	KNOB ASSEMBLY (RECORD L)

SYMBOL-NO	P-NO	DESCRIPTION
		MISCELLANEOUS
122	6289182	KNOB ASSEMBLY (RECORD R)
123	6149428	UPPER COVER (U,C)
124	6149427	UPPER COVER (W,FS,BS,AU)
125	6754291	DIN CAP (U,C)
126	6041971	BOTTOM COVER(U,C,FS,BS,AU)
127	6041972	BOTTOM COVER (W)
128	6796121	FELT LEG
129	0714308	PAN HEAD SCREW-2.6MMDX8MM
130	8699410	BT BIND HEAD SCREW-3MMDX10MM (BLACK)
131	7781581	BT FLAT SCREW-3MMDX10MM
132	7781146	BT SCREW-3MMDX20MM
133	7781731	BT BIND SCREW-4MMDX10MM (W,FS,BS,AU)
134	8699610	BT BIND SCREW-4MMDX10MM (U,C)
135	0921847	WASHER-FIBBER WASHER



When ordering hardware excluding stated on these lists, be sure to make your orders with type and size.

D-3300M

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Codes : All Codes Used

Printed in Japan (K)

HITACHI

SERVICE MANUAL

TK | No. 1500E

D-3300M

(U, C, FS, BS, AU, W)

TROUBLESHOOTING

This troubleshooting manual describes examples of faults and methods of investigating causes. Use this manual together with the previously issued Service Manual No. 1302.

CONTENTS

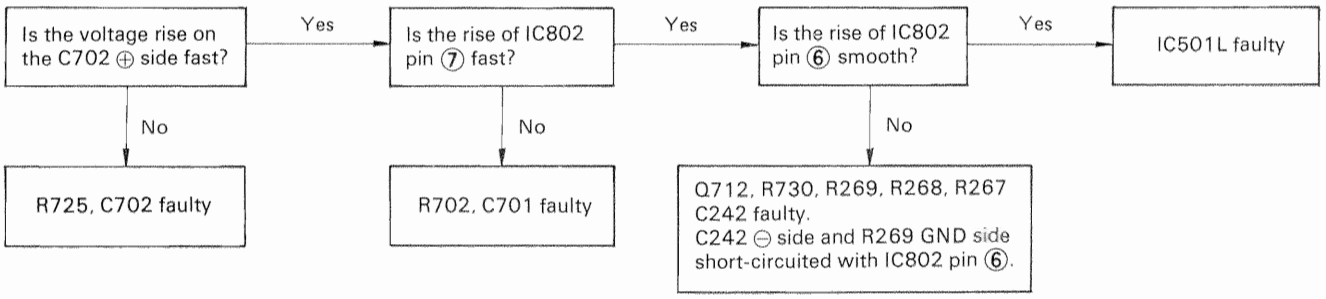
STEREO CASSETTE TAPE DECK

January 1981 TOKAI WORKS

1. FAULTY RISING OF BIAS

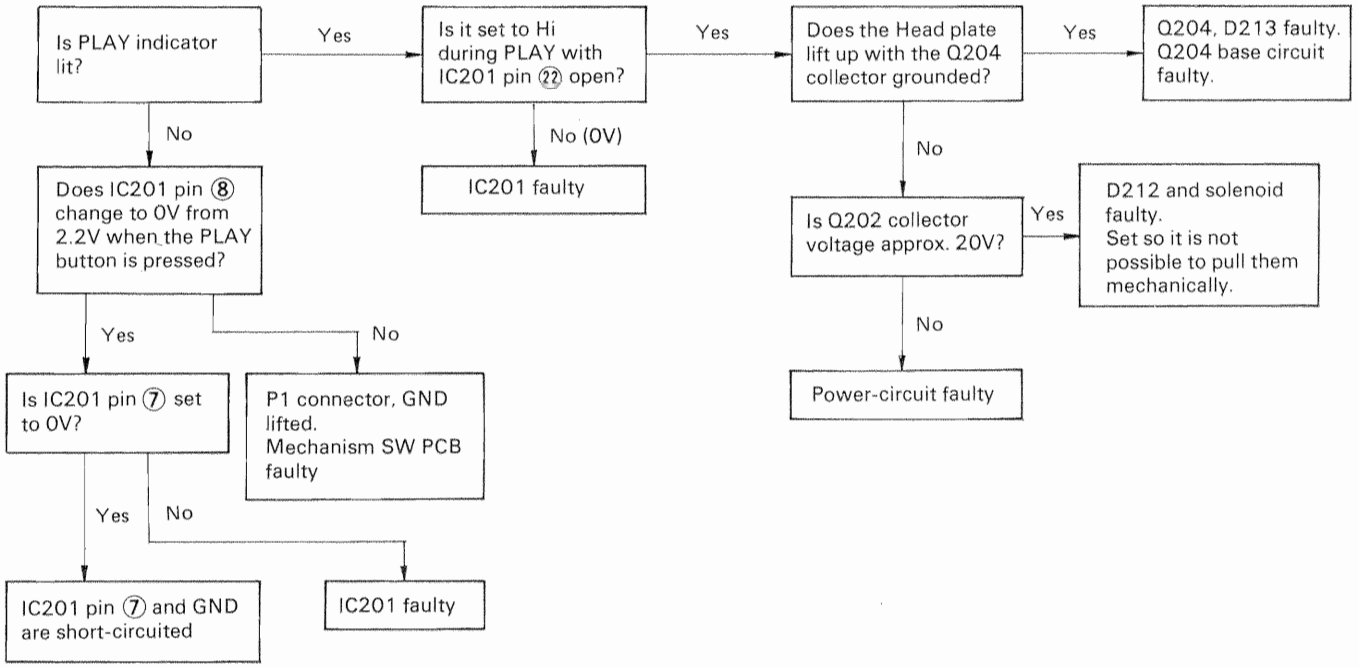
When the sound gradually rises during the STOP → REC mode in the condition in which the signal is input; The bias oscillator increases/decreases the bias current by controlling the power voltage of the oscillator using IC802 and Q709.

Check variation when the STOP mode is changed to the REC mode.



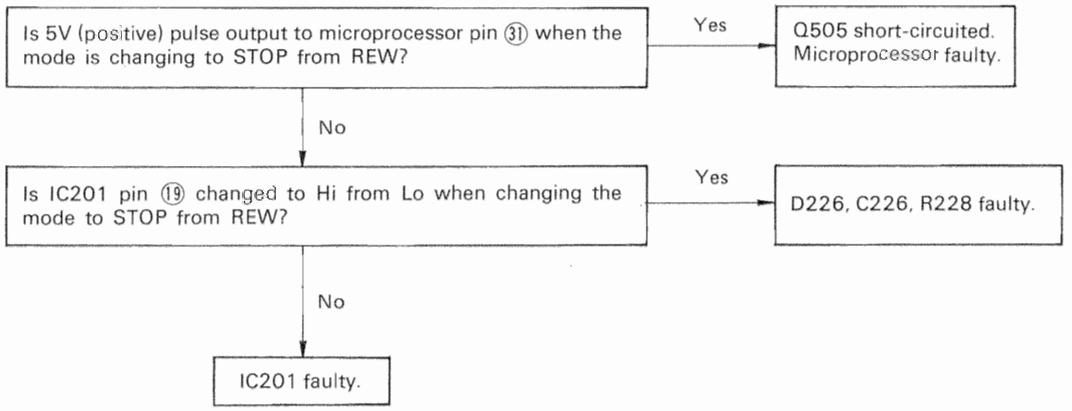
2. HEAD DOES NOT LIFT UP

Check the power voltage (≒ 5V) of IC201 first, when does not FF, REW etc.

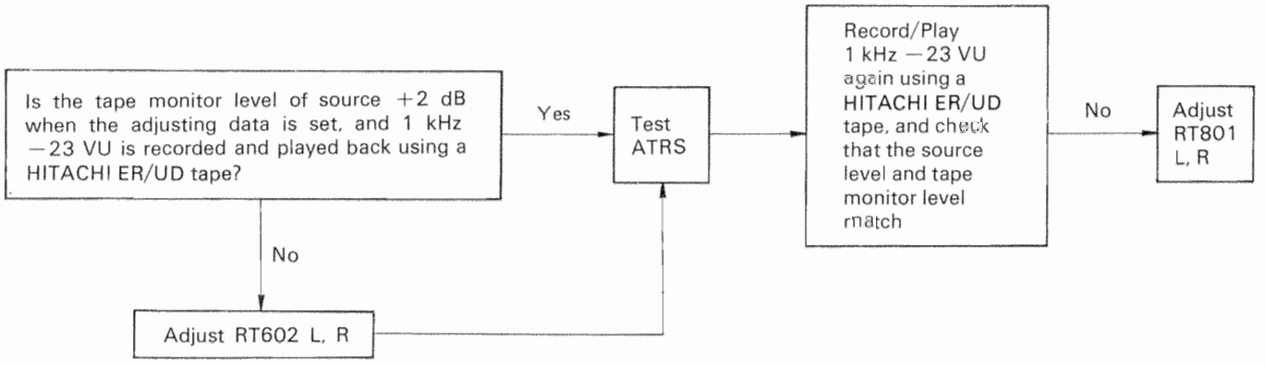


3. TEST LAMP DOES NOT GO OFF

When the TEST lamp (1 kHz) of ATRS does not go off after testing is complete; Approx. 5V positive pulse is generated by D225 ~ 7, C226 ~ 8, R228 ~ 32 and Q210, and input to Microprocessor pin ㉛, when testing is completed the lamp goes off; in the 3 cases in which the unit comes out of the PLAY mode, when the unit enters the PAUSE mode during testing, or when the unit comes out of the REW mode during rewinding after testing.



4. REC/PLAY L, R DO NOT MATCH



When RT602 L, R cannot be adjusted:
(1) Setting bias current inadequate
(2) IC501 L, R faulty
(3) RT601 L, R adjusted poorly

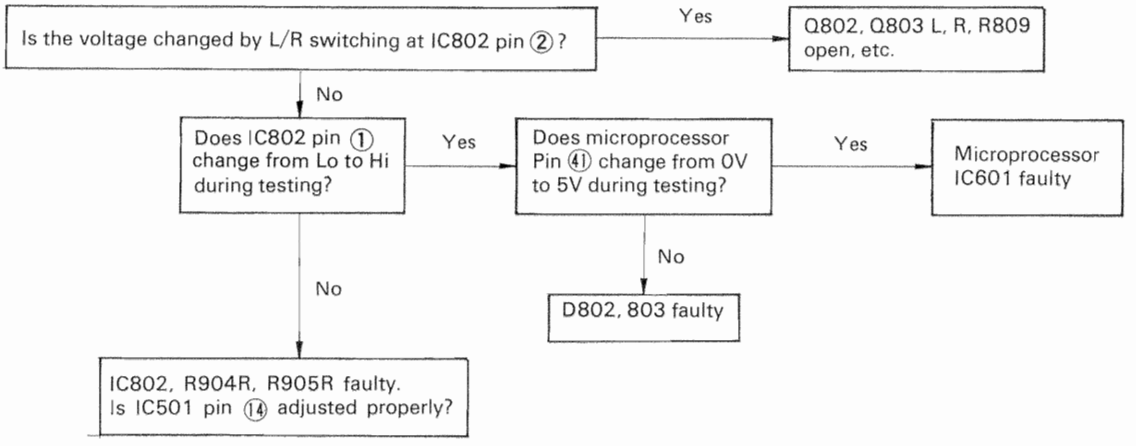
When RT801 L, R cannot be adjusted:
(1) IC501 L, R faulty
(2) A/D circuit faulty

- **A/D circuit faulty**

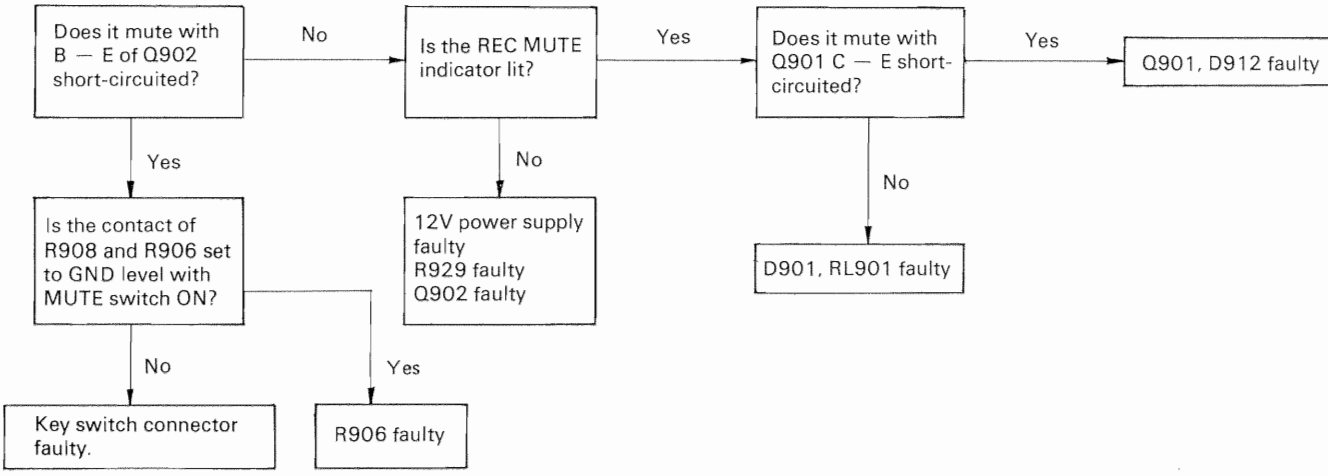
Pull out P23 L, R and input 0 dBm −20 dB (1 kHz) from the external oscillator. Or set the standard data and input 0 − 22 dB (1 kHz and record/play back the signal. Set RT801 L, R to the neutral point. Check the level of each section at that time.

- The output of IC501 L, R pin ④ is approx. −6 dBm. (The OP amp. of IC501 may oscillate at that time depending on the VTVM during measurement. Insert a 10 kΩ resistor in series with the input and perform measurement). —No→ IC501 faulty, IC501 pin ① bias faulty (R816, 801, etc.).
- DC voltage at ⊕ side of C807 is approx. 1V (Measure using a digital voltmeter —No→ IC801, D801 L, R faulty.

- **L/R switching circuit using Q802, Q803 L, R faulty.**



5. REC MUTING IS NOT DONE



6. HIGH FREQUENCY DETERIORATED

Cause:

(1) When the high frequency is deteriorated due to a faulty head, or faulty adjustment in another section of the circuit during the setting of adjustment data, and it is corrected by bias control, the bias value may become unbalanced between L and R.
The optimum bias value is detected on the R CH side during ATRS test, and L CH follows it, so the bias value may become inadequate.

(2) When the high frequency is deteriorated during sourc monitoring: MPX filter faulty, soldertouch, etc.

(3) When the AF oscillator for ATRS testing is not adjuste properly.

(4) Head magnetized

7. DISTORTION GREAT

Cause:

(1) When the bias current is inadequate due to (1) in item 6 above.

(2) Muting circuit faulty. Q107 L, R, Q104 L, R, etc. (Try to set C — E open.)

(3) Head faulty.

8. ATRS DOES NOT OPERATE (When TEST error occurs)

Cause:

(1) When RT801 L, R is set to minimum.

(2) When RT602 L, R is poorly adjusted.

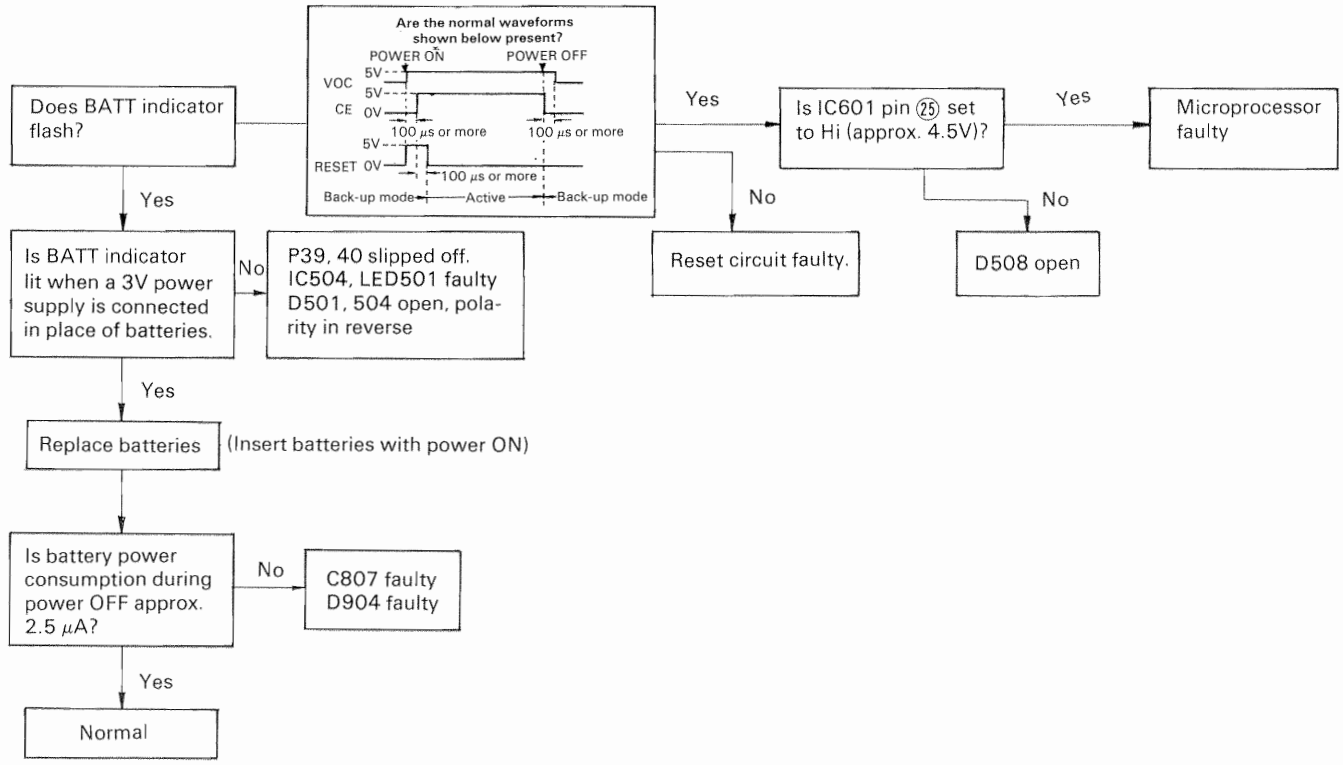
(3) A/D converter circuit faulty.

(4) Microprocessor faulty (especially pin ㊶).

(5) Level deteriorated due to dirt — etc. on the head.

(6) When the testing oscillator is not operating. (Is approx 4 dBm output to C506 ⊖ side?)

9. ATRS DOES NOT MEMORIZE DATA (All the tape selector LEDs flash)



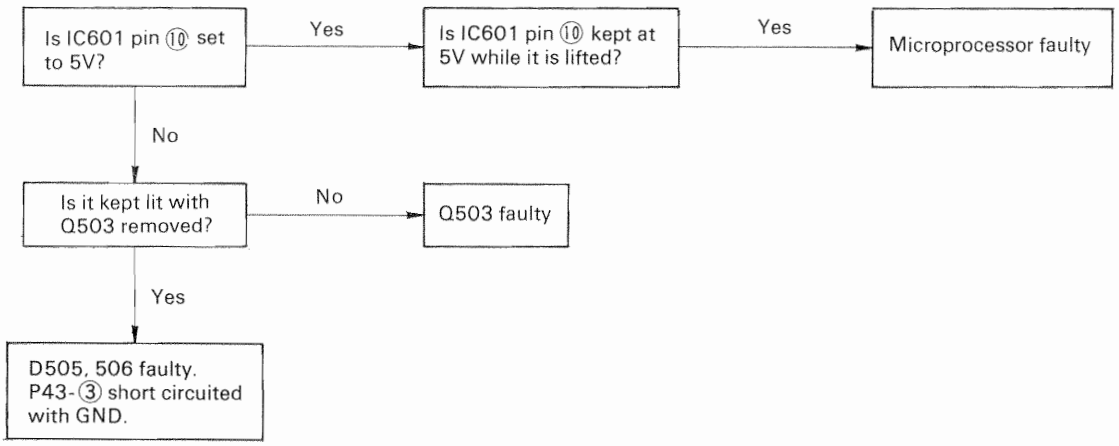
10. ATRS SYSTEM

(1) 15 kHz TEST indicator is kept lit.

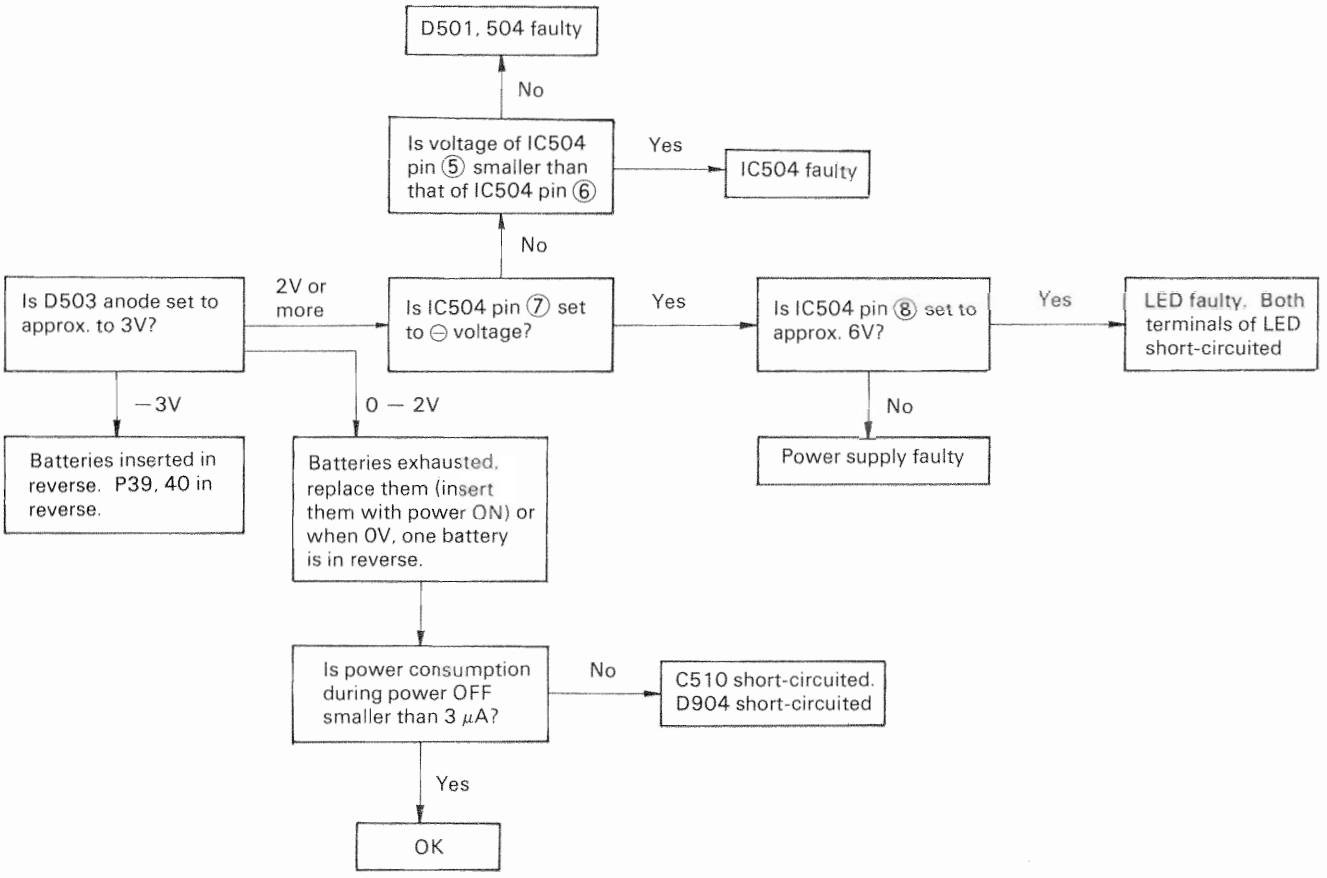
The oscillation of the microprocessor and the oscillation frequency switching control output data are given in the table below.

Oscillation		Oscillation control (D13)	Oscillation frequency control	
			D12	D11
Oscillation stop		0	—	—
During oscillation operation	1 kHz	1	0	0
	7 kHz	1	0	1
	15 kHz	1	1	1

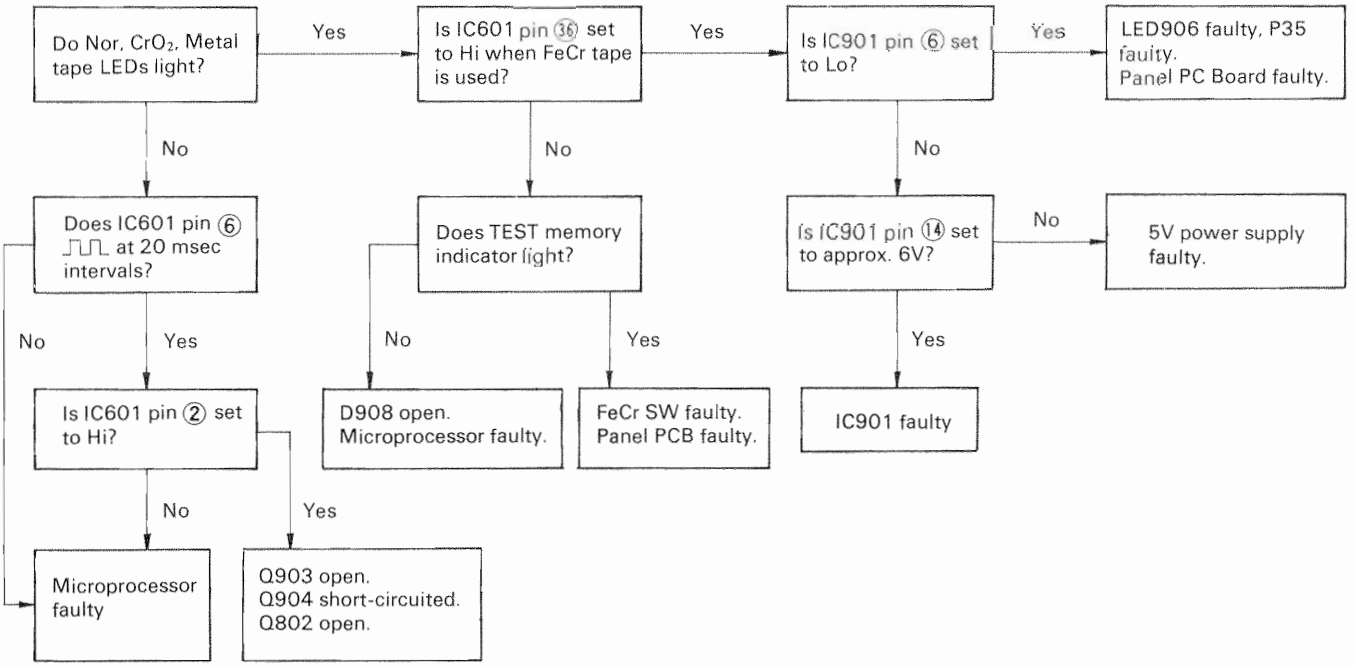
The oscillation frequency during testing is controlled by the output as shown in the table above. The ATRS test indicator uses the signal and lights up.



(2) Battery indicator does not light.

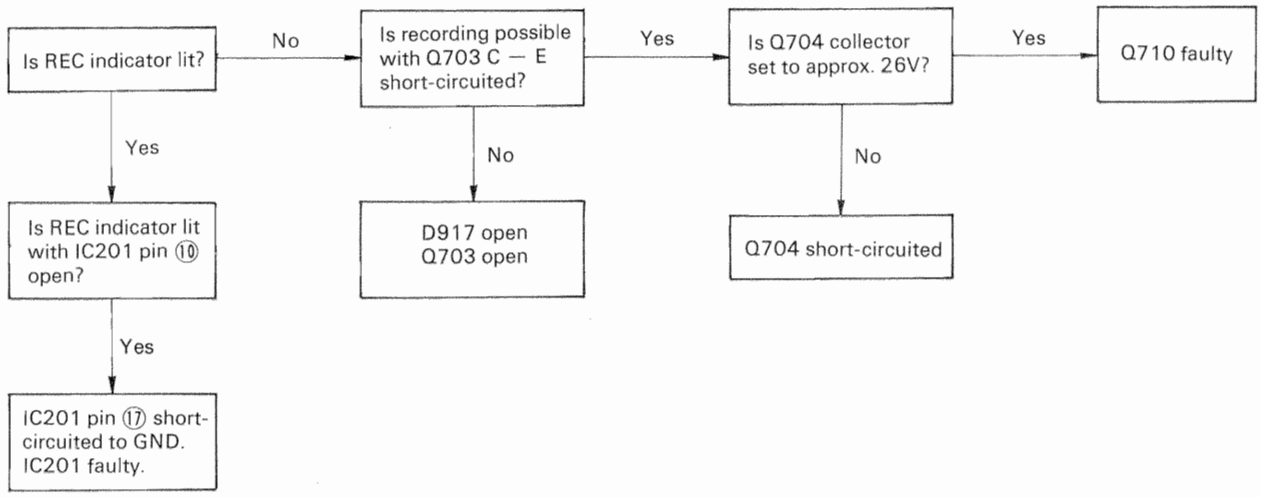


(3) Indicator of FeCr (or Tape select LED) does not light.



11. RECORDING SYSTEM

(1) Enters the ERASE or RECORD mode during PLAY.



12. REC/PLAY FREQUENCY RESPONSE OF LOW FREQUENCY TOO BOOSTED

Cause:

(1) Headphone amp. Q108 L, R B — E short-circuited.
(2) ATRS test performed with tape position confused.
(3) C602 L, R faulty.

13. IMMEDIATELY STOPS WITH STOP → PLAY OPERATION (Especially reduced voltage)

Cause:

(1) Regulation of the 5V power supply is not satisfactory for some reason, and the reset circuit operates with little load fluctuation.
(2) C211 → Capacity small, D206 — 209 disconnected (connect diodes in parallel to check it).
(3) D237, 238 short-circuited, Q214 faulty.

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Codes : All Codes Used

D-3300M TK No. 1500E TOKAI

U, C, FS, BS, AU, W

Printed in Japan ($H.M_2$)

HITACHI
SERVICE MANUAL

TK | **No. 1549E**

D-3300M(U,BS)
(Black)

This cassette deck is the same as the model D-3300M [silver] except that it has the black appearance.

The table below shows the different points from D-3300M [silver], so use together with the D-3300M [silver] Service Manual (No. 1302) issued previously.

REPLACEMENT PARTS LIST

D-3300M(U, BS) [Black]			D-3300M(U, BS) [Silver]	
SYMBOL-NO.	P-NO.	DESCRIPTION	P-NO.	DESCRIPTION
86	6630998	CASSETTE METAL ASSEMBLY	6630995	CASSETTE METAL ASSEMBLY
95	6203912	METER FILTER ASSEMBLY	6203911	METER FILTER ASSEMBLY
—	8699410	BT BIND HEAD SCREW-3MMD x 10MM (BLACK) [FOR CASSETTE METAL MOUNTING]	———	———
—	8737408	FLAT SCREW-3MMD x 8MM (BLACK) [FOR 11P MOULD SOCKET MOUNTING]	———	———
101	6671774	FRONT PANEL	6671772	FRONT PANEL
102	6223324	SUB PANEL ASSEMBLY	6223322	SUB PANEL ASSEMBLY
103	6757832	FUNCTION METAL ASSEMBLY	6757831	FUNCTION METAL ASSEMBLY
105	6257723	FUNCTION BUTTON ASSEMBLY	6257721	FUNCTION BUTTON ASSEMBLY
106	6257724	FUNCTION BUTTON ASSEMBLY (STOP)	6257722	FUNCTION BUTTON ASSEMBLY (STOP)
107	6533372	EARTH SPRING	6533371	EARTH SPRING
108	6052753	PUSH BUTTON ASSEMBLY	6052751	PUSH BUTTON ASSEMBLY
109	6052722	EJECT BUTTON ASSEMBLY	6052721	EJECT BUTTON ASSEMBLY
111	6052742	RESET BUTTON	6052741	RESET BUTTON
115	6092512	CASSETTE DOOR ASSEMBLY	6092511	CASSETTE DOOR ASSEMBLY
116	6052762	PUSH BUTTON ASSEMBLY (POWER)	6052761	PUSH BUTTON ASSEMBLY (POWER)
117	6296704	KNOB (TIMER)	6296701	KNOB (TIMER)
118	6052732	BUTTON ASSEMBLY (MEMORY, PEAK HOLD)	6052731	BUTTON ASSEMBLY (MEMORY, PEAK HOLD)
119	6669783	FUNCTION KNOB	6669781	FUNCTION KNOB
120	6669773	KNOB (OUTPUT)	6669771	KNOB (OUTPUT)
121	6287594	KNOB ASSEMBLY (RECORD L)	6287592	KNOB ASSEMBLY (RECORD L)
122	6289184	KNOB ASSEMBLY (RECORD R)	6289182	KNOB ASSEMBLY (RECORD R)
123	6043374	UPPER COVER (U)	6149428	UPPER COVER (U)
124	6043374	UPPER COVER (BS)	6149427	UPPER COVER (BS)
128	6796123	FELT LEG	6796121	FELT LEG
132	8671420	DT BIND SCREW-3MMD x 20MM	7781146	BT SCREW-3MMD x 20MM
133	8699610	BT BIND SCREW-4MMD x 10MM (BLACK)	7781731	BT BIND SCREW-4MMD x 10MM

SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

STEREO CASSETTE TAPE DECK

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D-3300M(Black) **TK** **No. 1549E** **TOKAI**

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