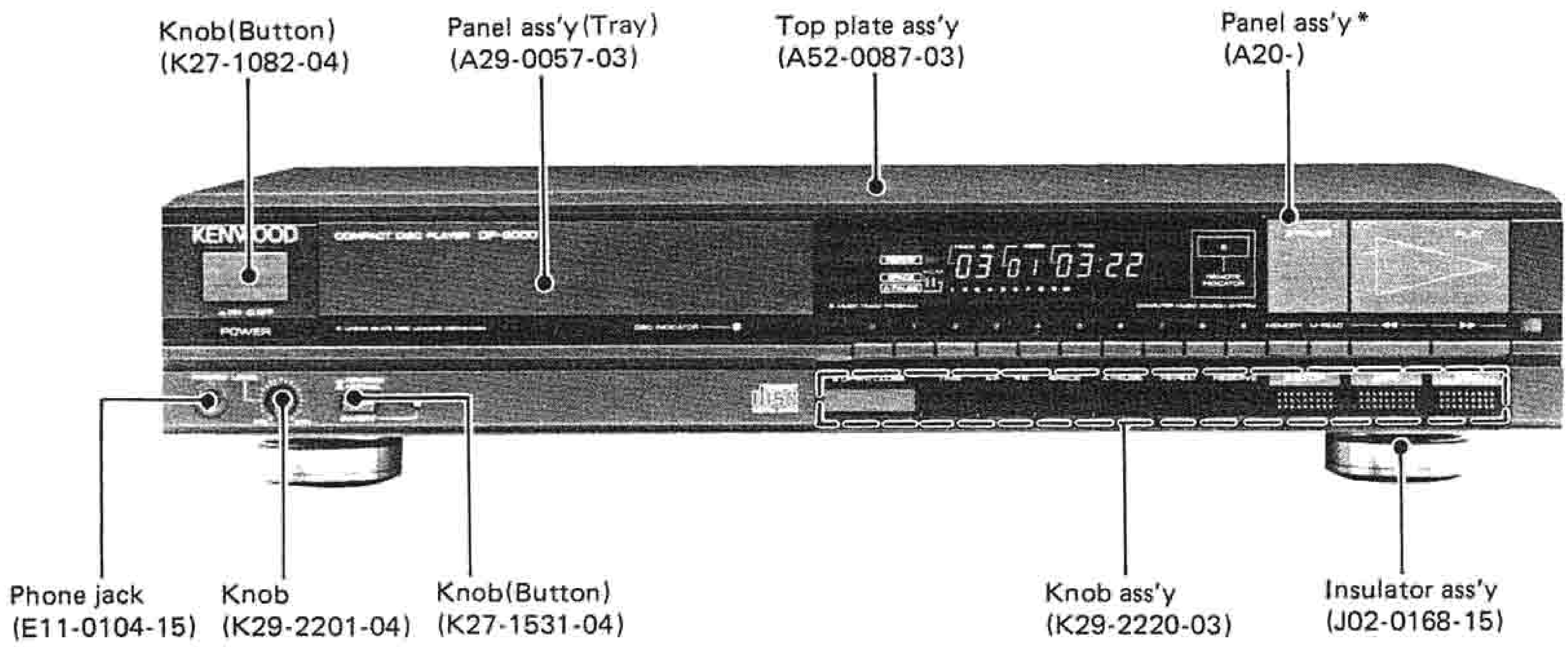
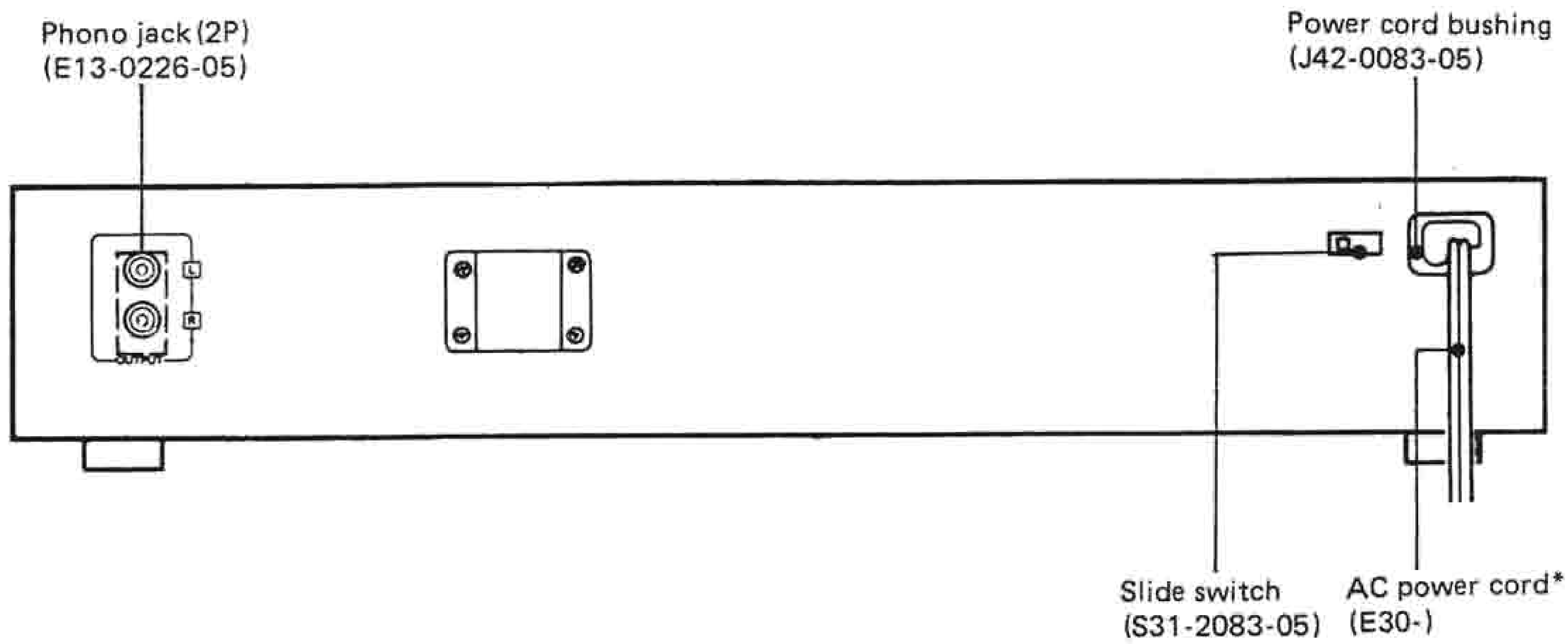
SERVICE MANUAL

KENWOOD

DP-2000

COMPACT DISC PLAYER





In compliance with Federal Regulations, following are reproductions of labels on, or inside the product relating to laser product safety.

TRIO-KENWOOD Corp. certifies this equipment conforms to DHHS Regulations No. 21 CFR 1040. 10, Chapter 1, Subchapter J.

DANGER : Laser radiation when open and interlock defeated.
AVOID DIRECT EXPOSURE TO BEAM.

***Refer to parts list on page 82.**

CONTENS

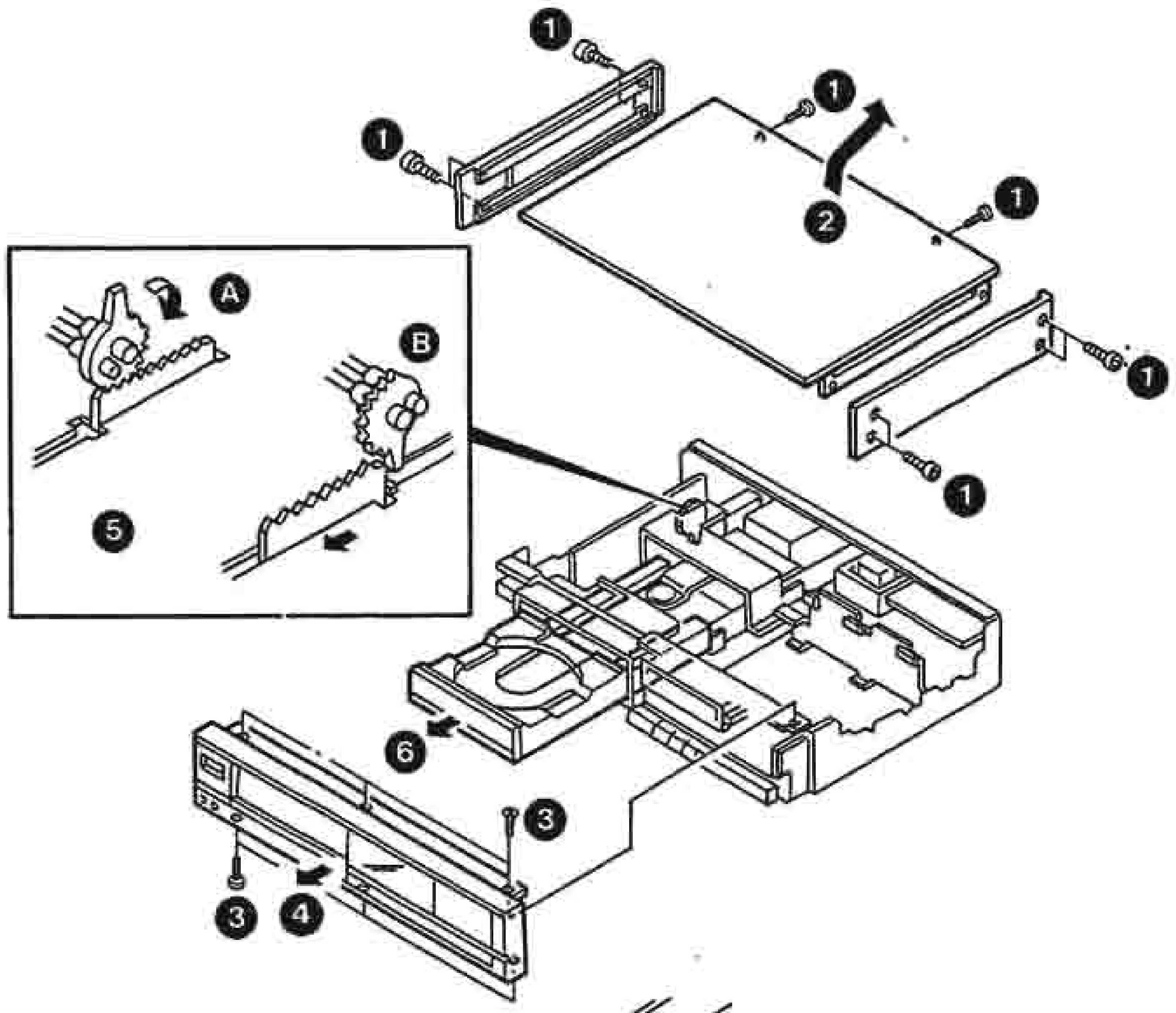
CONTENS

DISASSEMBLY FOR REPAIR

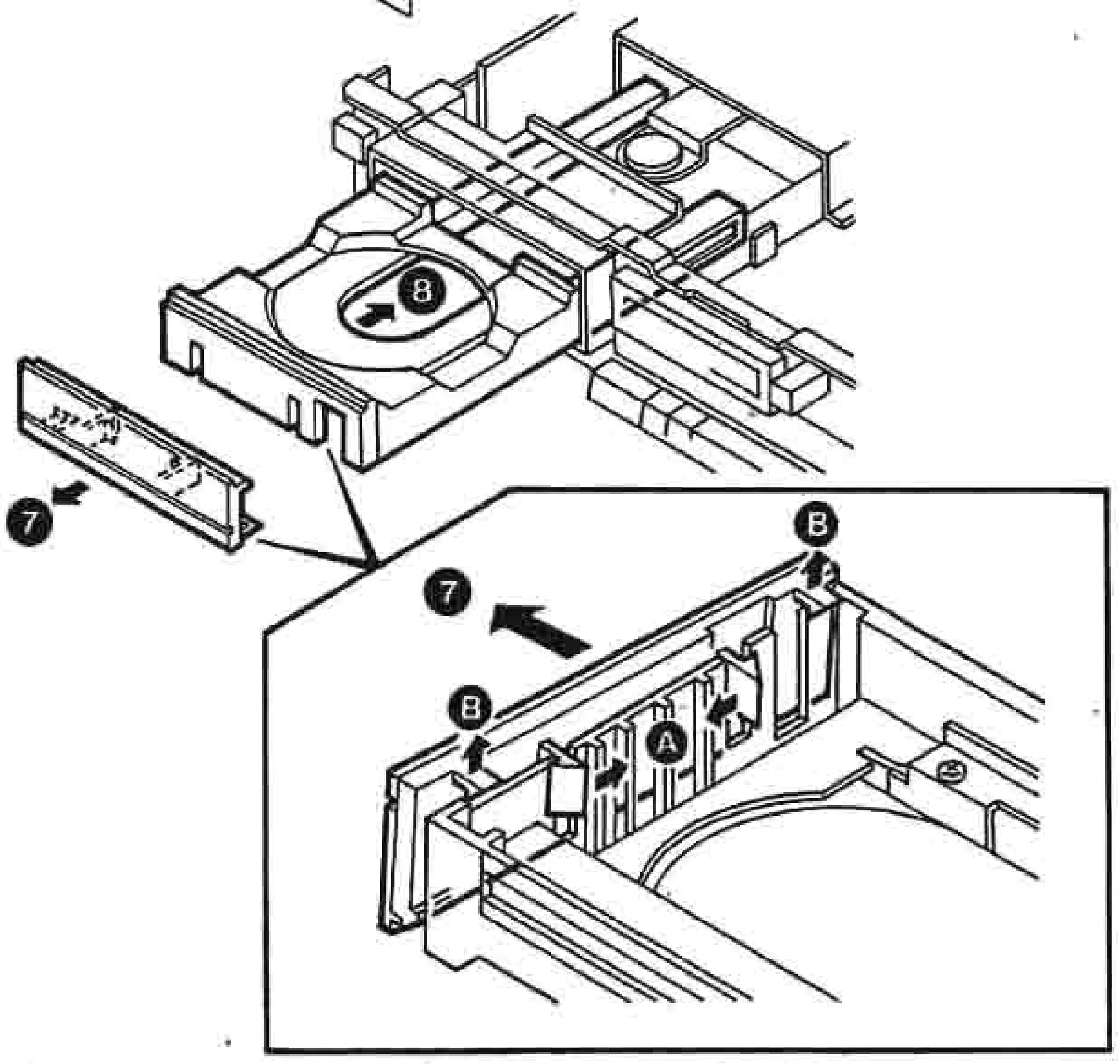
MECHANISM DISASSEMBLY PROCEDURE

Note : The AC cord must be pulled off before starting the following procedure.

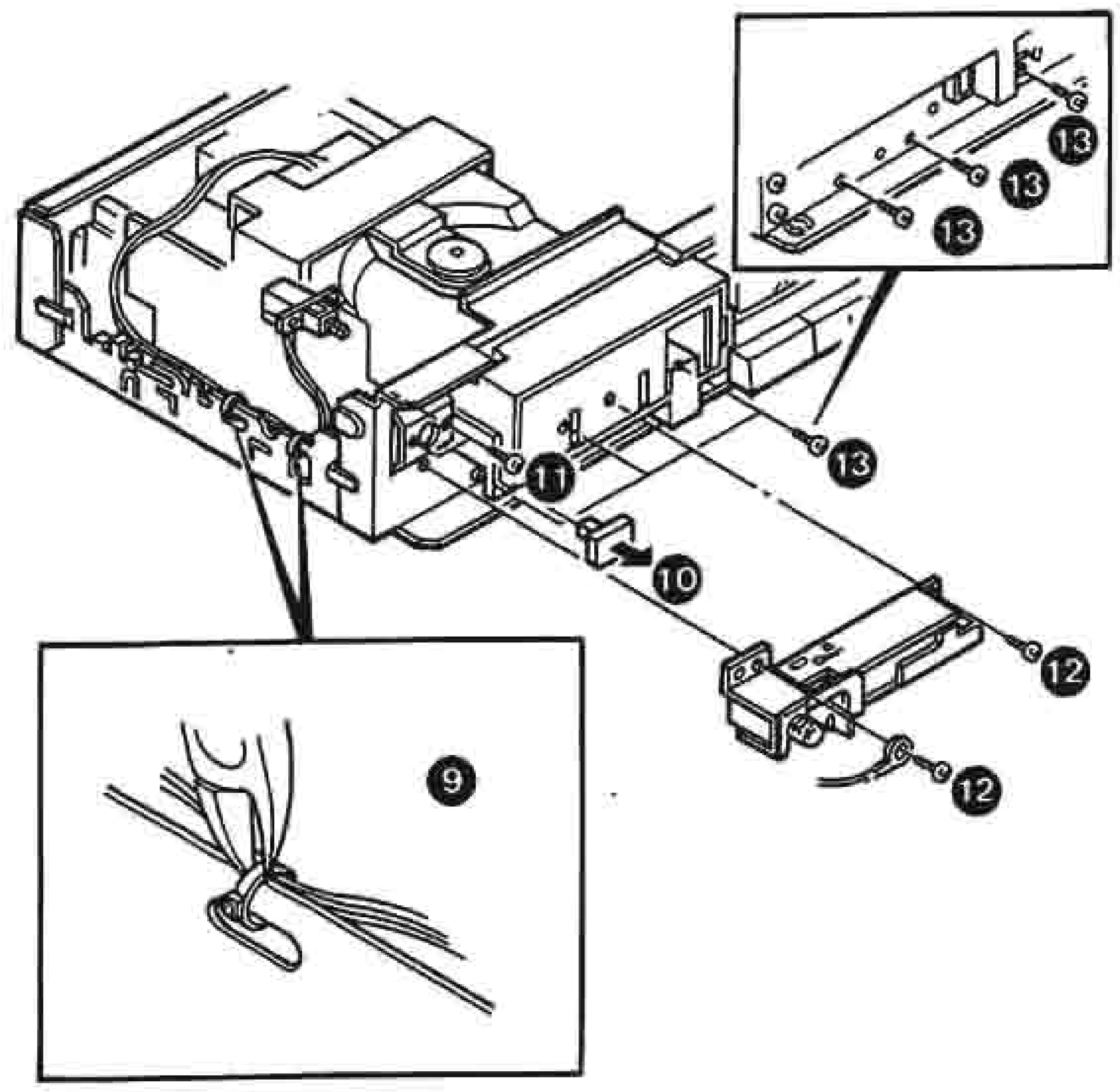
1. Remove the case (1 , 2).
2. Remove the six set screws at the top and bottom of the front panel (3). (The top three screws are flat pan-head screws.)
3. Slowing remove the panel toward you (4).
4. Turn the stem of the gear located at the rear left as indicated (toward A until it stops at the bottom (see B). This drives the tray toward you (5).
5. Slowly pull the tray out toward you (6).



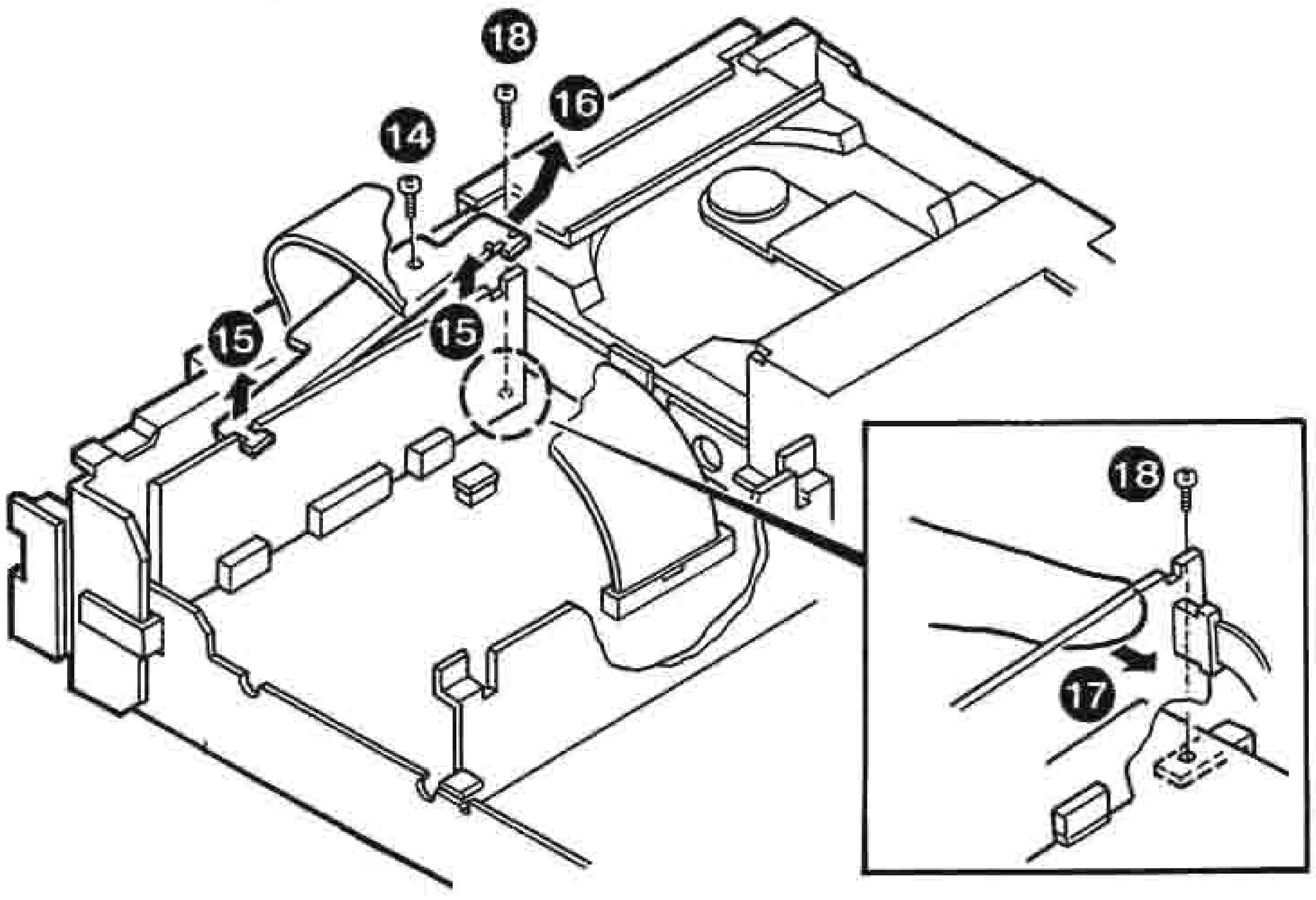
6. Push in the tray panel clamping hooks as indicated by A and B to remove tray panel (7).
7. After removing the tray panel, slowly push back the tray into the set (8).



8. Cut the wire clamper, loosen the two set screws of the power switch knob, and then remove the power switch from the chassis (9 , 10 , 11).
9. Remove the headphone board from the front bottom of the tray (12 , 13).

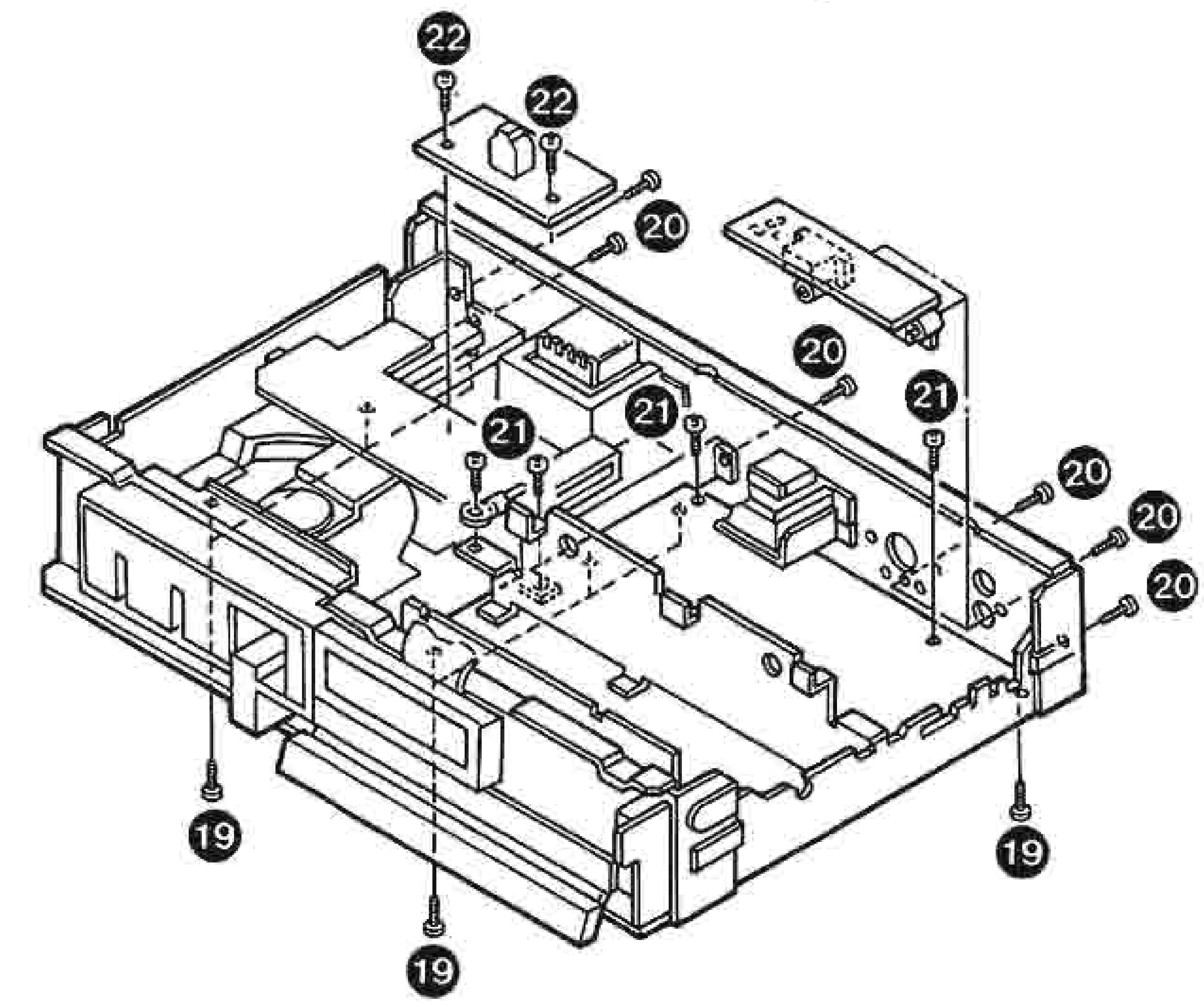


10. Remove the printed circuit board (PCB) holding plate set screw (14).
11. Remove the PCB holding plate as arrowed (15 , 16).
12. Push the PCB edge with your finger as arrowed to remove the screw from the bottom of the PCB (17 , 18).

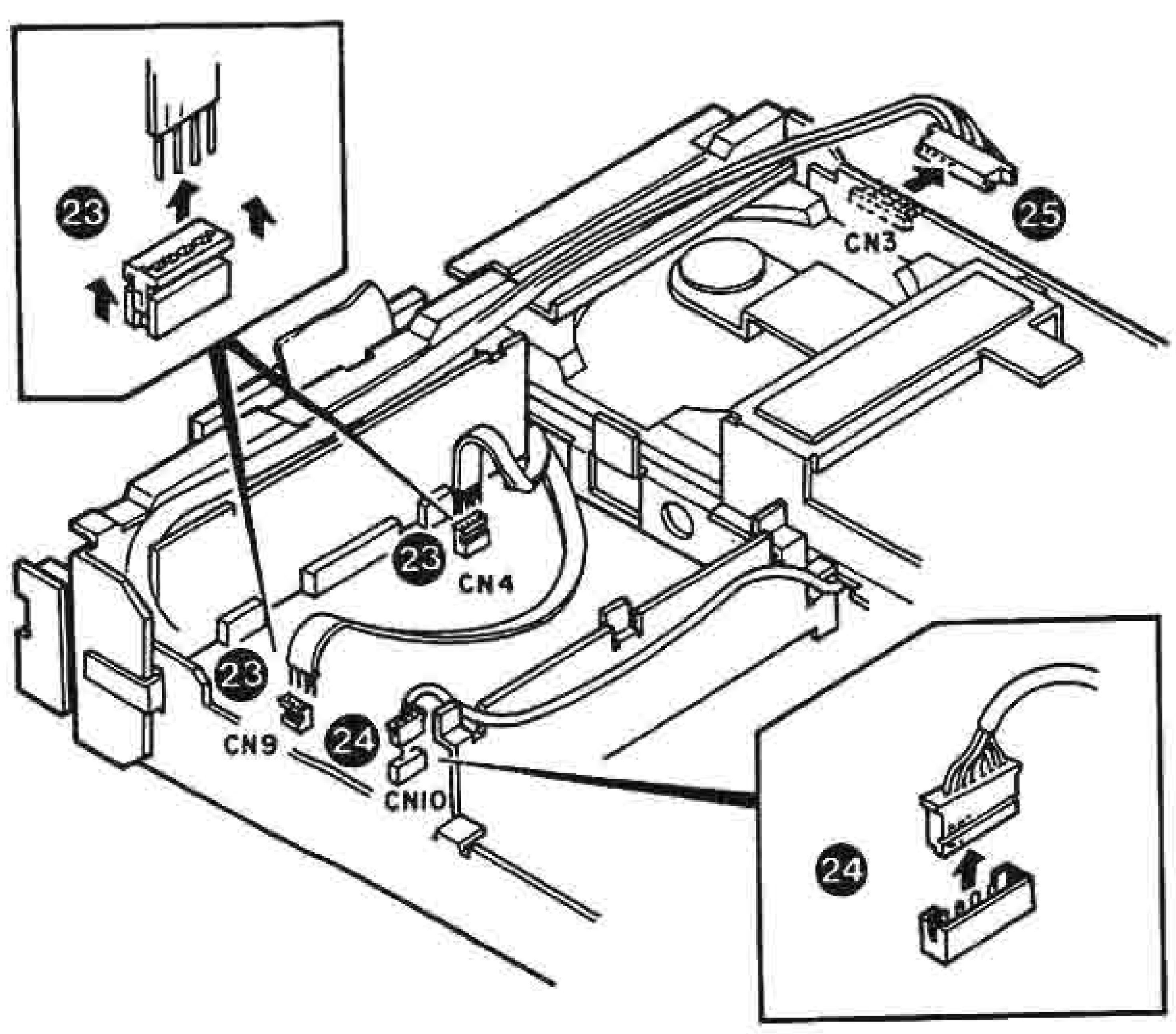


DISASSEMBLY FOR REPAIR

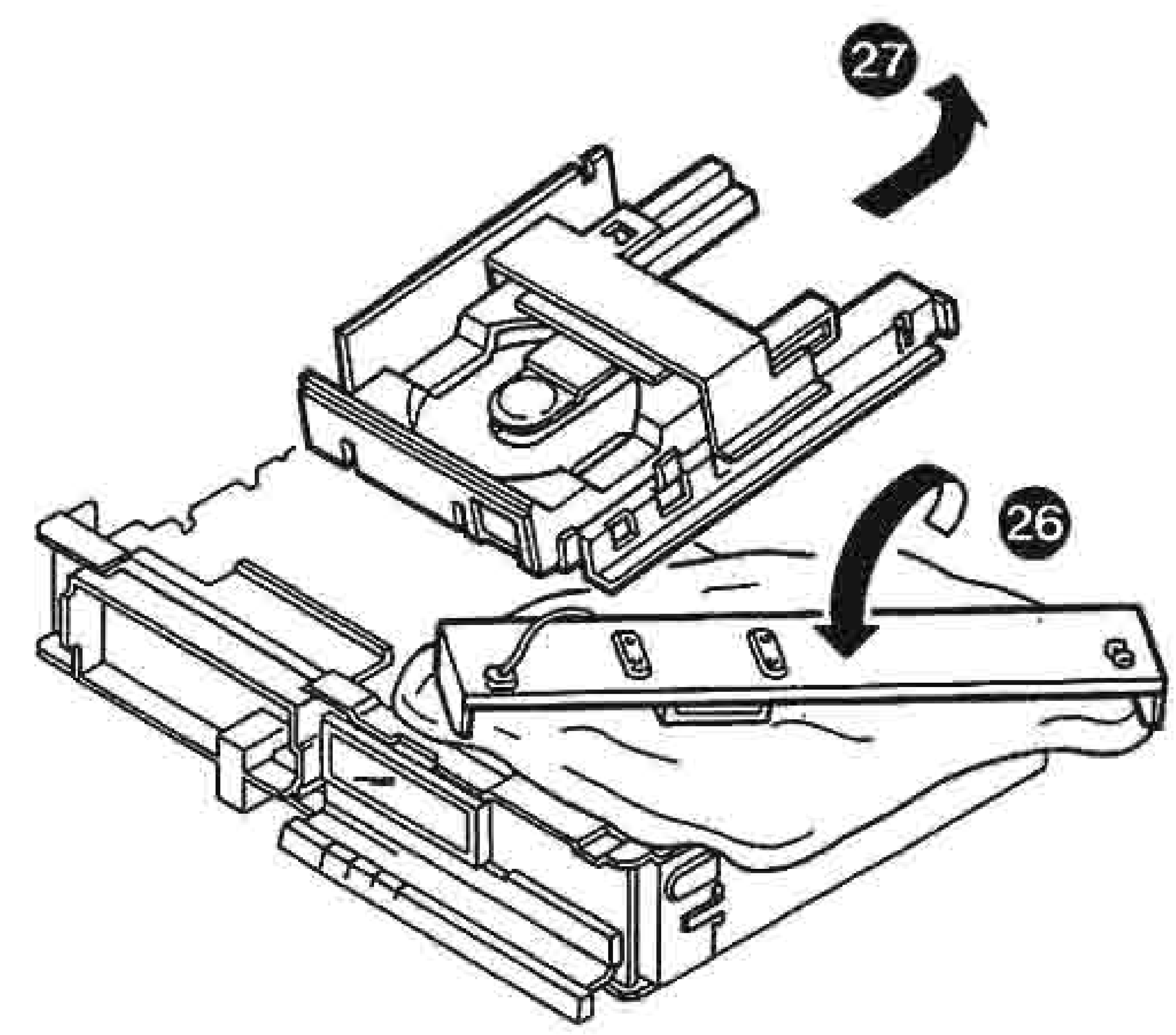
10. Remove the mechanism set screws, some of the back-panel and circuit board set screws (19 , 20 , 21 , 22).



11. Remove the cable connectors and wrapping, which connect the mechanism to other circuit boards, as illustrated (23 , 24 , 25).



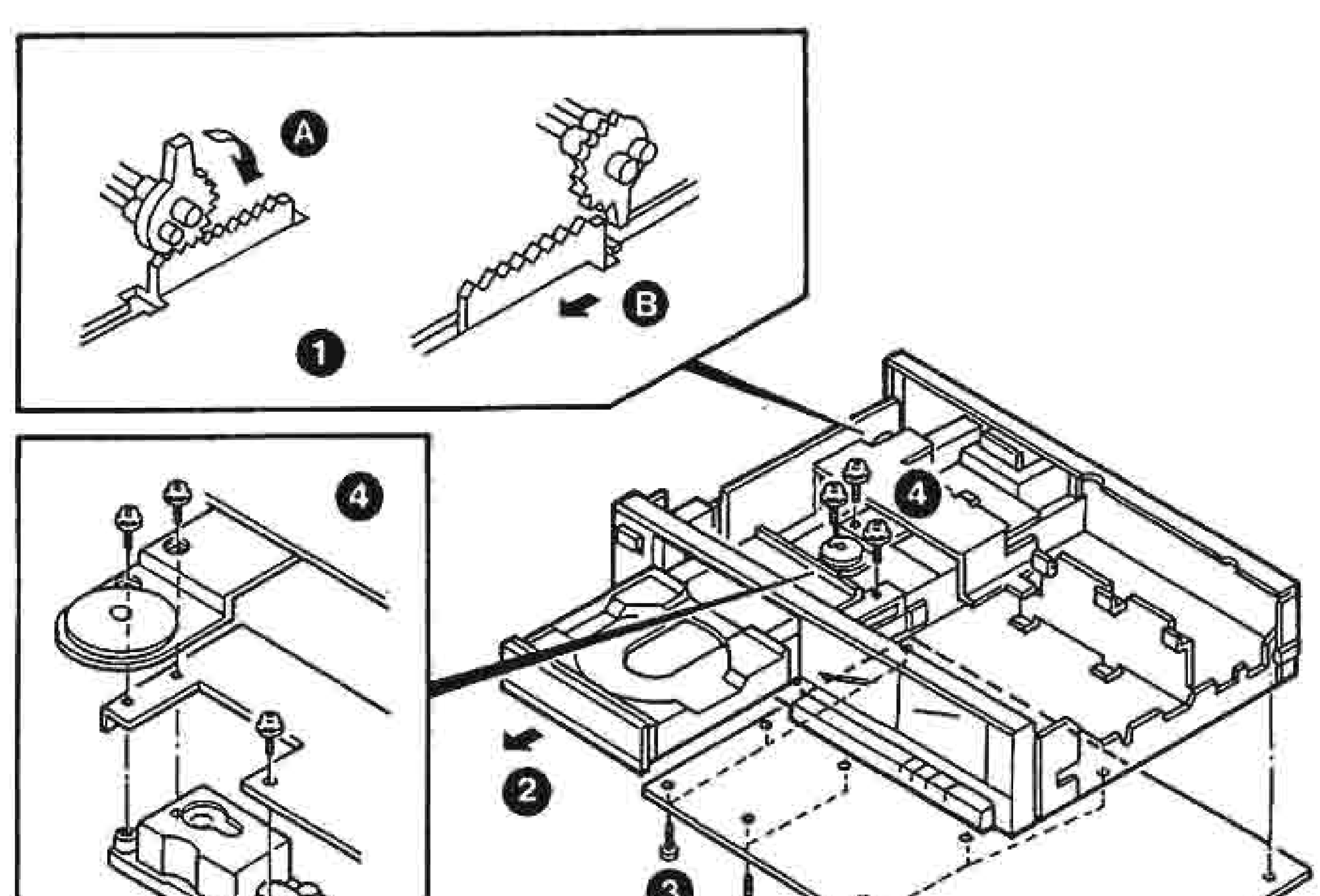
12. Cover the set with a piece of cloth and put the back paenl on it (26).
Then, slowly pull the mechanism off backward (27).



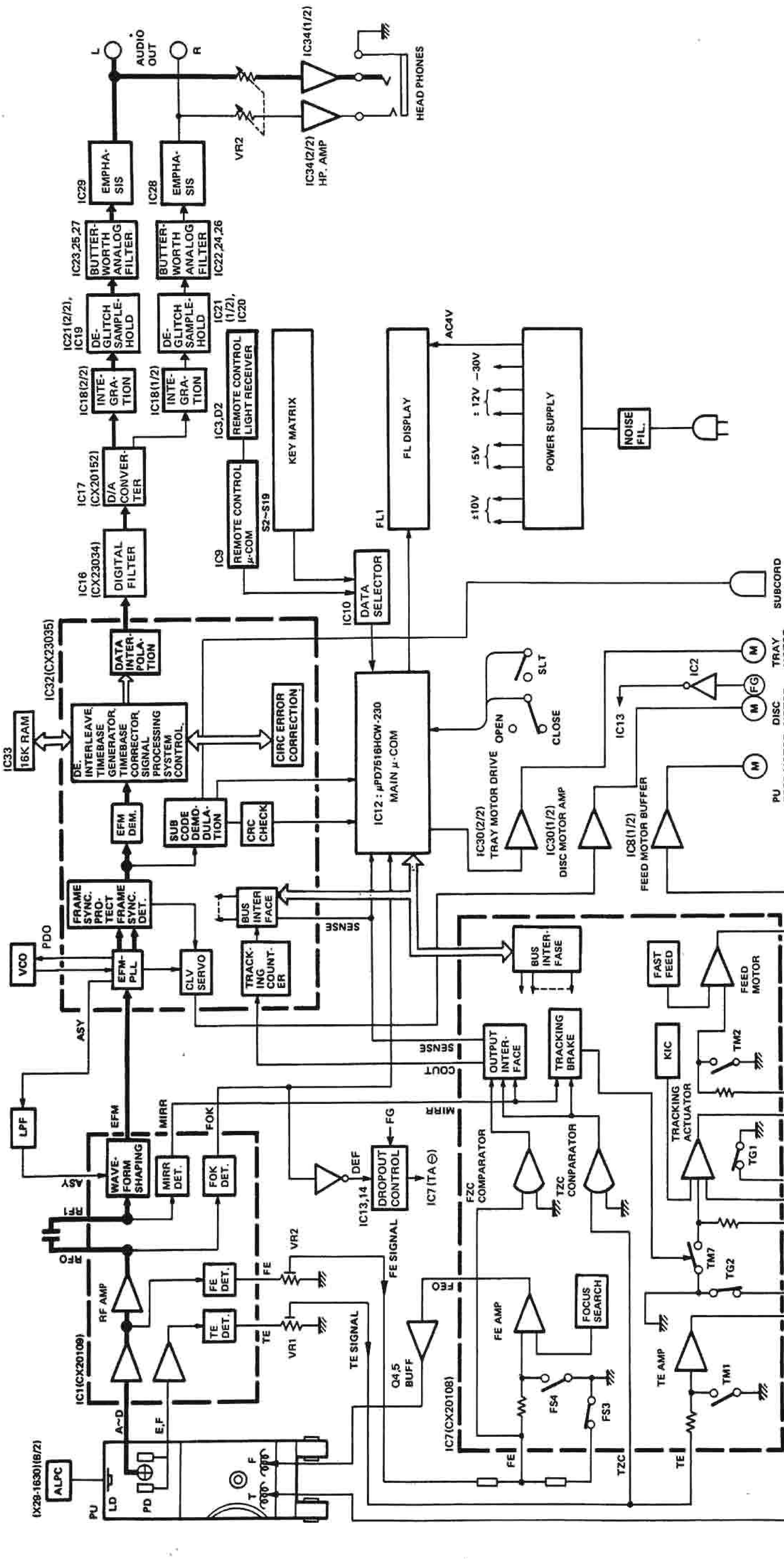
LASER PICKUP DISASSEMBLY PROCEDURE

1. Turn the rear left gear stem as indicated by A to the bottom B ; similarly to the mechanism disassembly procedure (1), and pull the tray off toward you (2).
2. Remove the bottom plate set screws (3).
3. Remove the three screws setting the laser pickup to the mechanism (4).

Note : The laser pickup should not be removed unless it is determined to be malfunctions.
When mounting a new laser pickup, all possible anti-electrostatic measures should be taken (against the work desk, human body, and soldering iron, etc.). The laser diode short pin should be remained attached until immediately before the set is operated as far as possible. A failure to observe any of these precautions may shorted the laser diode life, resulting in a malfunction of the set in a shorter period.



BLOCK DIAGRAM



CIRCUIT DESCRIPTION

1. Description of components

1–1. CONTROL (X29-1632-71)

Component	Application/function	Operation/condition/compatibility
IC1	3-beam optical pickup preamplifier	Generates a focus error and a tracking error signals; generates, and compensates the phase of an RF signal; and provides an automatic symmetrical correction circuit.
IC2	C-MOS inverter	Amplifies the output of the mechanism photo-interreflector to generate an FG signal.
IC3	Remote control preamplifier	Amplifies and converts the signal from the infrared photodiode to a digital signal whose voltage is 0 or 5V.
Q1	IC1 FOK output current buffer	Used as an emitter-follower to amplify the FOK signal current.
Q2	Disc defect detector	Comes on when the tracking error voltage exceeds + 3.0V.
Q3	Disc defect detection signal disabling during search	Comes on when the TEP signal is activated to disable the DEF signal.
Q4	FL driver	Used as an emitter-follower circuit and supplements the microprocessor output port current.
Q5	FOKF current buffer	Serves as an FOK current buffer.
D1	Remote control ray reception indicator LED	Comes on when the remote control circuit receives a signal.
D2	Remote control ray reception photodiode	Remote control PIN diode; may be replaced by PH302B.

Table 1–1

1–2. PROCESSOR (X32-1040-00)

Component	Application/function	Operation/condition/compatibility
IC1	3-terminal voltage regulator	Generates the –5V supply for the digital and servo systems.
IC2	3-terminal voltage regulator	Generates the + 5V supply for the digital and servo systems.
IC3	3-terminal voltage regulator	Generates the + 12V supply for the D/A converter system.
IC4	3-terminal voltage regulator	Generates the –12V supply for the D/A converter system.
IC5	3-terminal voltage regulator	Generates the + 5V supply for the D/A converter system.
IC6	3-terminal voltage regulator	Generates the –5V supply for the D/A converter system.
IC7	Servo control	Generates the pulses for the focus, tracking, and feed motor servos, as well as the search pulse.
IC8	Power operational amplifier	Tracking actuator driver (2/2) and feed motor dirver (1/2).
IC9	Remote control microprocessor	Compares the data from the remote control amplifier with the custom code of the DP-2000 CD player and, if they match, informs the main microprocessor IC12 of the data arrival and directs the data to it.
IC10	C-MOS 4-bit data selector	When IC12 pin 59 (A KEY) is "L", directs the data from the remote control microprocessor IC9 to the IC12 terminals K0 through K3. When "H", directs the scanned data from the tact switches to the same IC12 terminals.
IC11	C-MOS NAND GATE	Provides inverters (1/4, 3/4, and 4/4) and a clock selector (2/4). When IC12 pin 3 (CHNG) is "H", the clock selector directs the WFCK signal from IC32 pin 25 to IC12 pin 9 (SCK) and, when "L", directs the clock signal (SCK) from IC12 pin 9 to the CLK terminal of IC32 and IC7.
IC12	Main micorporcessor	Controls the player display and operation.
IC13	Dropout control microprocessor	Detects disc scratches or dusts and changes the amplifier gain over scratch areas through a preestimation.
IC14	C-MOS NOR GATE	Latches the DEF signal.
IC15	C-MOS NAND GATE	Provides an exclusive OR function which is disabled; that is, the data from the digital filter IC16 is not inverted, when the INVCL signal is "L", and enabled; the digital filter output data is inverted, when the INVCRL signal is "H"
IC16	Digital filter	A 96th degree digital filter which doubles the sampling frequency of 44 kHz to 88kHz and sends out produced data.
IC17	D/A converter	Provides the same function as CX20017 but cannot be replaced.
IC18	Bi-FET operational amplifier	Serves as an integrator and convert the D/A converter output DC current to a voltage.
IC19	C-MOS analog switch	Sample holding circuit switch (L ch).
IC20	C-MOS analog switch	Sample holding circuit switch (R ch).
IC21	Bi-FET operational amplifier	Sample holding amplifier
IC22~IC27	Operational amplifier	An operational amplifier making up the 5th Butterworth filter.
IC28	Operational amplifier	Provides the R ch. de-emphasis circuit and cascade amplifier.
IC29	Operational amplifier	Provides the L ch. de-emphasis circuit and cascade amplifier.

Table 1–2

CIRCUIT DESCRIPTION

Component	Application/function	Operation/condition/conpatibility
IC30	Power amplifier	Serves as the disc motor driver (1/2) and the tray motor dirver (2/2).
IC31	Operational amplifier	Serves as the CLV servo amplifier (1/2) and the PLL amplifier (2/2).
IC32	Signal processor	Provides various signal processing functions including EFM demodulation, synchronizing separation, error correction, CLV servo control, and PLL control.
IC33	RAM	Compatible with CXK5816 (Sony), HB6116FP-4 (Hitachi), MP8416-20LPF (Fujitsu), or TC5517AF-2 (Toshiba).
IC34	Operational amplifier	Headphone amplifier.
IC35	Reset IC	Holds the output (pin 3) at "L" until the input voltage (pin 1) reaches 4.4± 0.2V to effectively reset the set. The 3.3μF capacitor C7 determines the reset time.
Q1	Constant-voltage supply circuit	Supplies a –9V constant voltage to the pickup ALPC unit.
Q2	Switch	Turns on/off the pickup laser. The laser is ON when LDC is "H" and OFF when "L".
Q3	Switch	Enables/disables the relay muting feature with the FOKF signal; the player PLAYs when FOKF is "H" is muted when "L".
Q4,Q5	Focus driver	Focus servo amplifier (IC7) output current buffer.
Q6,Q7	Switch	The switched signal DCON is level-shifted by Q9 and switches the tracking gain and the phase compensation factor.
Q8	Remote control ray reception indicator LED mislighting prevention	Prevents the LED from being turned on at power ON/OFF.
Q9	Level shifter	Used in combination with the switch consisting of Q6 and Q7 and shifts the level of the Dropout control microprocessor output signal DCON from "H" to –10V or from "L" to +5V.
Q10	Relay driver	Energizes the relay that enables emphasis. Emphasis is enabled when the input level is "H" and disabled when "L".
Q11	Switch	When the IC32 terminal MON is "L", pulls the ASY terminal of the automatic symmetrization circuit down to –12V to disable the circuit. When the MON terminal is "H", this transistor has no effect.
Q12	Inverter level shifter	Inverts and shifts the level of the IC32 terminal MON output from "L" to –10V or from "H" to +5V.
Q13	Switch	When the IC32 terminal MON is "L", zeroes the offset of IC30 to prevent the disc motor from revolving due to the offset. When the MON terminal is "H", the output is open.
Q14	Constant current FET	Used in combination with D30 to provide the reference potential for the current into the D/A converter terminal ISET. The drain voltage is approximately 7.5V.
Q15	Constant current FET	Used in combination with D31 to provide the reference potential for the current into the D/A converter terminal ISET. The drain voltage is approximately 2.5V.
Q16	Constant current FET	Determines the current into the D/A convetter terminal ISET.
Q17~Q18	Discharger FET	Switch that discharges the I-V conversion capacitor of the D/A converter output circuit.
Q19	Relay dirver	Muting relay driver.
Q20	Constant current FET	Determines the bias current for the D/A converter.
D1,D2	Rectifier	
D3	Rectifier	
D4	FL heater bias zener diode	Determines the FL heater potential.
D6	Reference voltage supply zener diode	Generates the reference voltage to the –9V regulated power supply circuit for the pickup ALPC unit.
D7~D10	Level shifter zener diode	Lowers the V_{CE} of Q4 and Q5 and must have a minimum Pc of 1W.
D11~D15	Switch diodes	Used to prevent IC12 port damage by external surge.
D17~D23	Switch diodes	Prevents the –32V potential from being applied to the key scan inputs K0 through K3 to IC12.
D25	Varicap diode	Makes the VCO oscillation frequency variable.
D26~D29	Electrostatic proof diodes	
D30,D31	Reference voltage supply	Generates the reference voltage for the current into the D/A converter terminal ISET
D33,D34	Switch diodes	Prevents Q10 and Q19 from being destroyed due to the counter electromotive force of the relay.
D36	2-color LED	Inverting switch LED which is lighted "green" in normal mode and "red" in inverted mode.

CIRCUIT DESCRIPTION

2. Circuit operation description

2–1. EFM Signal inputs inhibiting circuit

The DP-2000 and DP-1000 use the disc motor drive instruction signal to input the EFM signal to the signal processing IC (CX23035). The MON terminal of the CX 23035 outputs a signal which disables the disc motor when it is "L" and drives the disc motor when it is "H".

"L" at the MON terminal turns Q3 on which turns Q3 on in turn, lowering the voltage at point a to −12V. This also pulls the ASY terminal of the CX20109 down to a negative potential, disabling the automatic symmetry circuit and fixing the EFM terminal at "H". Q3 in conduction also keeps Q5 in conduction or in the on state, forcing the disc motor driver output at 0V and thus preventing the disc motor from being turned by the offset of the driver amplifier.

When the MON terminal rises "H", Q3 through Q5 are turned off, enabling the automatic symmetry circuit which supplies the EFM signal to the CX23035. The potential at point a rises up to approximately + 2.5V to allow the disc motor driver to feed the drive voltage to the motor.

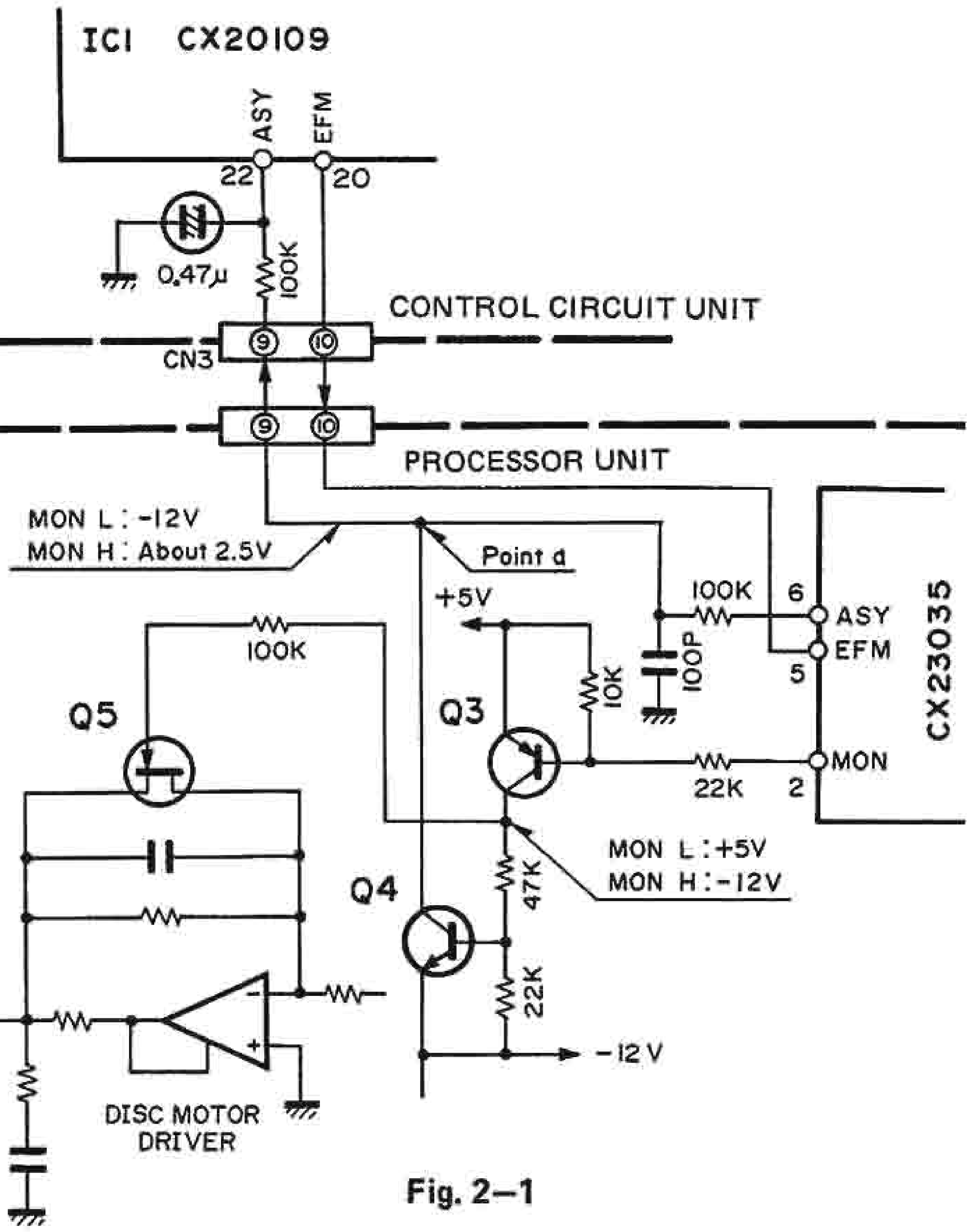


Fig. 2–1

2–2. Remote control/Key data switching circuit

To inform the main microprocessor (μPD7516HCW) that any instruction has arrived from a main frame key or the remote control microprocessor, a signal voltage rise edge must be given to its INT terminal (pin 63). When a main frame key is pressed, some of K0 through K3 rises which are fed to the INT terminal through the composite element diodes. When the remote control microprocessor receives any remote control data, it determines what the data is and raises its PSHKY terminal from "L" to "H". This change is transmitted to the INT terminal of the main microprocessor through a diode.

When a voltage rise edge (_↑‾) is received at its INT terminal, the main microprocessor check to find if the PSHKY terminal is "H". If it is, the main microprocessor determines that the instruciton is from the remote control microprocessor. Otherwise, it determines that the instruction is from a main frame key.

Through a PSHKY logic, the main microprocessor gives an instruction ("H" when the instruciton is from a main frame key or "L" otherwise) to the TC40H157P data selector via the AKEY terminal. According this instruction, the data selector properly routes the data from the main frame key or the remote control microprocessor.

Data from a main frame key is input to the main microprocessor through a key scan. When receiving data from the remote control microprocessor, the main microprocessor sends a clock signal to the remote control microprocessor which responds with a timing signal via the STB terminal. The main microprocessor strobes the data in by using the timing clock available at its STB terminal.

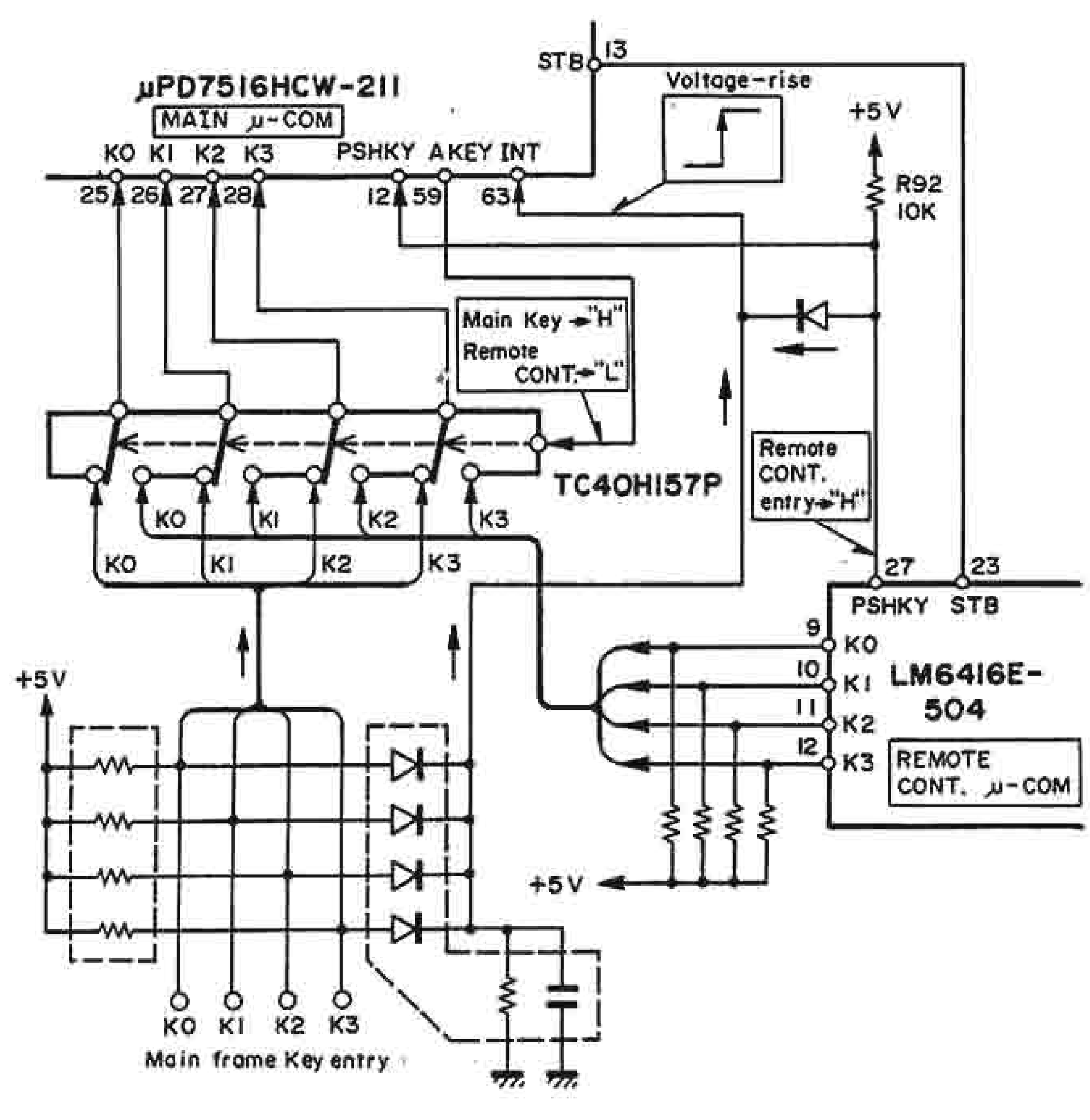


Fig. 2–2

CIRCUIT DESCRIPTION

2–3. Dropout control circuit

When the focus servo is enabled, FOK is "H". If the RF signal level falls due to flaws on the disc, etc., however, FOK momentarily falls to "L" which is fed to the DEF terminal of CN3 through an inverter.

A disc defect such as a bubble, etc. which largely swings the tracking error signal though it does not affect FOK (stays "H") turns Q2 on to supply "H" to the DEF terminal when the T.Error signal exceeds a certain level (approximately 2.9V).

A signal MIRR is used in order for holding the PLL operation, etc. due to some disc defect. During search, the RF signal is used to count the tracks crossed over.

The MIRR signal is "L" during normal play but it goes "H" when a flaw is detected. Further, the DEF signal is logically ORed to activate the MIRR signal at CN3 so that PLL is also held against such a disc defect that does not directly activate the MIRR signal.

Because the MIRR signal is used for track count during search, however, Q3 is maintained in conduction with the TEP signal which is "H" during search mode to isolate the DEF signal from the MIRR signal.

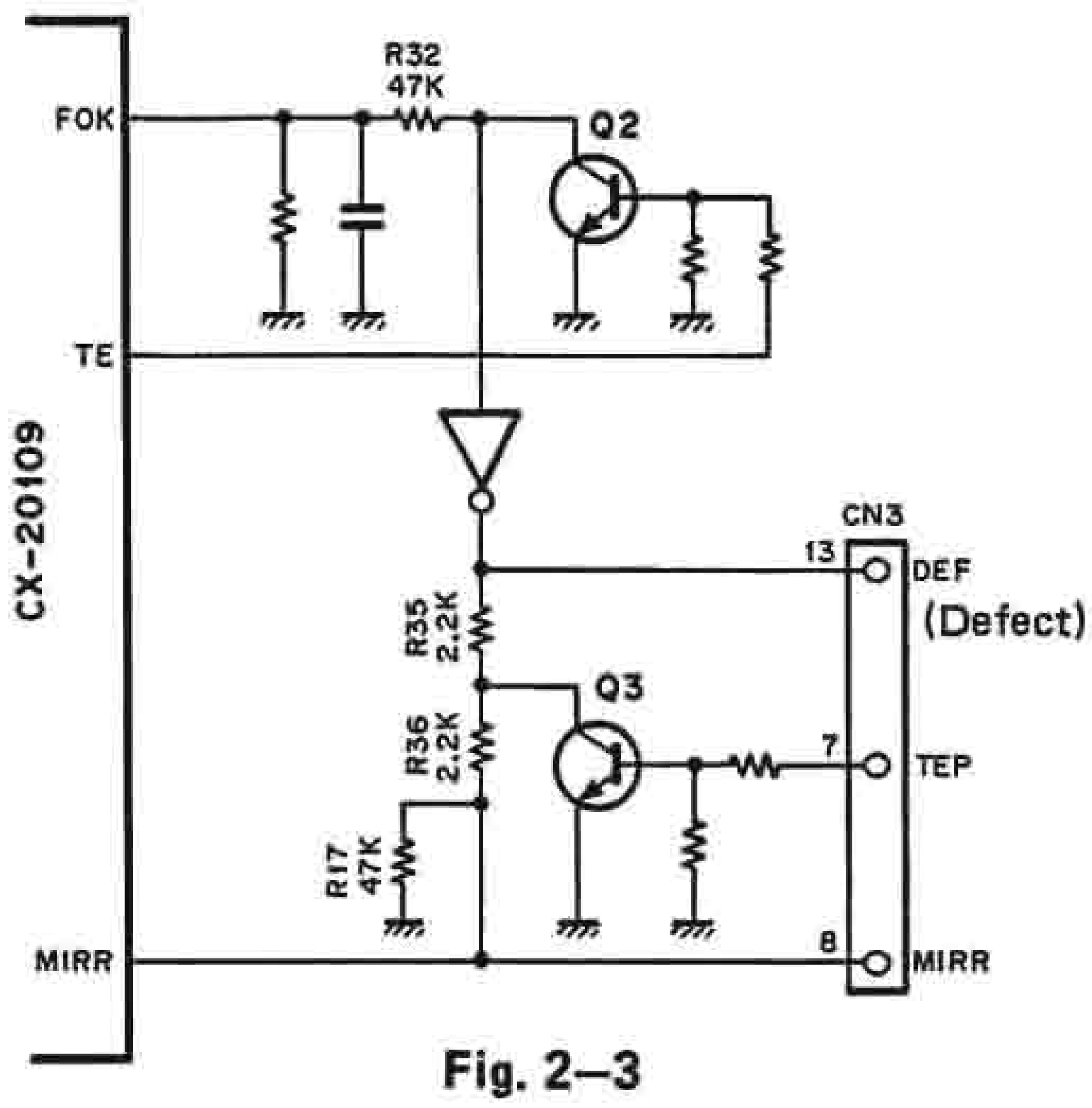
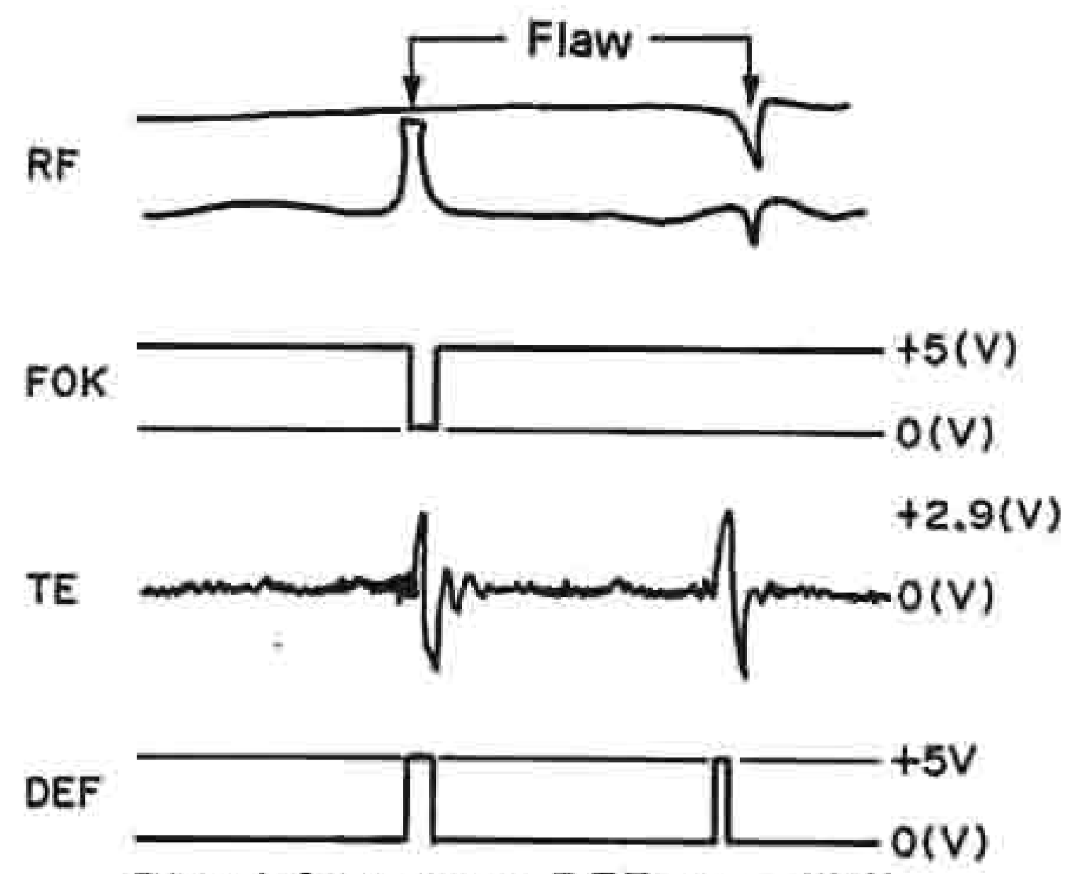


Fig. 2–3



Disc defects cause DEF to go "H".

Fig. 2–4

2–4. Digital filter (Doubled oversampling digital filter)

The CX23034 processes the data sampled at 44.1kHz (fs) through arithmetic operations to produce and interpolate a data in the sampled data which is expected to originally exist there. This effectively generates the same signal series that would have been generated through a sampling at 88.2kHz. The CX23034 operates on a 16.9344 MHz clock which is quartered down from the 67.7376MHz D/A converter (CX20152) master clock. It further halves the 16.9344MHz clock to 8.4672MHz as the signal processing master clock.

The digital filter is followed by a 5th degree butterworth analog filter which is built with discrete components and has superior phase characteristics.

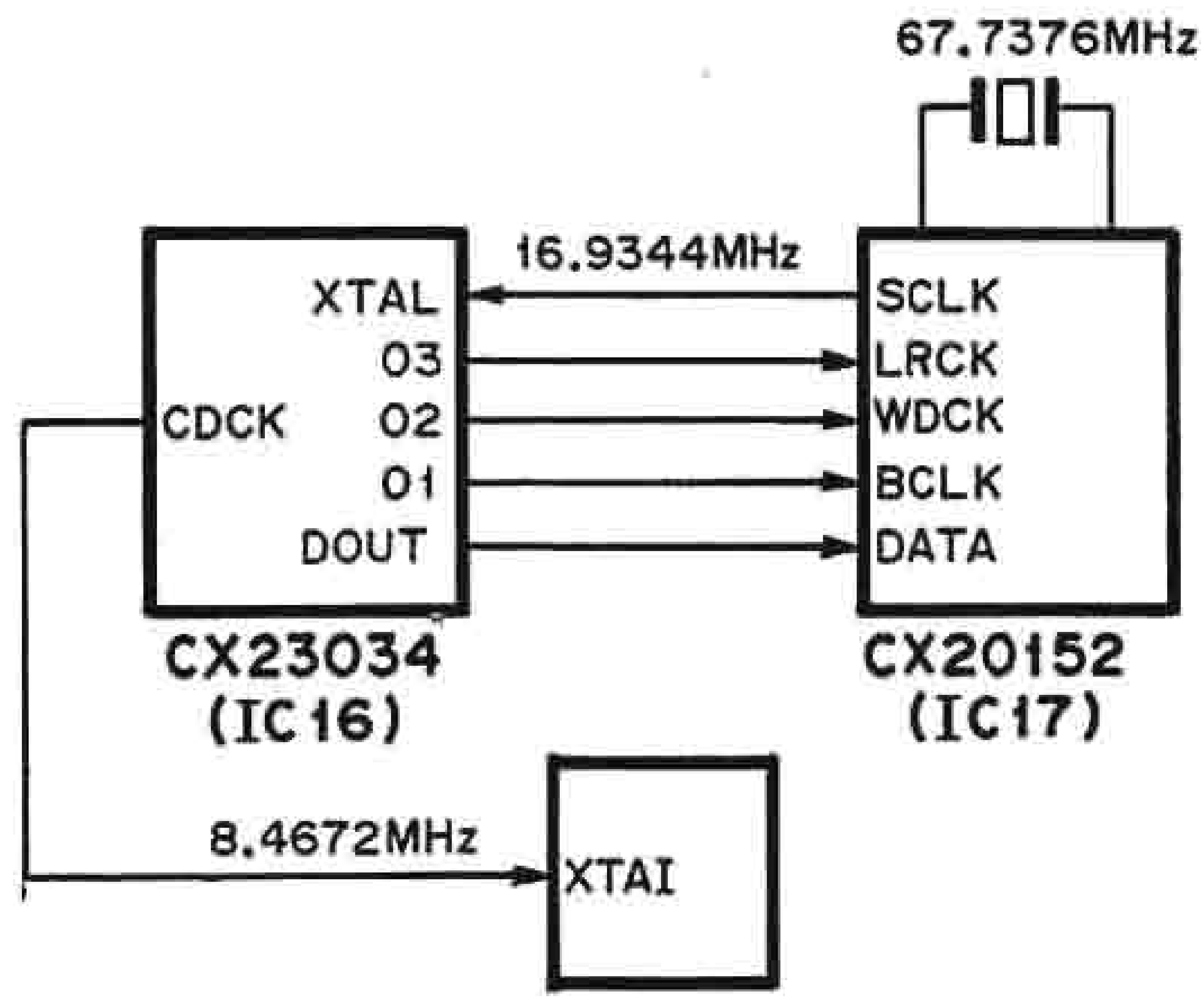


Fig. 2–5

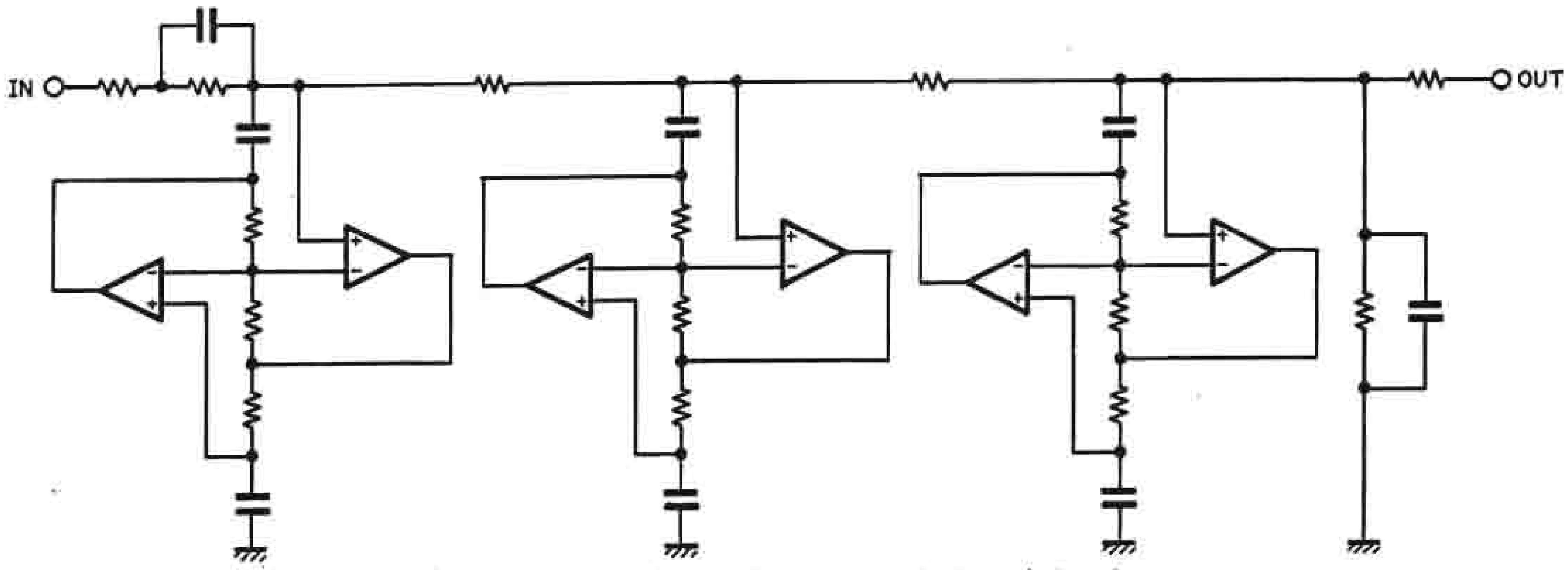


Fig. 2–6 5th degree butterworth filter circuit

2–5. Invert switch

When the Invert switch is at NORMAL, the audio signal is in the same phase as that recorded on the disc and the audio signal phase is inverted (shifted by 180°) when the switch is at REVERSE.

With the Invert switch at NORMAL, INVI is "H" which is inverted to "L" as INVICRL through the main microprocessor. This allows the digital filter (CX23034) output data to be input to the D/A converter (CX20152) as it is.

When the switch is pushed in to REVERSE, INVI goes "L" and INVICRL turns to "H", inverting the digital filter output data to the D/A converter. This effectively results in the inversion of the audio signal phase.

Pushing in the Invert switch causes the player to be muted 10ms later. This muting is removed 10ms after.

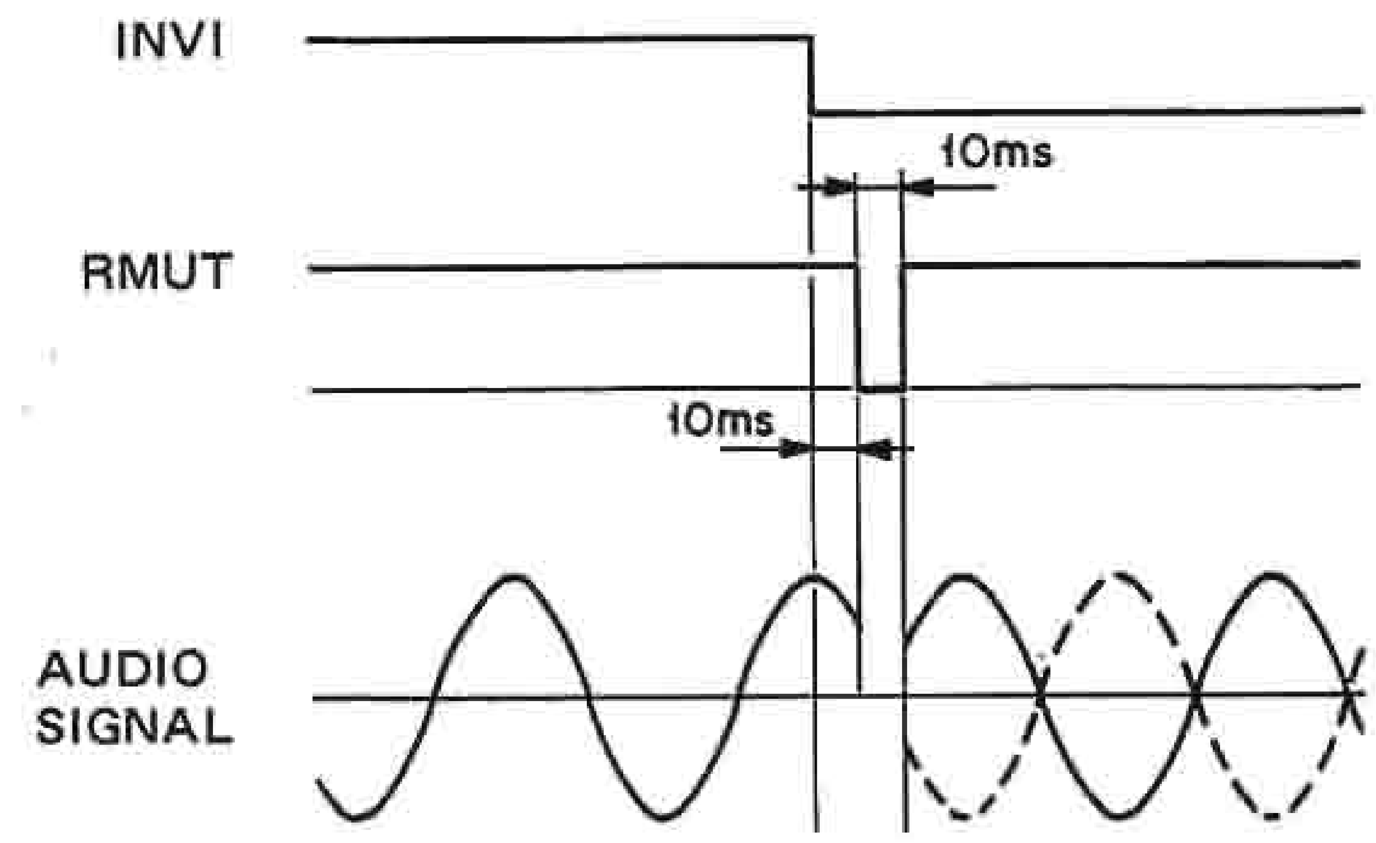


Fig. 2–7

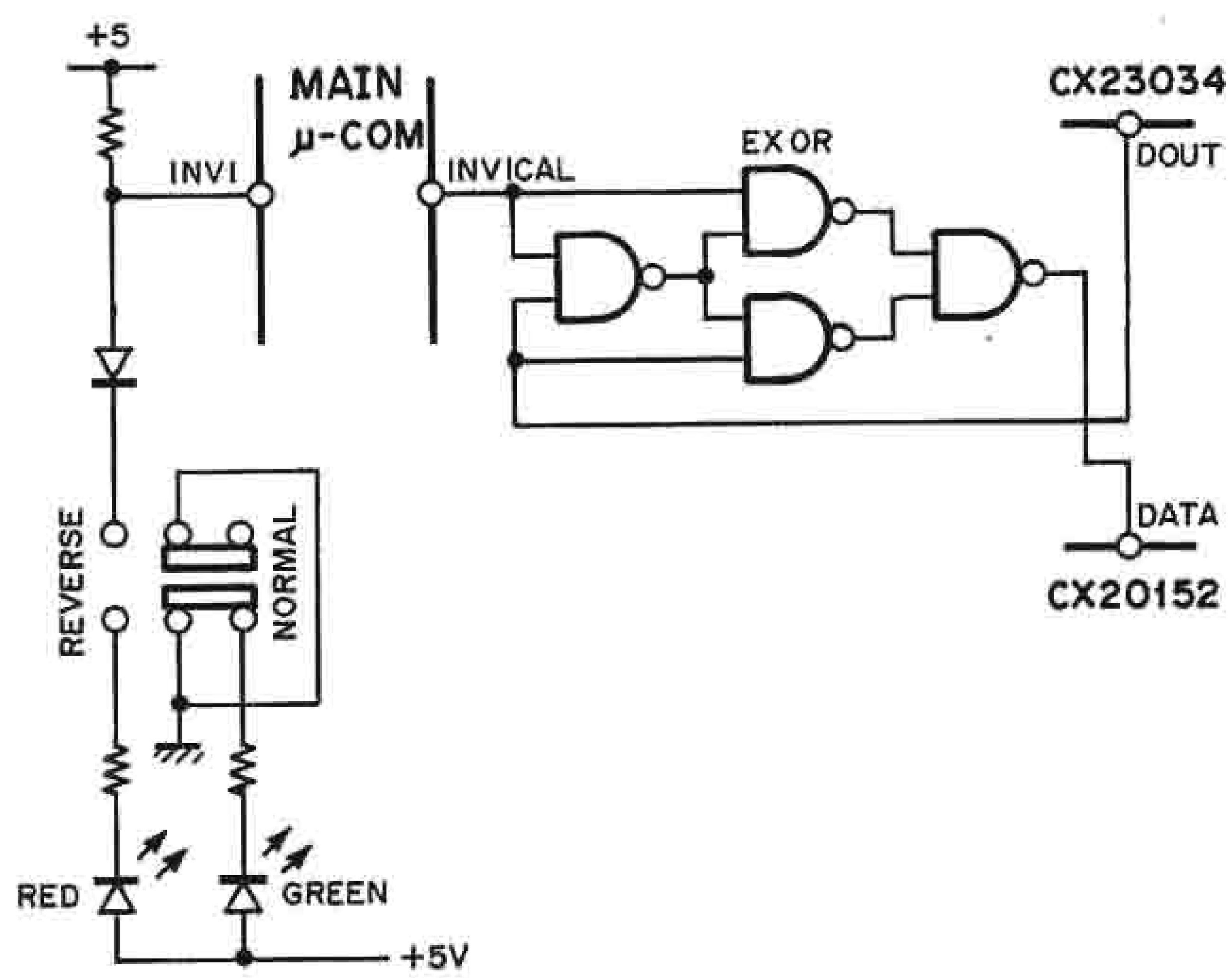


Fig. 2–8

CIRCUIT DESCRIPTION

3. Principle and operation of 3-beam laser pickup

"3-beam" means that three laser beams are used. But it does not mean that three semiconductor lasers are used. Consider it in such a manner that one laser beam is split into three by making use of the interference property of the beam, when lights is passed through narrow slit. and these beams are directed to the disc.

The pickup of this equipment employs magnetic floating system as the actuator drive system, astigmatism method as the method for focus error detection and three beam system as the method for tracking error detection.

3–1. Method for focus error detection (astigmatism method)

Such a property that the light reflected by the disc makes divergence, parallel motion and convergence against the distance from the pickup's objective lens to the disc is used. (See Fig. 3–1.)

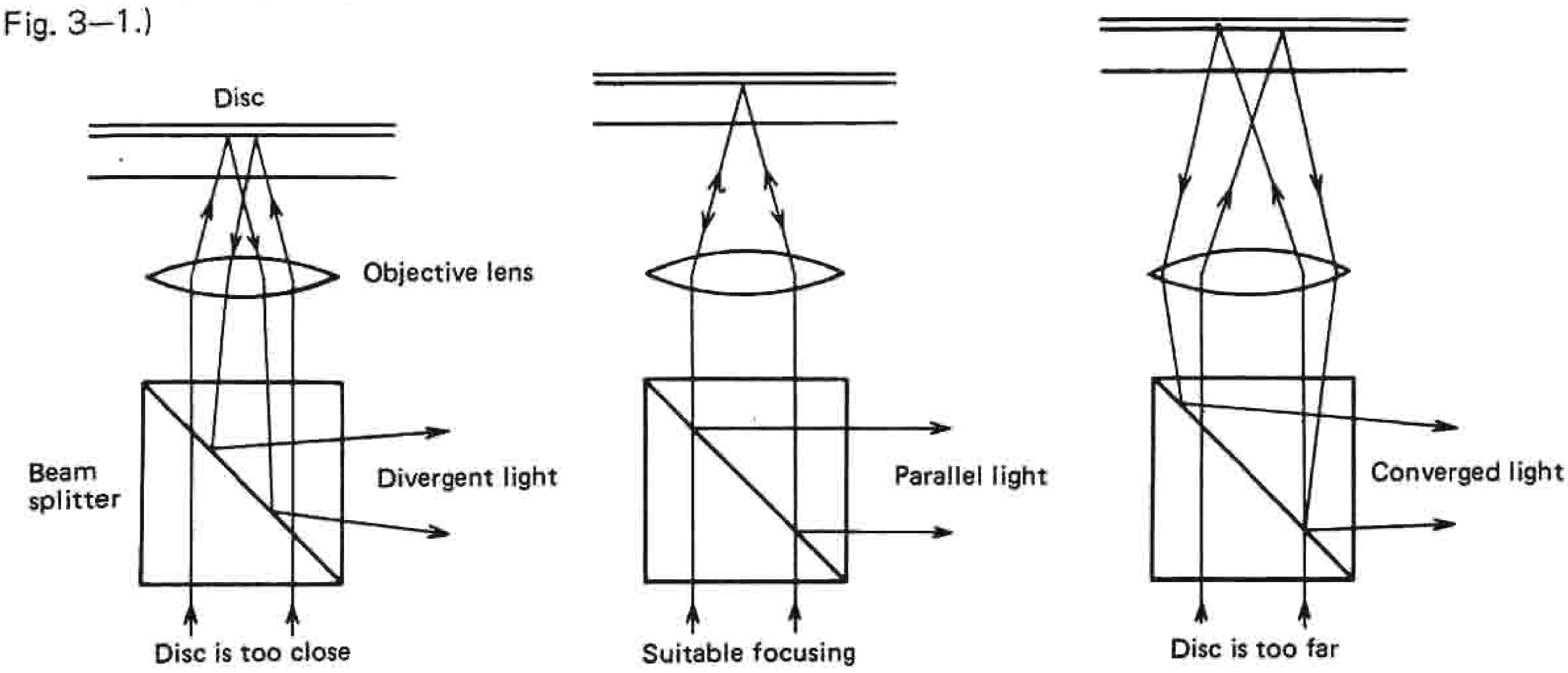


Fig. 3–1 Light reflected by disc

A focus error signal is obtained by detecting this reflected light with a lens, which is a combination of a convex lens and a cylindrical lens. (See Fig. 3–2.)

In the focus servo circuit, the difference between total of two detector signals at two diagonal points is calculated, that is, (A + C)–(B + D) is calculated, and focus servo is applied when it is always 0.

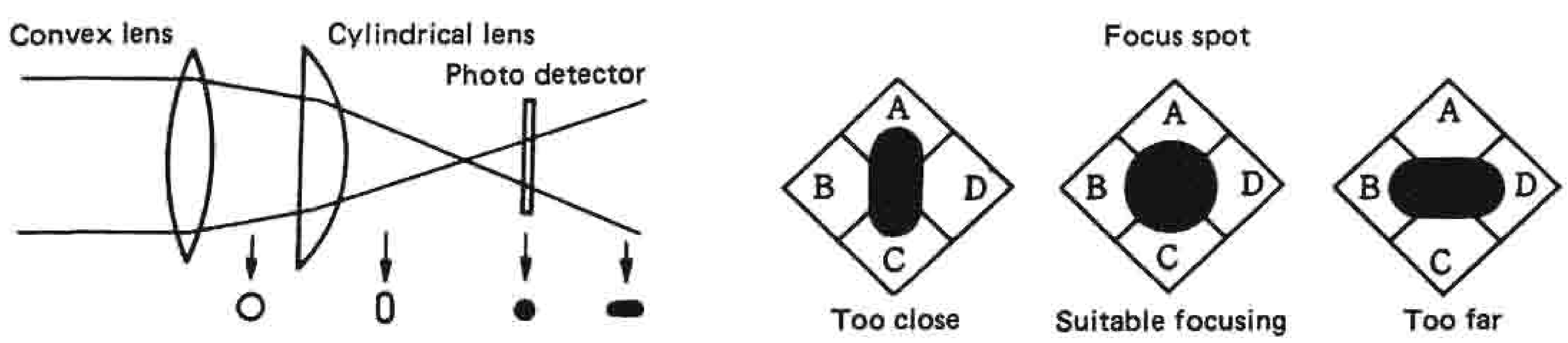
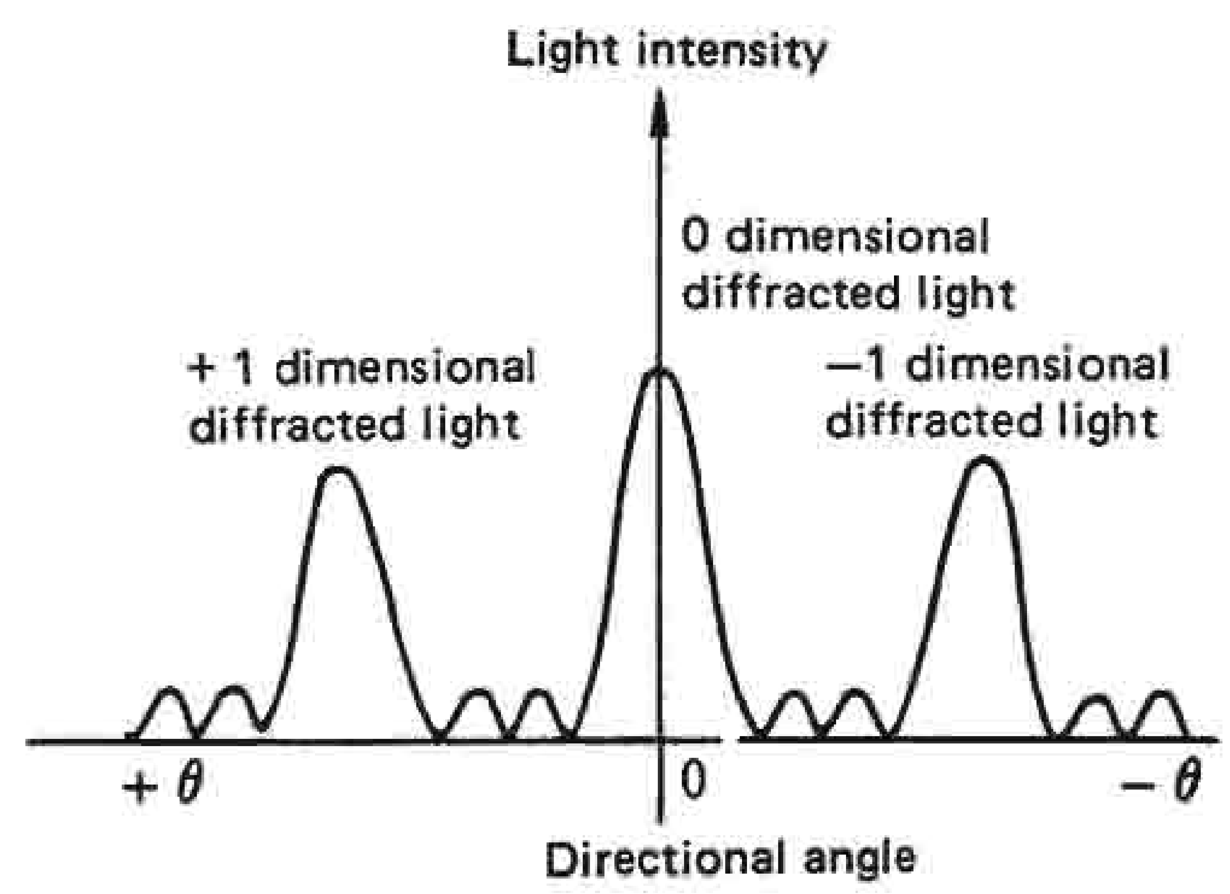


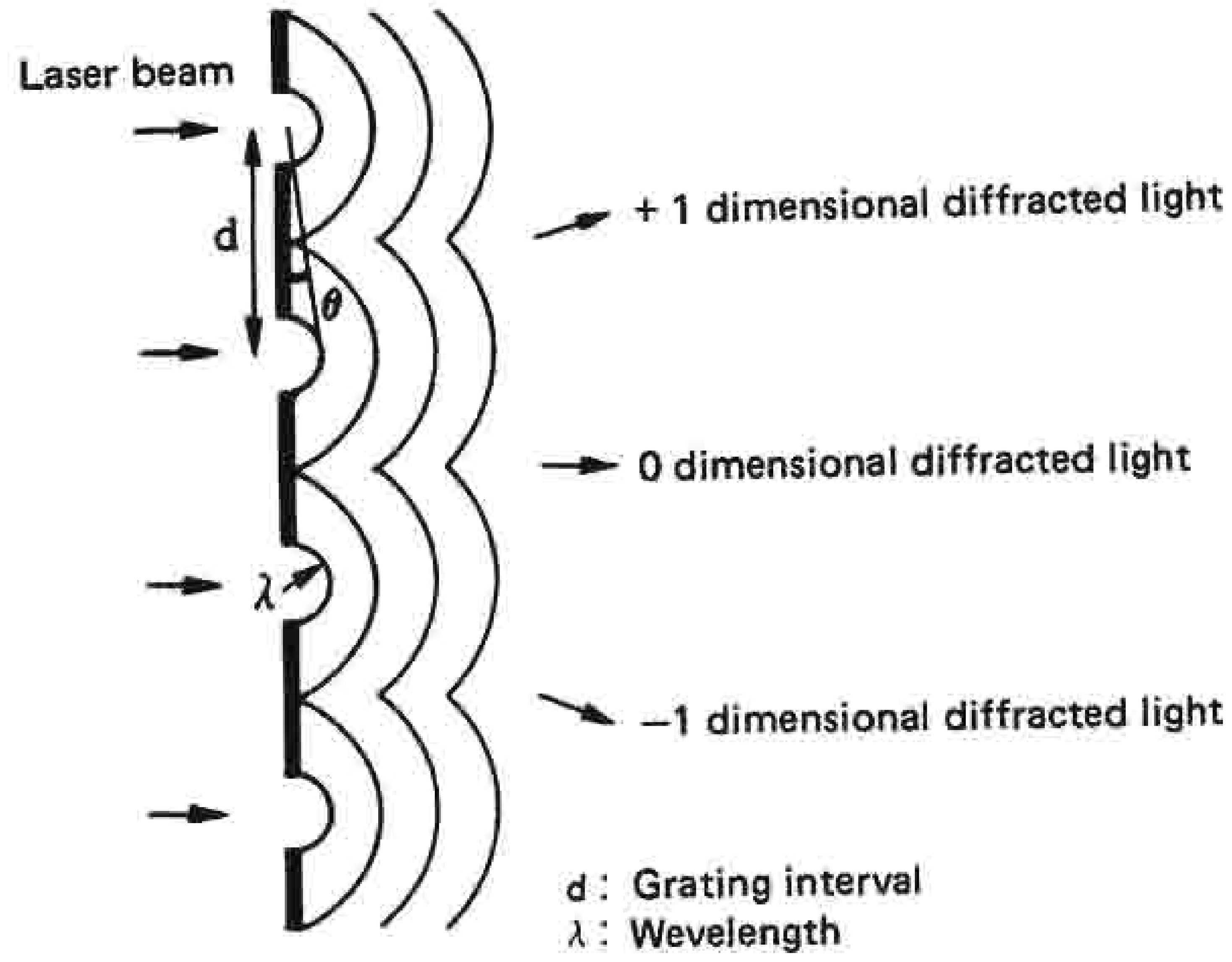
Fig. 3–2 Principle of astigmatism

CIRCUIT DESCRIPTION

3–2. Tracking error detect circuit (3-beam method)

The principle of generation of three beams is such that the laser beam generated out of a laser diode is directed to a board of slit form called diffraction grating to cause occurrence of interference, and thus the beam is split to three beams. (See Fig. 3–3.)





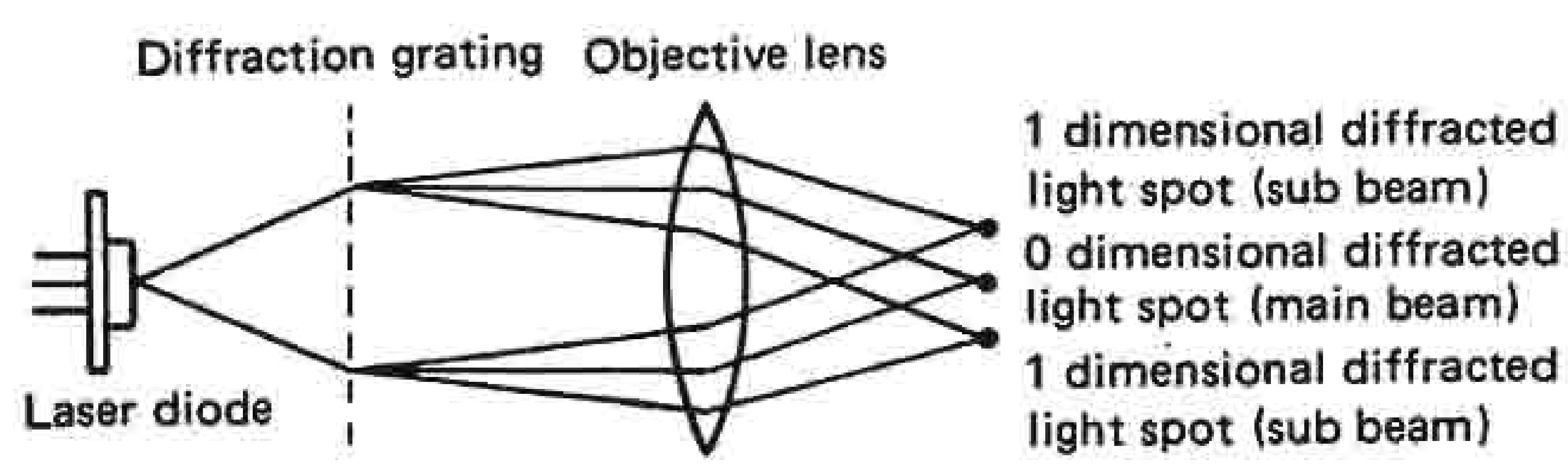


Fig. 3–3 Principle of generaiton of three beams

Tracking error detection by the 3-beam method is made as follows.

The sub beam are arranged in such a manner that they have certain offset angles to the main beam. If the main beam is deviated from the track, a difference will appear in the sub beam reflected lights, and it becomes a tracking error signal. In other words, if the differential signal between photodetectors E and F which receive sub beam reflected lights is obtained and it is always kept at 0, the main beam will always trace along the track. (See Fig. 3–4.)

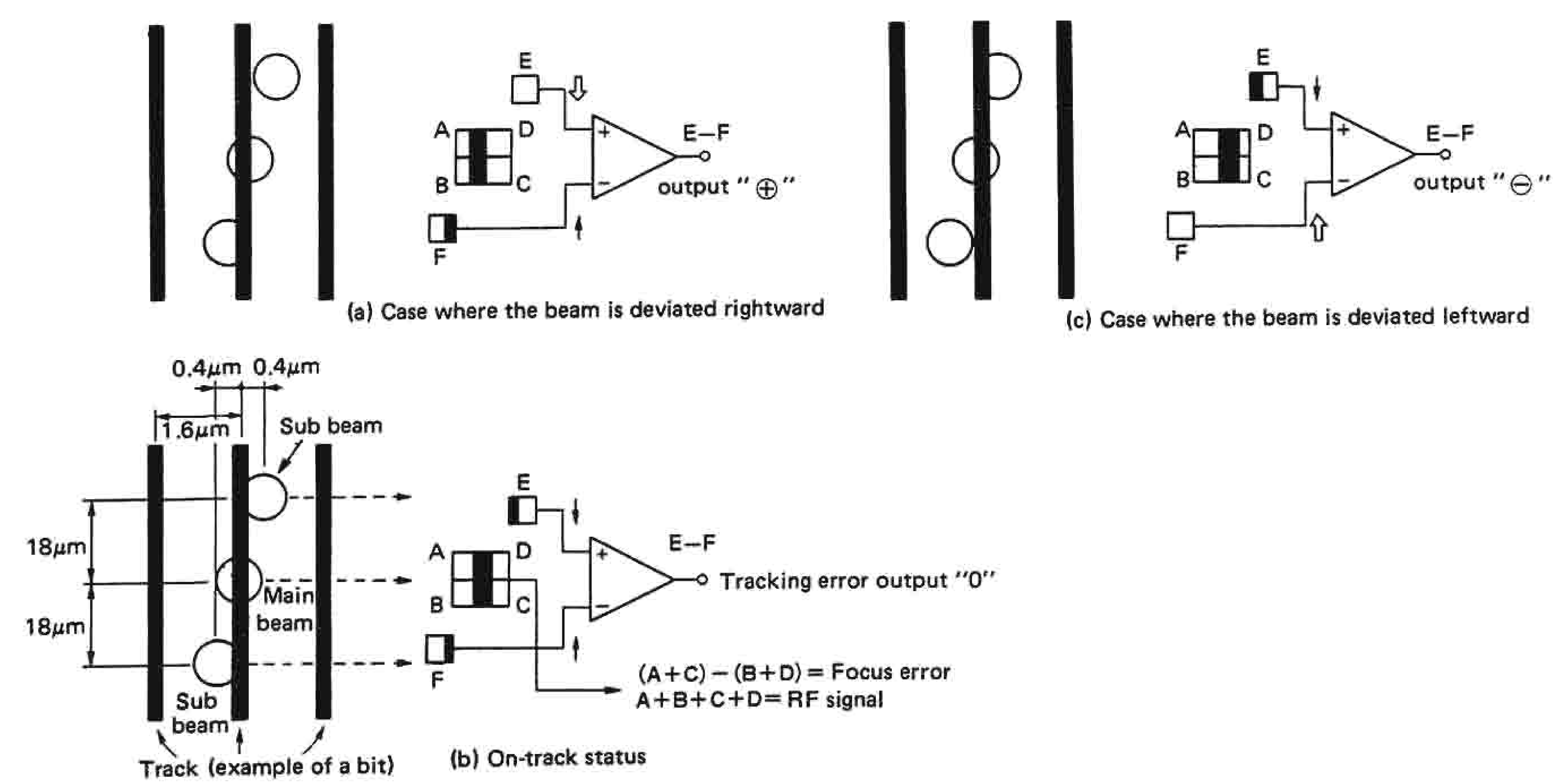
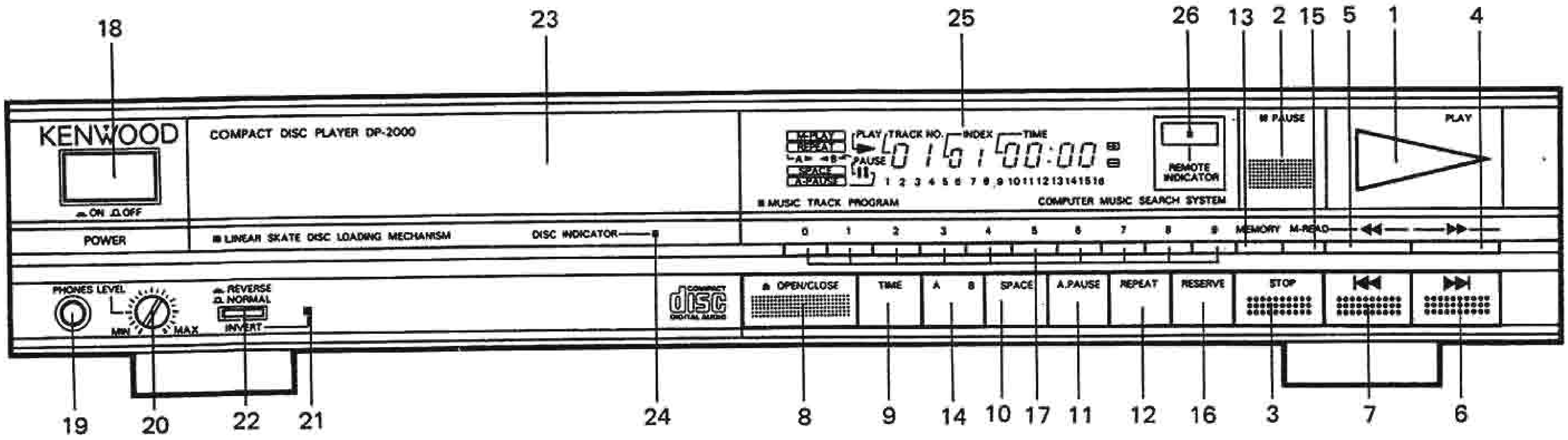


Fig. 3–4 Principle of generation of tracking error signal

CIRCUIT DESCRIPTION

4. Key operations and Displays

4–1. Front panel component names (DP-2000/1000)



1 : PLAY key
2 : Pause key (II PAUSE)
3 : STOP key
4 : Fast forward key (▶▶)
5 : Fast backward key (◀◀)
6 : Music search up key (▶▶)
7 : Music search down key (◀◀)
8 : OPEN/CLOSE key (▲)
9 : TIME key
10 : SPACE key
11 : Auto-pause key (A-PAUSE)
12 : REPEAT key
13 : MEMORY key
14 : Section memory key (A▶◀B)
15 : Memory read key (M- READ)
16 : RESERVE key
17 : Music track program select key (Ten key, 0 ~ 9)
18 : POWER switch
19 : Headphones jack (PHONES)
20 : Headphones level control (PHONES LEVEL)
21 : INVERT incicator
22 : INVERT switch
23 : DISC tray
24 : DISC INDICATOR
25 : DISPLAY
26 : Remote control indicator (REMOTE INDICATOR)

- **18 through 21 are irrelevant to the main microprocessor.**
- **21 and 22 are not provided in the DP-1000.**

Fig. 4–1

4–2. Displays

- **Display panel**

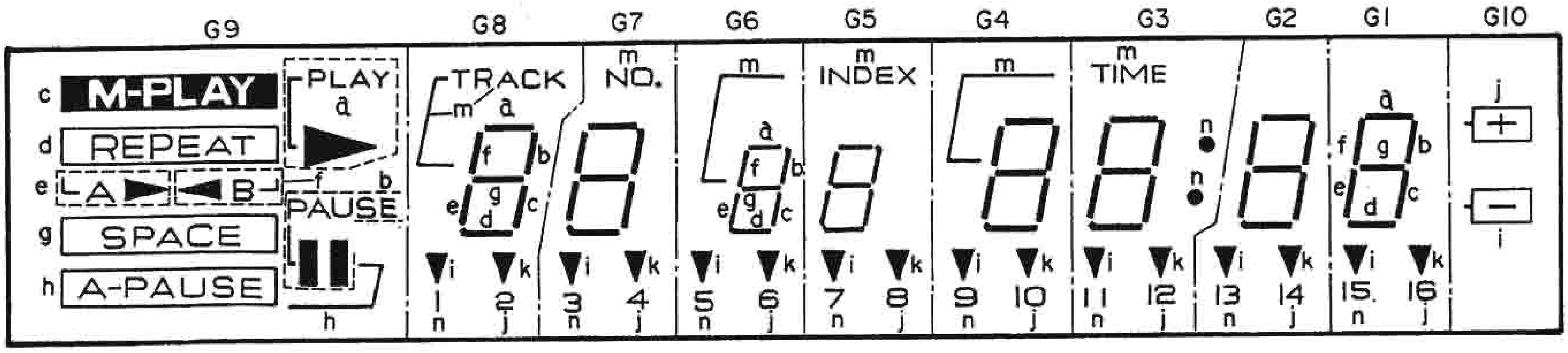


Fig. 4–2

CIRCUIT DESCRIPTION

● Displayed data

G	P	Indicator/data	Description
9	c	M-PLAY	● Comes on when a truck number is stored in memory in STOP mode. Stays on during M-PLAY. ● Goes off when the STOP switch is pushed.
9	d	REPEAT	● Turned ON/OFF by the REPEAT key. ● Also comes on when an A point is selected with the A▶◀B key.
9	e f	A▶◀B REPEAT	● "└A▶ " comes on together with "REPEAT" when an A point is selected with the A▶◀B key. Similarly, " ◀ B┘" comes on when a B point is selected. ● When "REPEAT" is off, "└A▶ " comes on immediately after the B point is passed.
9	g	SPACE	● Turned ON/OFF by the SPACE key.
9	h	A-PAUSE	● Turned ON/OFF by the A-PAUSE key.
9	a	PLAY	● Stays on while in PLAY state and comes on the PLAY key is pushed. ● Also stays on in SPACE mode or during search though the player is not playing if it is going to play after the end of the SPACE or search.
9	b	PAUSE	● Stays on while in PAUSE state and comes on when the PAUSE key is pushed.
8 7	–	TRACK No.	● These two data digits display the track number. ● Also display the contents of the CH in three seconds after the MEMORY or M-READ key is pushed.
6 5	–	INDEX	● These two data digits display the INDEX. ● Display 00 in three seconds after the MEMORY or M-READ key is pushed.
4~1	–	Time	● These four digits display the CH as well as the following different time data. ● Display relative time, absolute time, remaining time.
8~1	h j	Triangle mark (▼)	● When a track number of from 1 to 16 is stored in memory, the corresponding triangle mark comes on. ● During normal PLAY, the triangle mark above the reserved track number is on. ● The currnently lighted triangle marks goes off when the STOP key is pushed.
8~1	h j	Track number (1~16)	● The number of from 1 to 16 corresponding to the current disc track is lighted. ● The currently lighted disc number goes off when the OPEN/CLOSE key is pushed.
10	j	⊞	● Lighted to indicate absolute time.
10	i	⊟	● Lighted to indicate remaining time.

Table 4–1

● Displays in DP-2000/1000 states

● Disk non-loaded

When no disc is loaded, all of the TRACK No., INDEX, and time data digits display zeroes after the set is turned on.

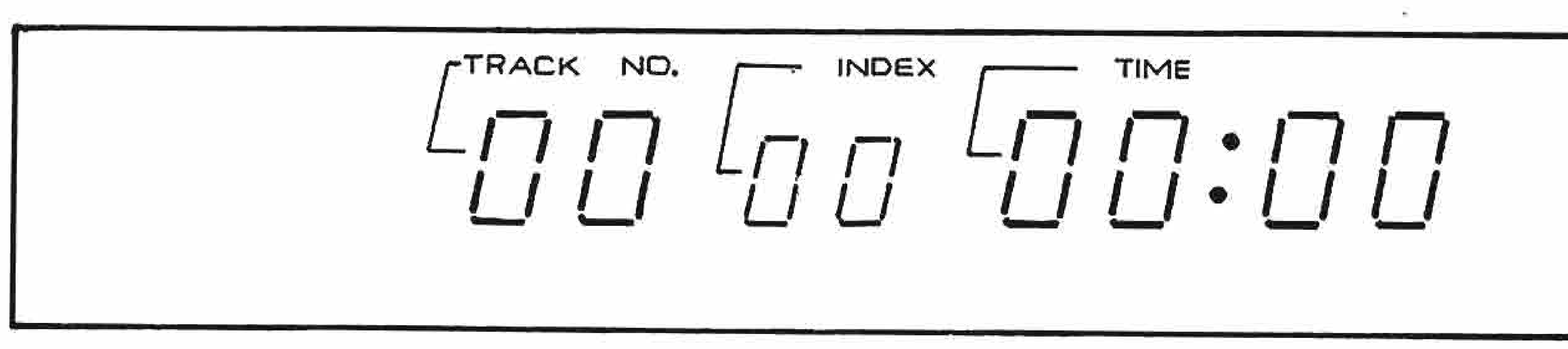


Fig. 4–3. Disc non-loaded display

● STOP or Standby

In this mode or state, the lowest track number is displayed and the time is zeroes (when neither ⊞ nor ⊟ is displayed).

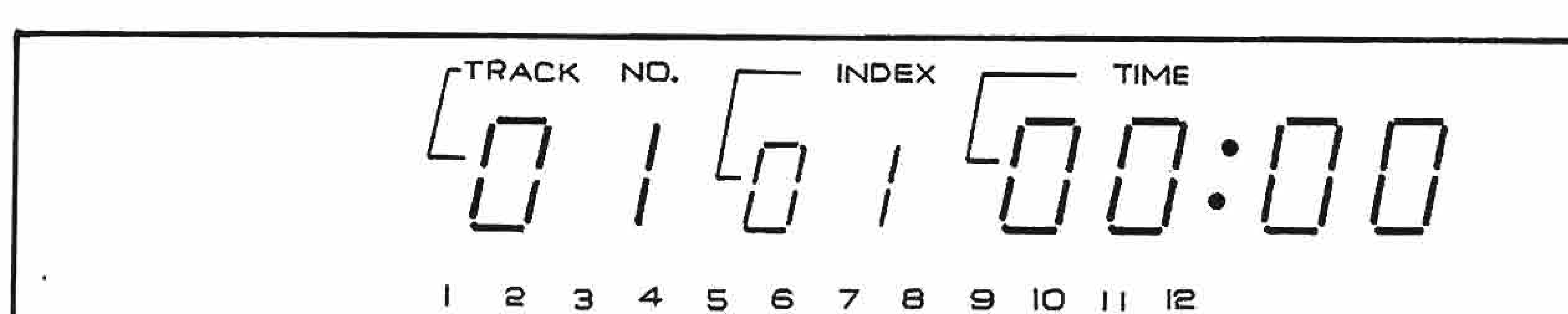


Fig. 4–4. STOP or standby display

CIRCUIT DESCRIPTION

- **PLAY**

  In PLAY mode, the mode indicator 'PLAY' and the '▶' mark below the indicator are displayed, followed by current track number, INDEX and time (in minutes and seconds). The right example also includes the 'REPEAT' indicator.

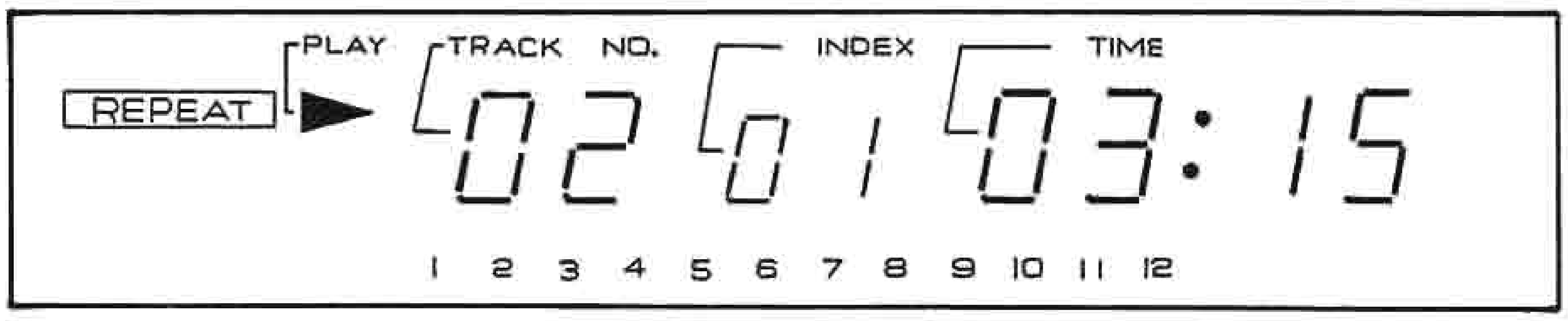


Fig. 4–5. PLAY display

- **PAUSE**

  In PAUSE mode, the mode indicator 'PAUSE' and 'the '▮▮' mark below the indicator are lighted, followed by the time of the pause position as well as the current track number and index.

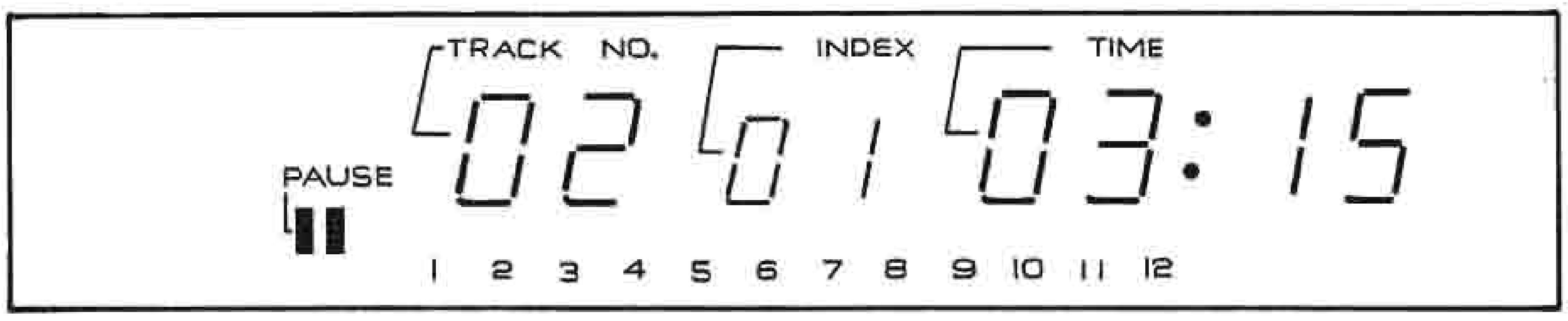


Fig. 4–6. PAUSE display

- **Displayed time mode [+] and [–]**

  When + mode is selected (reflected by the [+] indicator), the time digits display the amount of time that has so far been played (see the left figure in fig. 4–7). When – mode is selected (reflected by the [–] indicator), the digits display the remaining play time (see the right figure in fig. 4–7.)

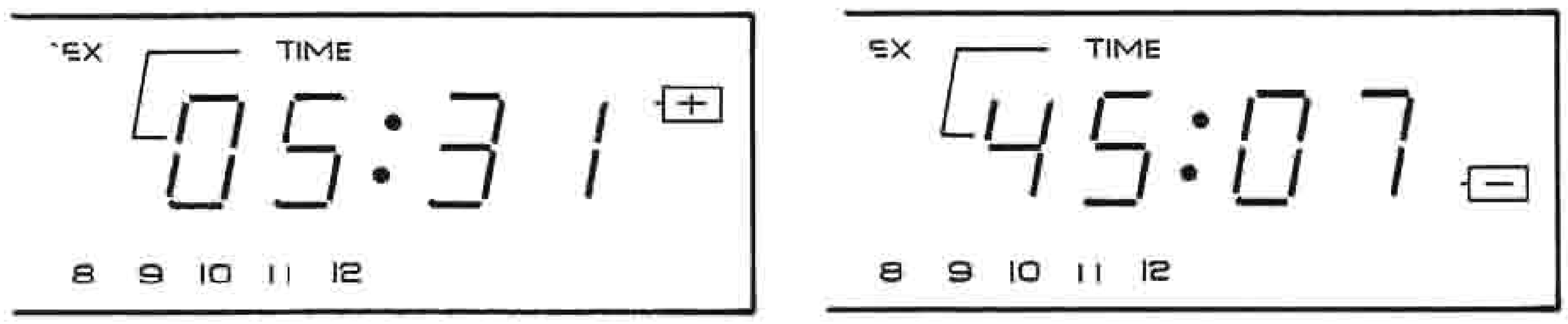


Fig. 4–7. Time displays

- **A▶◀B repeat**

  The left figure in fig. 4–8 shows the indications appearing when the A point is selected. The center figure shows the indications appearing when the B point is selected.

  A▶◀B repeat mode is removed by pushing the REPEAT key (see the right figure.)

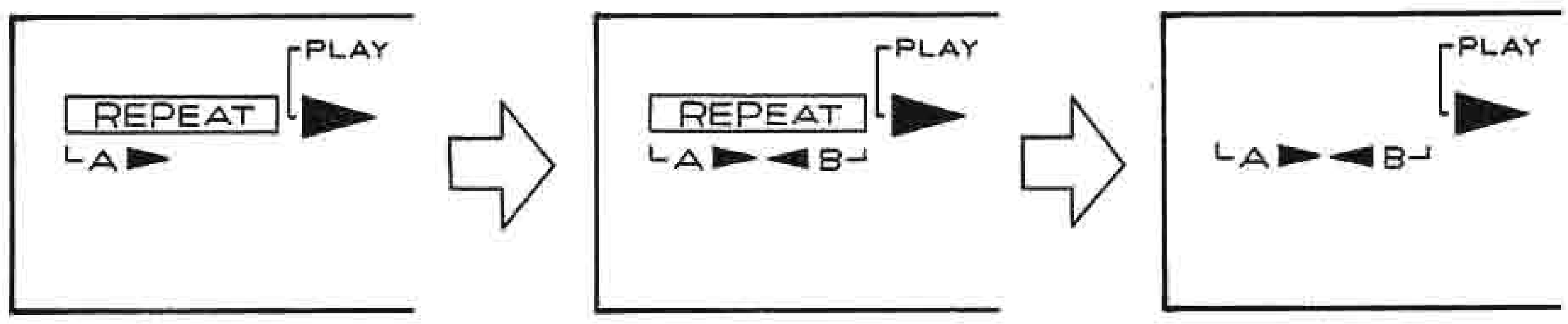


Fig. 4–8. A▶◀B repeat displays

- **A-PAUSE**

  If the A-PAUSE feature has been enabled during PLAY (reflected by the 'A-PAUSE' indicator as shown in the left figure in fig. 4–9), the 'PAUSE' indicator and the ' ' mark are displayed when the set enters A-PAUSE mode at the end of the current music.

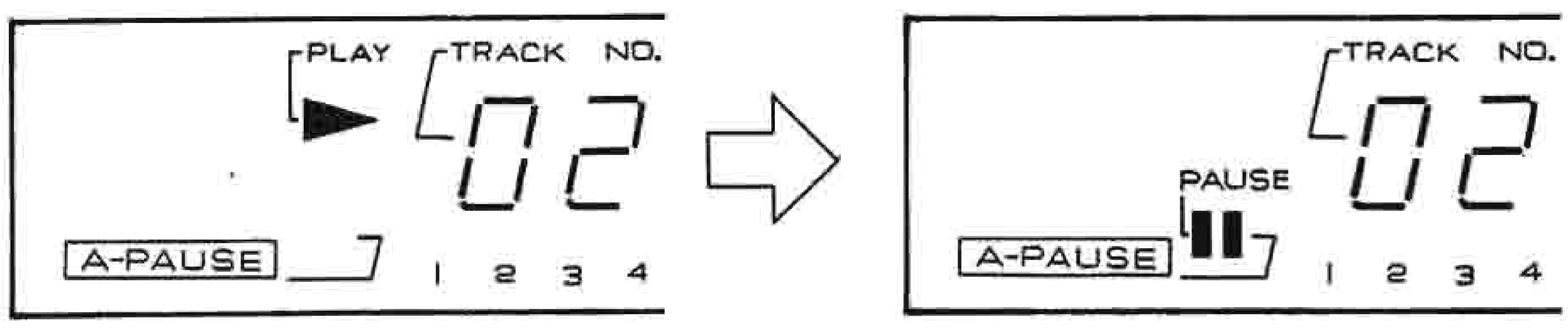


Fig. 4–9. A-PAUSE displays

- **SPACE**

  The right figure in fig. 4–10 shows example indicators and information which are displayed when this feature is selected. The set is in WAIT state for about four seconds at the beginning of the fourth piece of music after the third was played. The time digits are cleared.

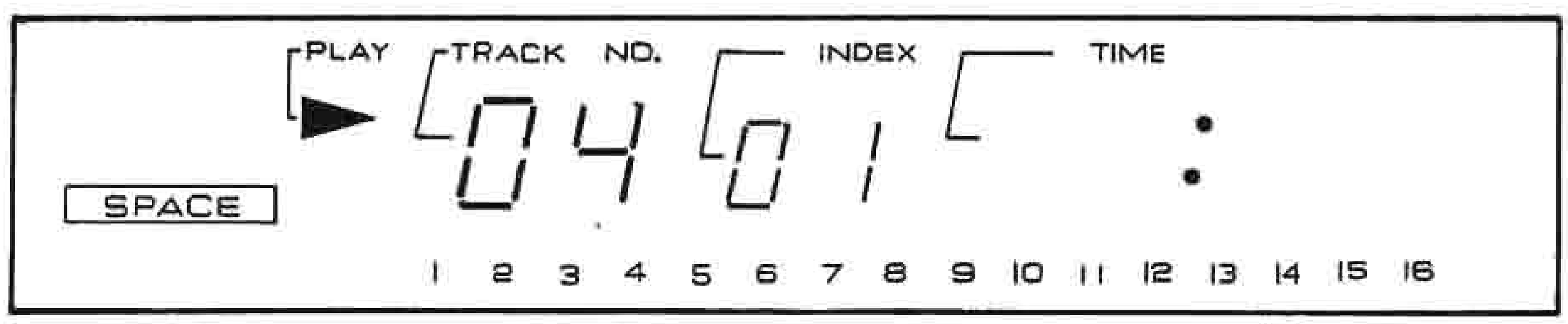


Fig. 4–10. Space display

- **RESERVE indication**
  This feature is enabled when a piece of music is RESERVEed via the ten keys. Fig. 4–11 is an example in which track 8 is reserved by pressing the '8' key. The inverse triangle mark ' ▼ ' above track number 8 is lighted.

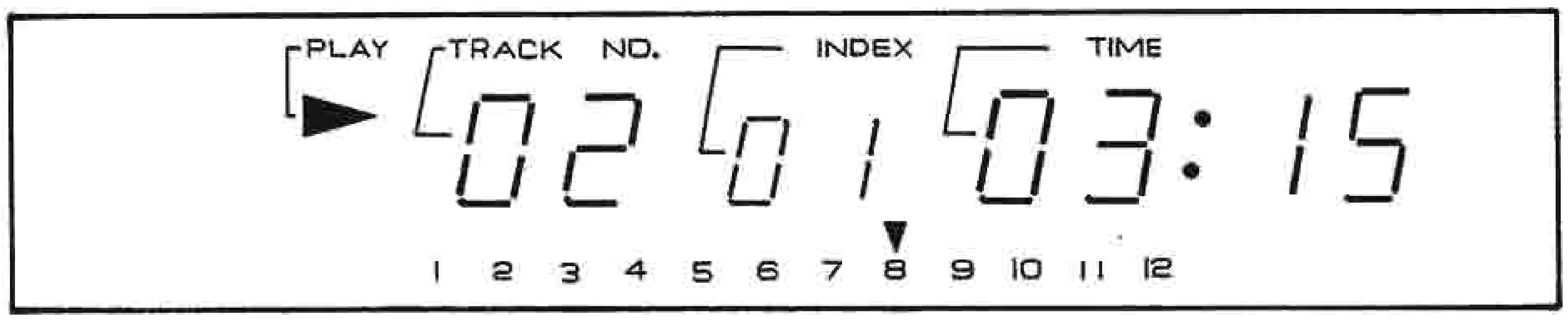


Fig. 4–11. RESERVE display

Memory PLAY displays

- **Memory write**
  Fig. 4–12 is an example displayed when tracks 1, 3, 4, 9, and 12 are transferred to memory. The inverse triangle marks ' ▼ ' above the written track numbers are lighted.

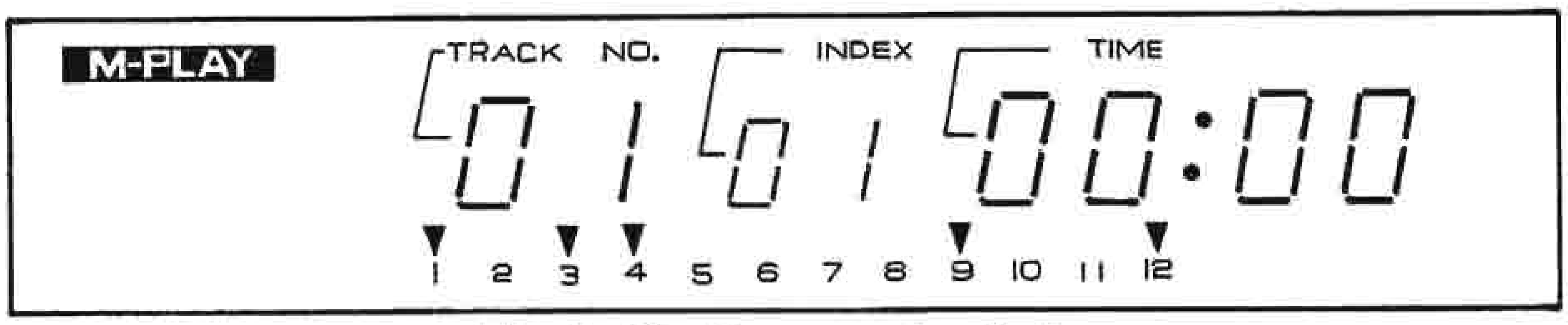


Fig. 4–12. Memory write display

- **M-READ**
  When the M-READ key is pushed, the selected memory CH number and the number of track stored in that CH are displayed for three seconds.

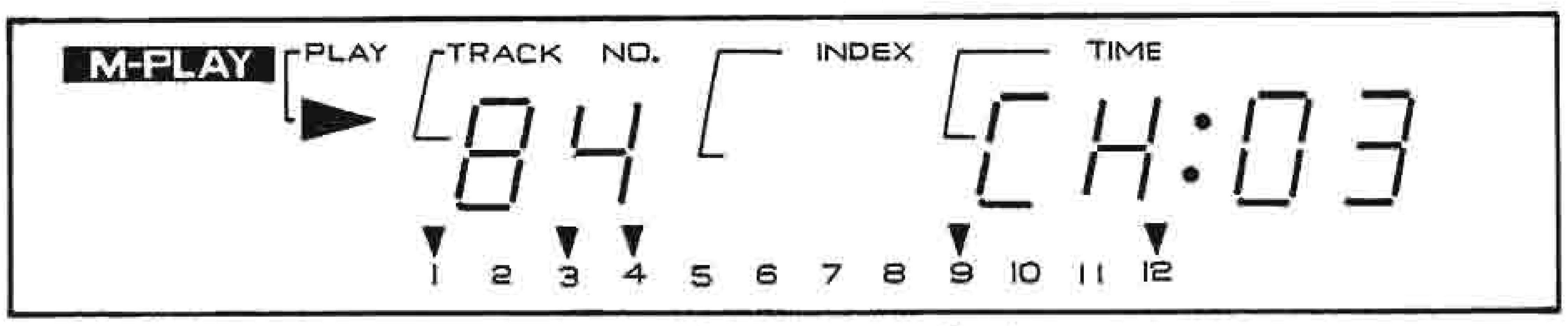


Fig. 4–13. M-READ display

- **M-READ in [+] or [−] displayed time mode**
  Since not time data is available for the 16th piece of music or above, the time digits display horizontal bars as shown in fig. 4–13.

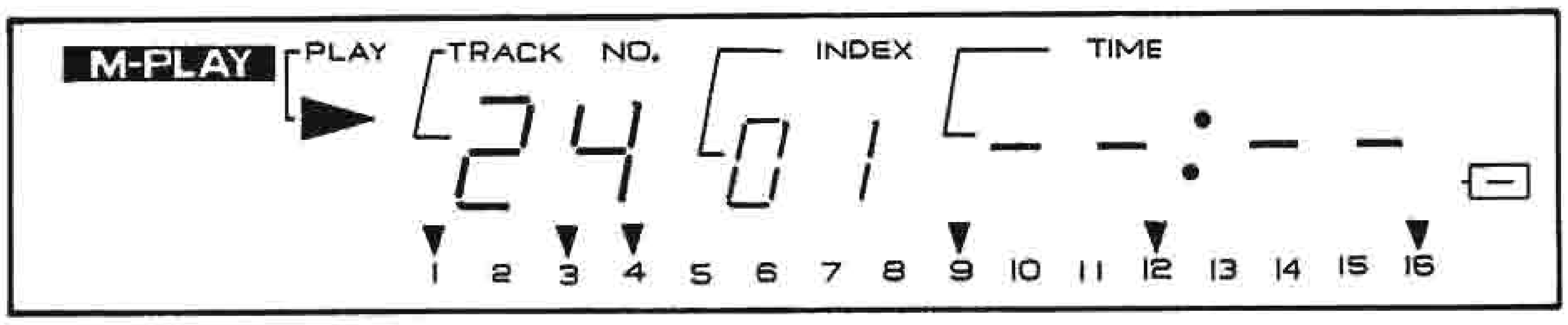


Fig. 4–14. M-READ display with [+] or [−] selected

- **Memory write of tracks 17 and above**
  Since the track number indicators are available only for tracks 1 through 16, no corresponding inverse triangle mark ' ▼ ' is lighted when track 17 or above is written to memory.

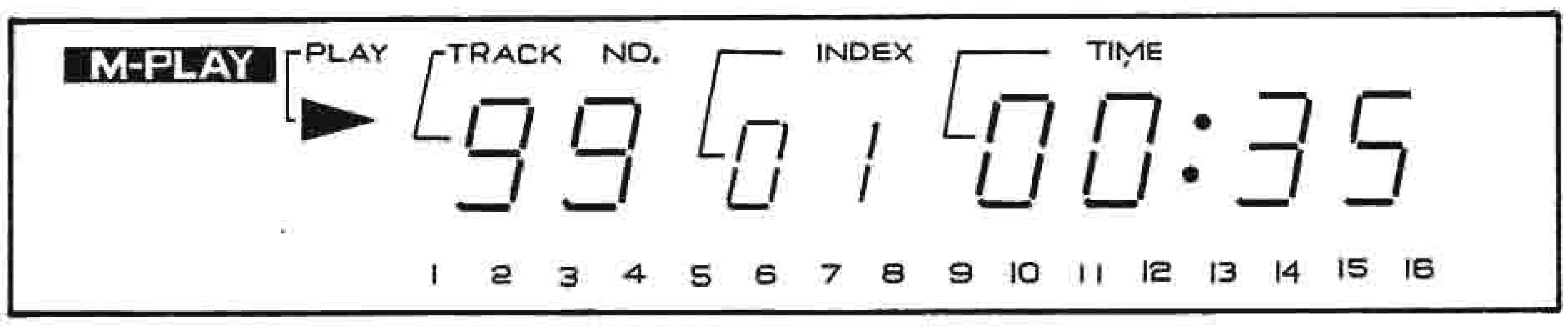


Fig. 4–15. Display for memory write of track 17 or above

4–3. Keys and Their Functions

● Normal mode

Key No.	Key name	Function
1	PLAY	Turns on the "PLAY" indicator and starts playing; ● When pushed with tray OPEN .... Tray CLOSE before playing ● When pushed after ten keys .... Music head search followed by normal PLAY. ● When pushed after M-READ .... Music head search followed by M-PLAY. ● When pushed after M-READ and ten keys .... Music head search of the current CH followed by M-PLAY (ten-key entry is ignored.)
2	PAUSE	Turns on the "PAUSE" indicator and pauses the player with the pickup maintained at the current position; ● When PAUSE key is pushed with tray OPEN . . Tray CLOSE followed by PAUSE. ● When pushed after ten keys .... Music head search followed by PAUSE. ● When pushed after M-READ .... Music head search of the memory CH followed by PAUSE ● When pushed after M-READ and ten keys .... Current CH head search followed by M-PAUSE (ten keys are ignored.)
3	STOP	Stops playing, turns the laser OFF, stops the disc, and returns the pickup to the start position; ● Track No. digits display the lowest Track No., INDEX digits display "01", and TIME digits display "00 : 00" ● Current CH is cleared and Memory PLAY mode is removed.
4	FF (▶▶)	Feeds the pickup fast forward or skips track; ● When pushed during PLAY .... The player is cued (–12dB). ● When pushed during PAUSE .... The player is muted. ● When momentarily pushed .... 8 or 16 tracks are skipped forward. ● This key is effective only within the current piece of music while in M-PLAY or PAUSE mode.
5	BWD (◀◀)	● Feeds the pickup fast backward or skips tracks; ● When pushed during PLAY .... The player is cued (–12dB). ● When pushed during PAUSE .... The player is muted ● When momentarily pushed .... 8 or 16 tracks are skipped backward. ● This key is effective only within the current piece of music while in M-PLAY or PAUSE mode.
6	UP (▶▶|)	Searches for the next music or CH (in M-PLAY mode) head or counts the Track No.; ● When pushed during normal PLAY .... Next Track No. head search followed by PLAY. ● When pushed in normal PAUSE .... Next Track No. head search followed by PAUSE. ● When pushed during M-PLAY .... Next CH head search followed by PLAY. ● When pushed in M-PAUSE .... Next CH head search followed by PAUSE. ● When pushed with disc stopped .... Track No. is counted up from the lowest Track No. (Track No. returns to the lowest Track No. three seconds later.) ● When pushed with tray OPEN .... Track No. is counted up from 1 (Track No. is cleared three seconds later.) ● When pushed with tray open and no disc loaded . This key operation is ignored. ● When momentarily pushed (for 0.3 second or below) .... The Track No. is counted up by 1. ● When continuously pushed .... Track No. is counted up by 1 every 0.3 second. ● When pushed with highest Track No. in Track No. .... Track No. returns to the lowest Track No.
7	DOWN (|◀◀)	Searches for the current or immediately preceding Track No. or CH head depending on whether this key is pushed momentarily or continuously (two successive pushes within 0.3 second is equivalent to a continuous push); ● When pushed during normal PLAY .... Current or preceding track head search followed by PLAY. ● When pushed in normal PAUSE .... Current or preceding track head search followed by PAUSE. ● When pushed during M-PLAY .... Current or preceding CH head search followed by PLAY. ● When pushed in M-PAUSE .... Current or preceding CH head search followed by PAUSE. ● When pushed while disc is stopped .... Track No. is counted down (Track No. returns to the lowest Track No. after three second later.) ● When pushed with tray OPEN .... Track No. is counted down (Track No. is cleared three seconds later.) ● When pushed with no disc loaded and tray OPEN .... This key operation is ignored. ● When continously pushed .... Track No. is counted by 1 every 0.3 second. ● When pushed with lowest Track No. in Track No. .... Track No. returns to the highest Track No.

Table 4–2

CIRCUIT DESCRIPTION

Key No.	Key name	Function
8	OPEN/CLOSE	OPENs or CLOSEs the disc tray (not effective in A-PAUSE and SPACE modes); OPEN • Current CH is displayed and TOC data is cleared whenever this key is pushed. • When pushed during PLAY or in PAUSE . . . . The laser is turned OFF, the tray is OPENed after one second, and then the Track No. indicators go off. • When pushed while disc is stopped . . . . The tray is immediately OPENed and the Track No. indicators go off. CLOSE • When pushed, the tray is CLOSEd, the DISC indicator LED comes on if a disc is loaded, the TOC data is read, and the set is read. If no disc is loaded, all the data digit fluorescent lights display zeroes.
9	TIME	Selects one of the three displayed time modes; relative time (elapsed time within the current single piece), absolute time (TOTAL) elapsed time, selected by $\boxed{+}$), and REMAINING time (selected by $\boxed{-}$). • When pushed in STOP with $\boxed{+}$ indicated . . . Track No. displays the lowest Track No., INDEX displays "01", and TIME displays the lowest track absolute start time. • When pushed in STOP with $\boxed{-}$ indicated . . . . Track No. displays the lowest Track No., INDEX displays "01", and TIME displays the last data area absolute time. (See 15. M-READ for the description on the functions provided by this key with $\boxed{+}$ or $\boxed{-}$ selected in M-PLAY mode).
10	SPACE	Provides a 4-second (including search time) SPACE between pieces of music. In A ▶◀B repeat mode, this key is effective between tracks when the A position is selected; • When PLAY key is pushed during this 4-second wait . . . . The next piece is played four seconds later. • When PAUSE key is pushed during this 4-second wait . . . . The set PAUSEs four seconds later.
11	A-PAUSE	After the current piece of music is played, searches for the next piece head, and PAUSEs the set: • This key is not effective between tacks in FF or BWD mode. • The set PAUSEs only when the Track No. changes during PLAY. • In A▶◀B repeat mode, the set plays up to B, searches for A, and PAUSEs. • Music head search by the UP or DOWN key is not effective.
12	REPEAT	This key is stationary. When set ON, it plays the music from the first piece again after the last piece is played; • All pieces are normally PLAYed, M-PLAY, A▶◀B } Repeated play • When REPEAT is reset OFF, the set is STOPped after the last piece or CH is played.
13	MEMORY	Writes a given track among the lowest through the highest to the currently selected CH. • The INDEX is excluded (always index "01" is written.) • Tracks 1 through 99 can be written. • Up to 16 pieces of music (CHs 1 through 16) can be written. • The pieces are written sequentially from CH 1. • A piece is written by one of the following sequences of key operations in STOP state; (Displayed Track No.) → MEMORY UP/DOWN → MEMORY Ten keys → MEMORY • Any CH can be rewritten (except during PLAY). Read the CH to be rewritten with the M-READ key, enter a desired Track No. via the ten keys, and then push the MEMORY key.
14	Memory write between two points (A▶◀B)	Repeats to play the music between any two selected points A and B; • First time – The A point is stored and the "A" and "REPEAT" indicators are turned on. • Second time – The B point is stored, the A point is located and played. • When two or more pieces of music are contained between the two points, the A-PAUSE and SPACE keys are effective. • If REPEAT is reset OFF, the "A▶◀B" indicators go off after the music is played to the B point.

Table 4–2

CIRCUIT DESCRIPTION

Key No.	Key name	Function
15	M-READ	Reads memory data sequentially from CH1 to the highest CH (each CH is displayed for three seconds). • In M-PLAY mode, the currently played CH is displayed first. • When followed by PLAY . . . . Memory PLAY from the specified CH. • When followed by ten keys and MEMORY . . . CH rewrite to memory. * M-READ displays When the M-READ key is pushed, the following data are displayed; In STOP state When [+] is indicated . . . . All the Track Nos. in memory and TOTAL play time of all the music in memory. When [−] is indicated . . . . All the Track Nos. in memory and the play time of the displayed Track No. During M-PLAY or PAUSE The current Track No. and its relative play time; When [+] is indicated . . . . The current Track No. and the total elapsed play time of all the preceding CH's. When [−] is indicated . . . . The current Track No. and the remaining time from the current to the highest CH. When any track above Track No. 16 is written in memory, the TIME fields displays "—— : ——" regardless whether [+] or [−] mode is selected if the lowest Track No. in memory is "01".
16	RESERVE	Allows a piece of music to be reserved as the request to be played next during normal PLAY or PAUSE; • A reservation is made by specifying a track via the ten keys and then pushing the RESERVE key. • The " ▼ " mark above the reserved Track No. comes on. • The Track No. being reserved must be between 1 and 16 inclusive. • The reserved piece is unreserved when UP/DOWN, STOP, OPEN/CLOSE key is pushed or by a ten key search. • When FF or BWD key is used, the play jumps to the reserved piece after the new track is played. • The reserved piece can be rewritten.
17	Ten keys	Used for track write to CH, music head search, and music reservation, etc.; • Ten key entry followed by MEMORY key . . . Memory write • Ten key entry followed by PLAY or PAUSE key . . . . Music head search followed by PLAY or PAUSE. • Ten key entry followed by RESERVE key . . . Reservation • Preceded by M-READ key and followed by MEMORY key . . . . CH rewrite.

- **Test mode**

Test mode is established by grounding the TEST terminal (pin 19) of the μPD7516.

Note : To establish test mode, connect TP12 and TP13 of the X32-1050-00(A/4) in the DP1000 or the X32-1040-00 (A/5) in the DP-2000.

- **Control flow of transition to test mode**

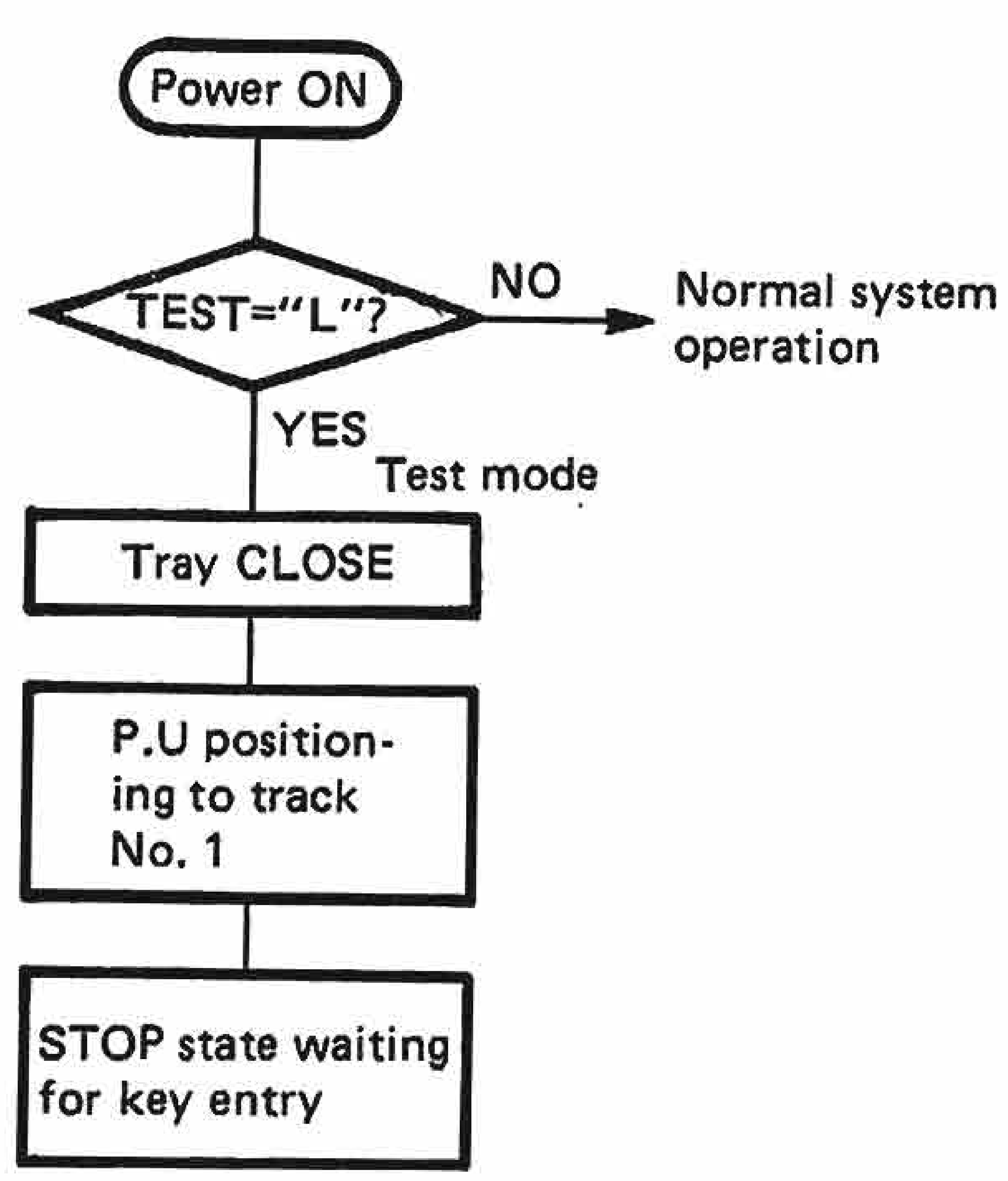


Fig. 4—16 Transition to test mode

● Keys effective in test mode and their functions

Key No.	Key name	Fuction
1	PLAY	Enables focus servo. Enables tracking servo. Enables feed servo — the set enters PLAY state but no sound is produced. If this key is pushed during PLAY, however, the set is stopped.
3	STOP	Disables focus servo Disables tracking servo. Disables feed servo and stops the set.
6	UP	Moves PU forward for about 100ms in STOP state. Moves PU forward skipping 16 tracks in PLAY state. This key is ignored in any other state.
7	DOWN	Moves PU backward for about 100ms in STOP state. Moves PU backward skipping 16 tracks in PLAY mode. This key is ignored in any other state.
8	OPEN/CLOSE	Removes test mode and opens the tray.
13	MEMORY	Enables focus servo. Enables tracking servo. Disables feed servo. Thereby, a certain area is repeatedly played.
15	M-READ	Enables focus servo. Disables tracking servo. Disables feed servo.

Table 4–3

● Control flow from power on to TOC read

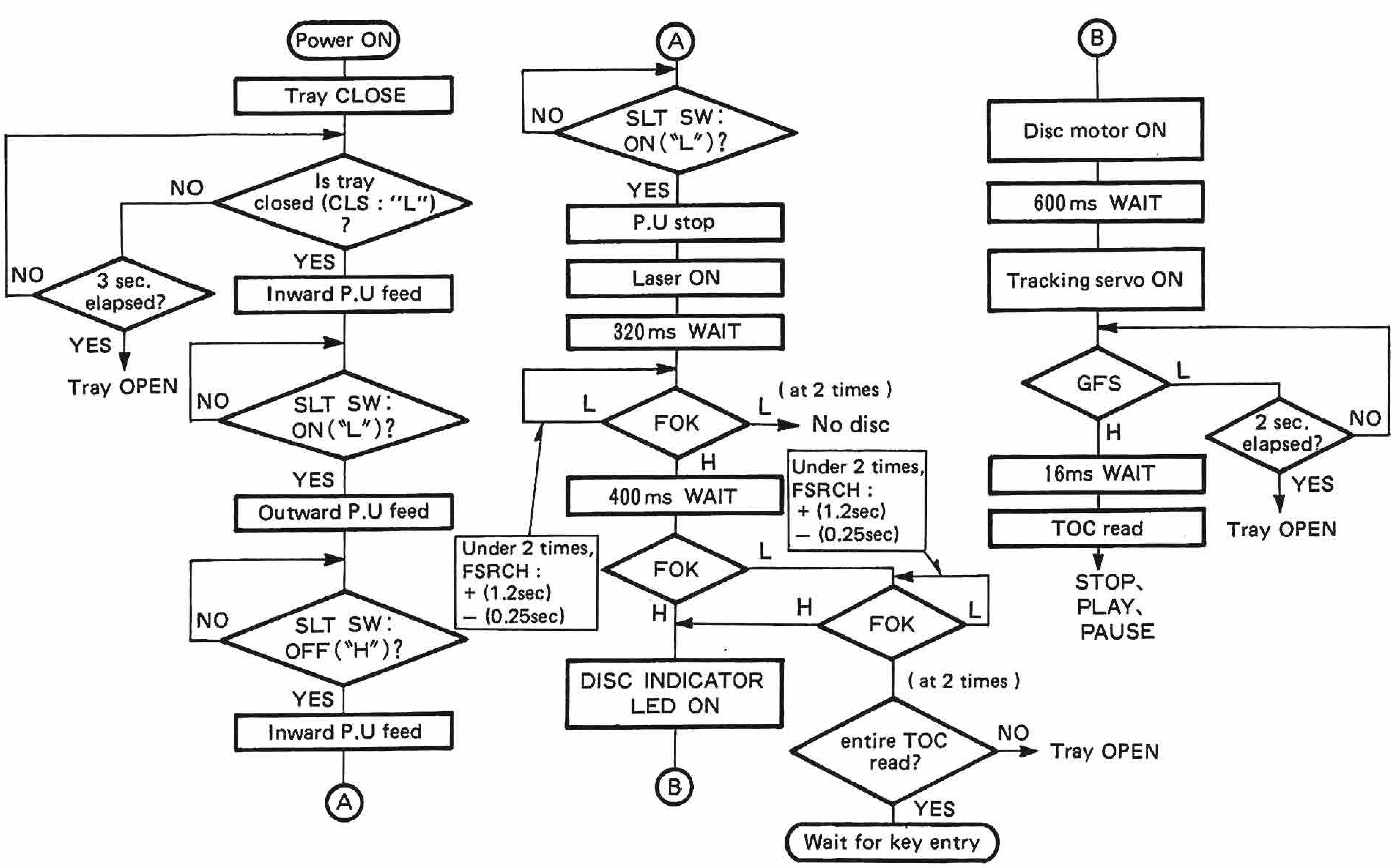


Fig. 4–17 Control flow from power on to TOC read

CIRCUIT DESCRIPTION

- **Control flow since power on until 01 is displayed below the TRACK No. indicator in test mode**

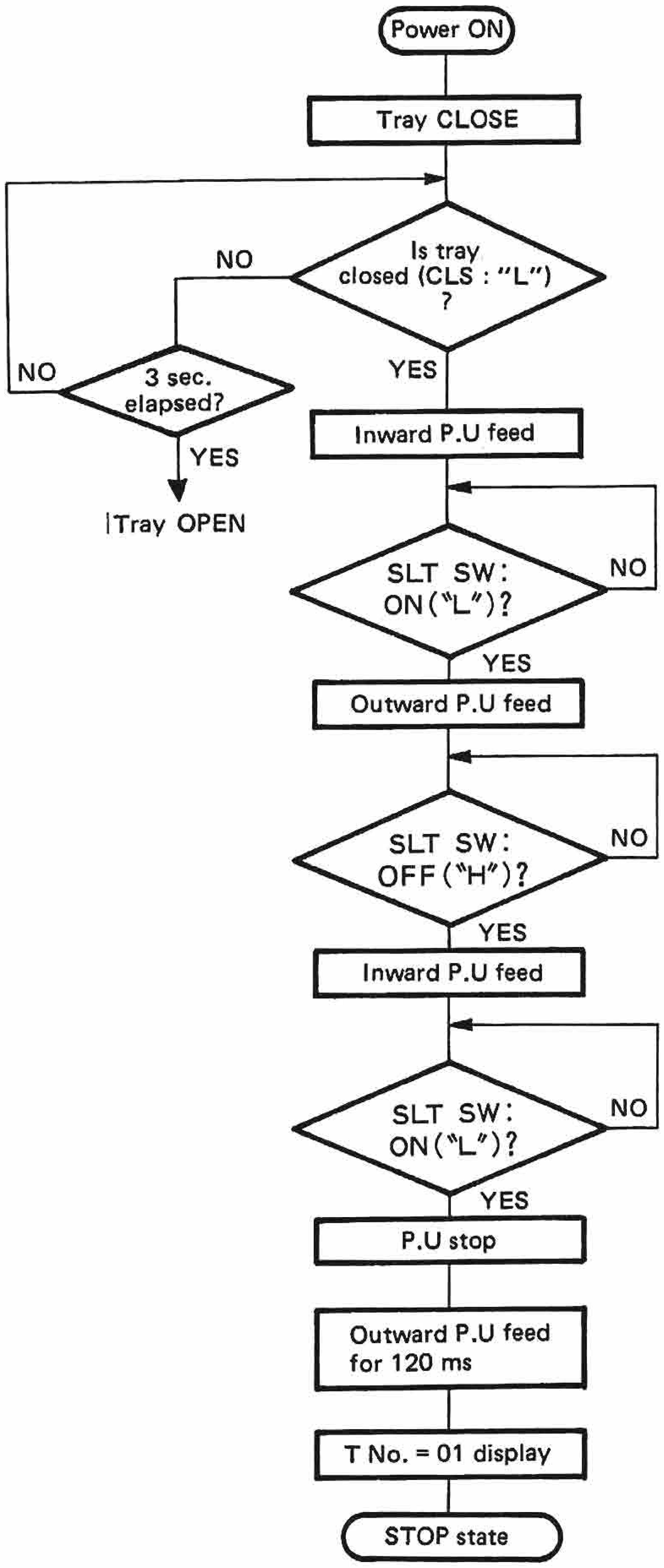


Fig. 4–18

- **Control flow after the PLAY key is pushed in STOP state**

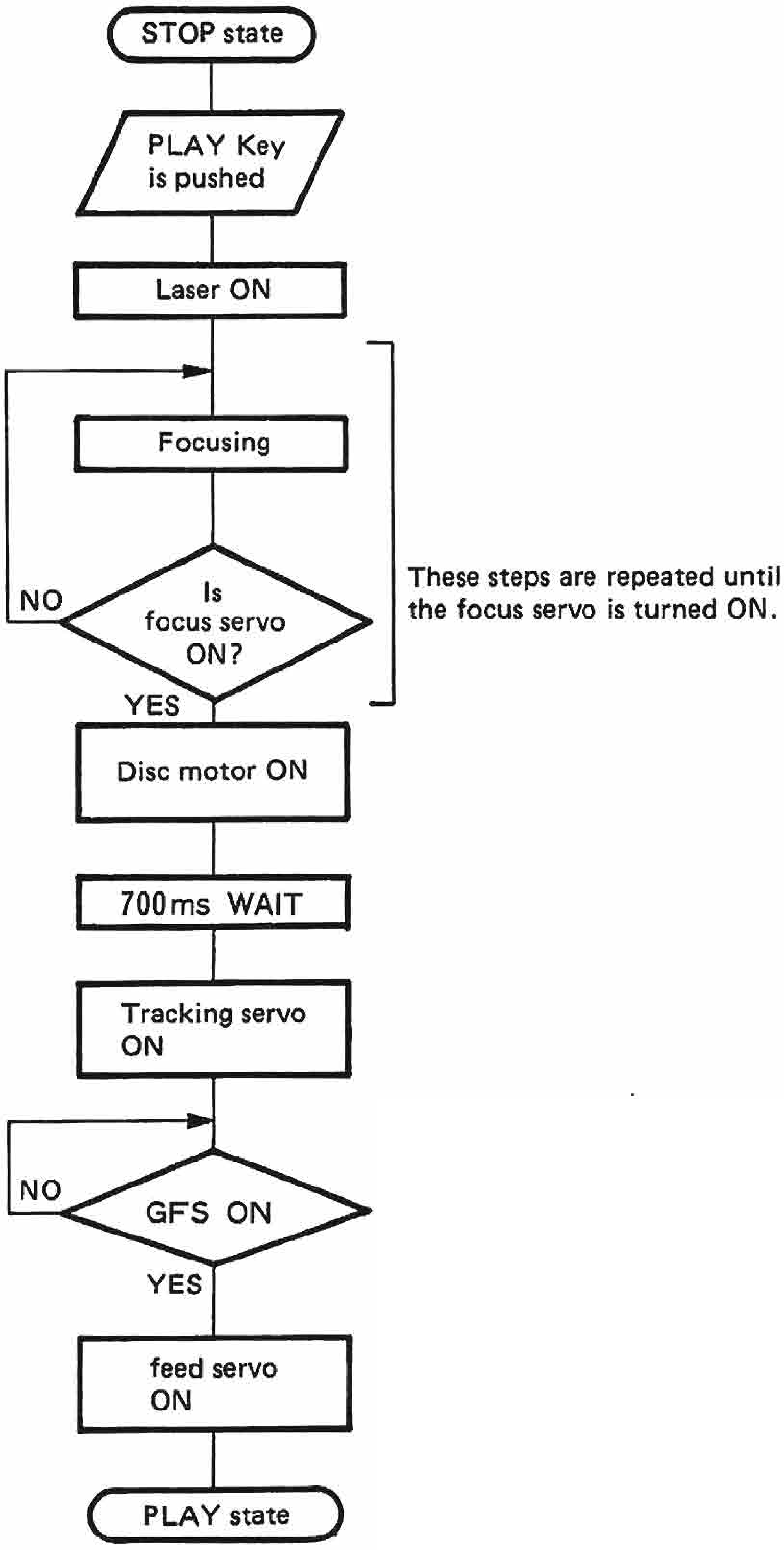


Fig. 4–19

CIRCUIT DESCRIPTION

5. Main microprocessor (μPD7516HCW-230)

5–1. Connection diagram

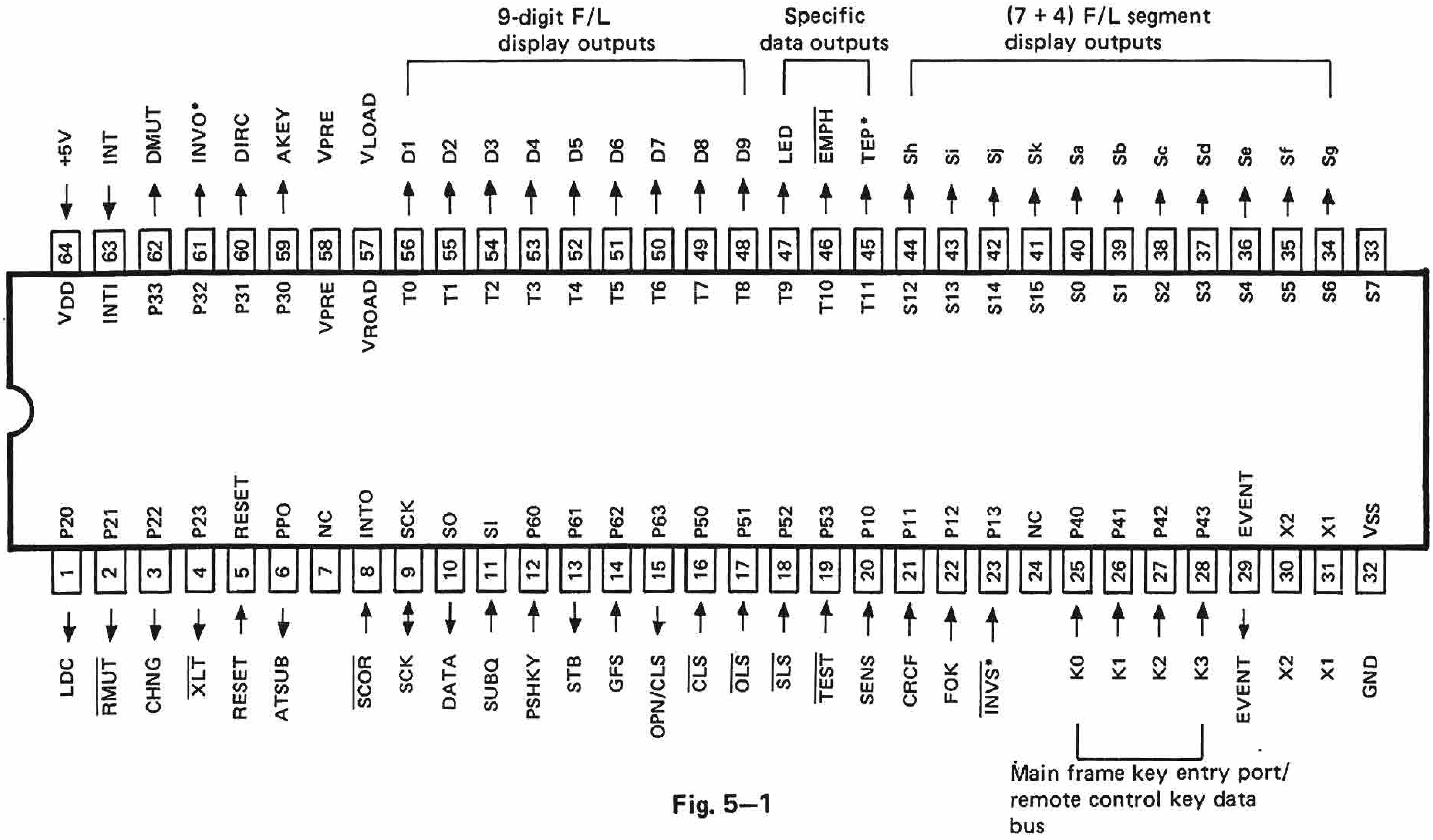


Fig. 5–1

5–2. Block diagram

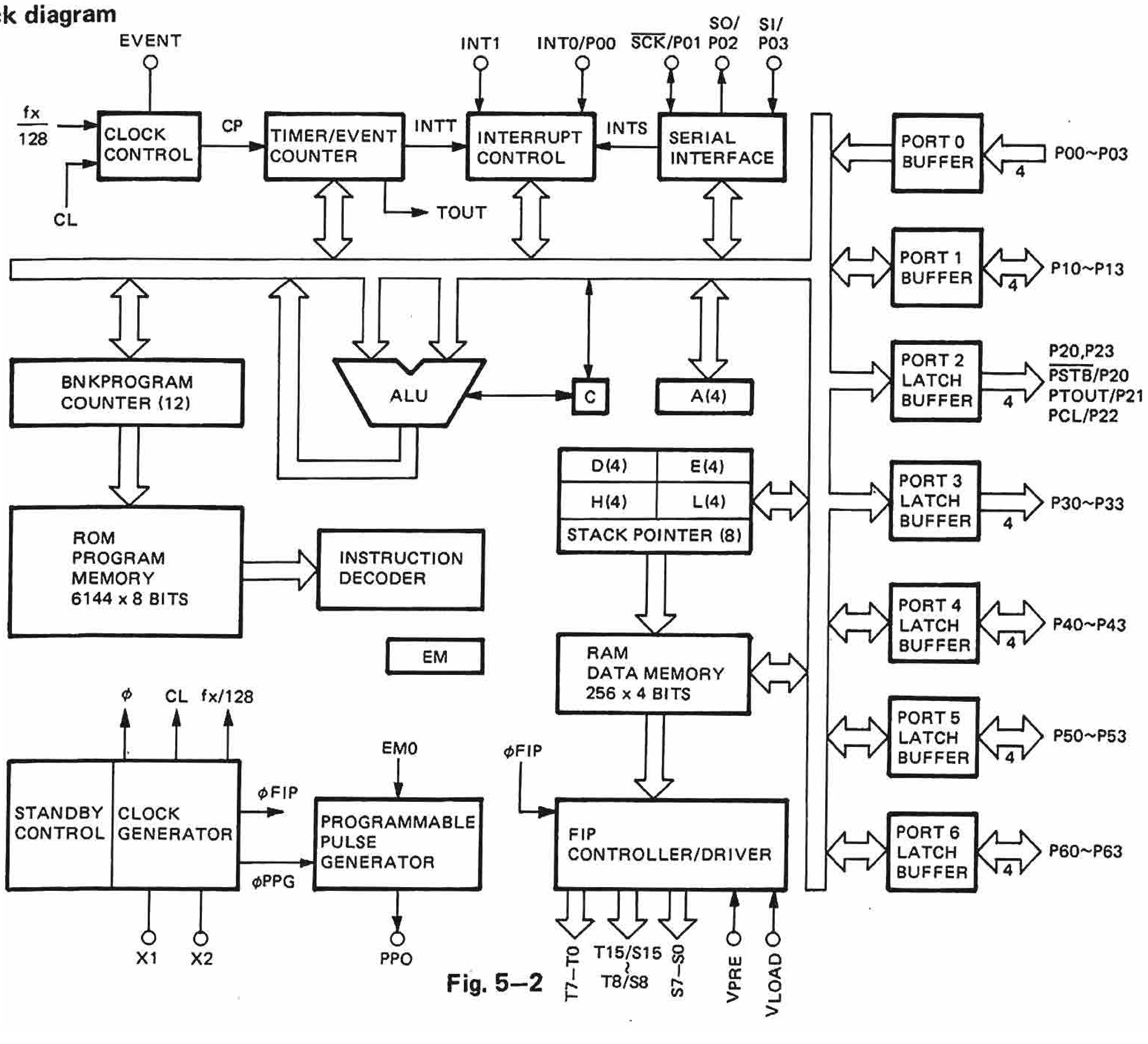


Fig. 5–2

CIRCUIT DESCRIPTION

5–3. Terminals and their functions

The asterisked (*) ports are not used in DP-1000.

Terminal No.	Port name		Signal name	I/O	Function/operation
1	P2	P20	LDC	O	Turns the laser diode ON/OFF ("H"/"L").
2		P21	$\overline{\text{RMUT}}$	O	Enables/disables relay muting ("L/"H"). RMUT is activated when playing the CD-ROM.
3		P22	CHNG	O	Controls SCK terminal I/O; Lets the terminal serve as input terminal when "H" and as output terminal when "L".
4		P23	$\overline{\text{XLT}}$	O	10μs negative going pulse to latch data to the CX23035/20108.
5		RESET	RESET	I	μPD7516 system reset input ("H" active.)
6		PPO	ATSUB	O	"H" during fast feed and "L" otherwise.
8	P1	INTO	$\overline{\text{SCOR}}$	I	Q data synchronizing signal interrupt.
9		$\overline{\text{SCK}}$	SCK	I/O	(1) Clock output to transfer DATA to the CX23035/20108 (CHNG = "L"). (2) Clock input to transfer Q data from the CX23035 (CHNG = "H").
10		SO	DATA	O	Serial data output to the CX23035/20108.
11		SI	SUBQ	I	Q data input from the CX23030.
12	P6	P60	PSHKY	I	"H" while any remote control key is depressed.
13		P61	STB	O	Strobe signal output to the remote control microprocessor to allow it to read the depressed remote control key code inputs.
14		P62	GFS	I	Disc inversion check input. The disc is determined to be inverse when GFS = "L" though in proper focus. This is the EFM synchronization OK signal from the CX23035 which indicates that the CX23035 has correctly read EFM when GFS = "H" with tracking servo ON.
15		P63	OPN/CLS	O	Tray opening/closing signal; "L" to OPEN and "H" to CLOSE. Otherwise, this terminal is forced to a high impedance.
16	P5	P50	$\overline{\text{CLS}}$	I	Tray CLOSE SW signal input port (SW ON = "L").
17		P51	$\overline{\text{OLS}}$	I	Tray OPEN SW signal input port (SW ON = "L").
18		P52	$\overline{\text{SLS}}$	I	Start limit SW (SLT) signal input port (SW ON = "L").
19		P53	$\overline{\text{TEST}}$	I	Test mode forcing terminal which puts this microprocessor in test mode when "L".
20	P1	P10	SENS	I	Sense signal input from the CX23035/20108.
21		P11	CRCF	I	Q data CRC OK input from the CX23035 (active "H").
22		P12	FOK	I	Focus servo OK input from the CX20109 (active "H").
23		P13	$\overline{\text{INVS}}$*	I	Digital output inversion specification SW input (active "L").
25	P4	P40	K0	I	Main frame key entry port/remote control DATA input bus.
26		P41	K1	I	Main frame key entry port/remote control DATA input bus.
27		P42	K2	I	Main frame key entry port/remote control DATA input bus.
28		P43	K3	I	Main frame key entry port/remote control DATA input bus.
29		EVENT	EVENT		Has no internal connection and used a Vss terminal.
30		X2	X2		Clock oscillator crystal
31		X1	X1		(6.144MHz) terminals.
32		Vss	GND		Supplies the GND potential.
33	Segment output	S7			
34		S6	Sg	O	Fluorescent display tube segment output.
35		S5	Sf	O	Fluorescent display tube segment output.
36		S4	Se	O	Fluorescent display tube segment output.
37		S3	Sd	O	Fluorescent display tube segment output.
38		S2	Sc	O	Fluorescent display tube segment ouptut.
39		S1	Sb	O	Fluorescent display tube segment output.
40		S0	Sa	O	Fluorescent display tube segment output.
41		S15	Sk	O	Fluorescent display tube segment output.
42		S14	Sj	O	Fluorescent display tube segment output.
43		S13	Si	O	Fluorescent display tube segment output.
44		S12	Sh	O	Fluorescent display tube segment output.
45	Specific output ports	T11	TEP*	O	Reset signal to the dropout control microprocessor (active "H"). "H" for track jump.
46		T10	$\overline{\text{EMPH}}$	O	Enables emphasis when "L".
47		T9	LED	O	Tray LED control signal which turns the DISC LED on when a disc is loaded.

Table 5–1

Terminal No.	Port name		Signal name	I/O	Function/operation
48	Timing output	T8	D9	O	Fluorescent display tube digit output (G1).
49		T7	D8	O	Fluorescent display tube digit output (G2).
50		T6	D7	O	Fluorescent display tube digit output (G3).
51		T5	D6	O	Fluorescent display tube digit output (G4).
52		T4	D5	O	Fluorescent display tube digit output (G5).
53		T3	D4	O	Fluorescent display tube digit output (G6).
54		T2	D3	O	Fluorescent display tube digit output (G7).
55		T1	D2	O	Fluorescent display tube digit output (G8).
56		T0	D1	O	Fluorescent display tube digit output (G9/G10).
57		V_{LOAD}	V_{LOAD}		FIP driver power supply (—28V).
58		V_{PRE}	V_{PRE}		FIP driver power supply (—5V).
59	P3	P30	AKEY	O	Allows a remote control key code read from the K0 through K3 ports by disabling the input from the main frame key (active "L").
60		P31	DIRC	O	Output signal to the CX20108 which goes "L" for 1/3 -track kick.
61		P32	INVO*	O	Inverted signal of the digital output.
62		P33	DMUT	O	Digital muting output to the CX23035.
63		INT1	INT	I	Main frame key/remote control interrupt input port.
64		V_{DD}	+ 5V	I	+ 5V supply.

Table 5—1

CIRCUIT DESCRIPTION

5–4. DP-2000 microprocessor peripheral circuit block diagram

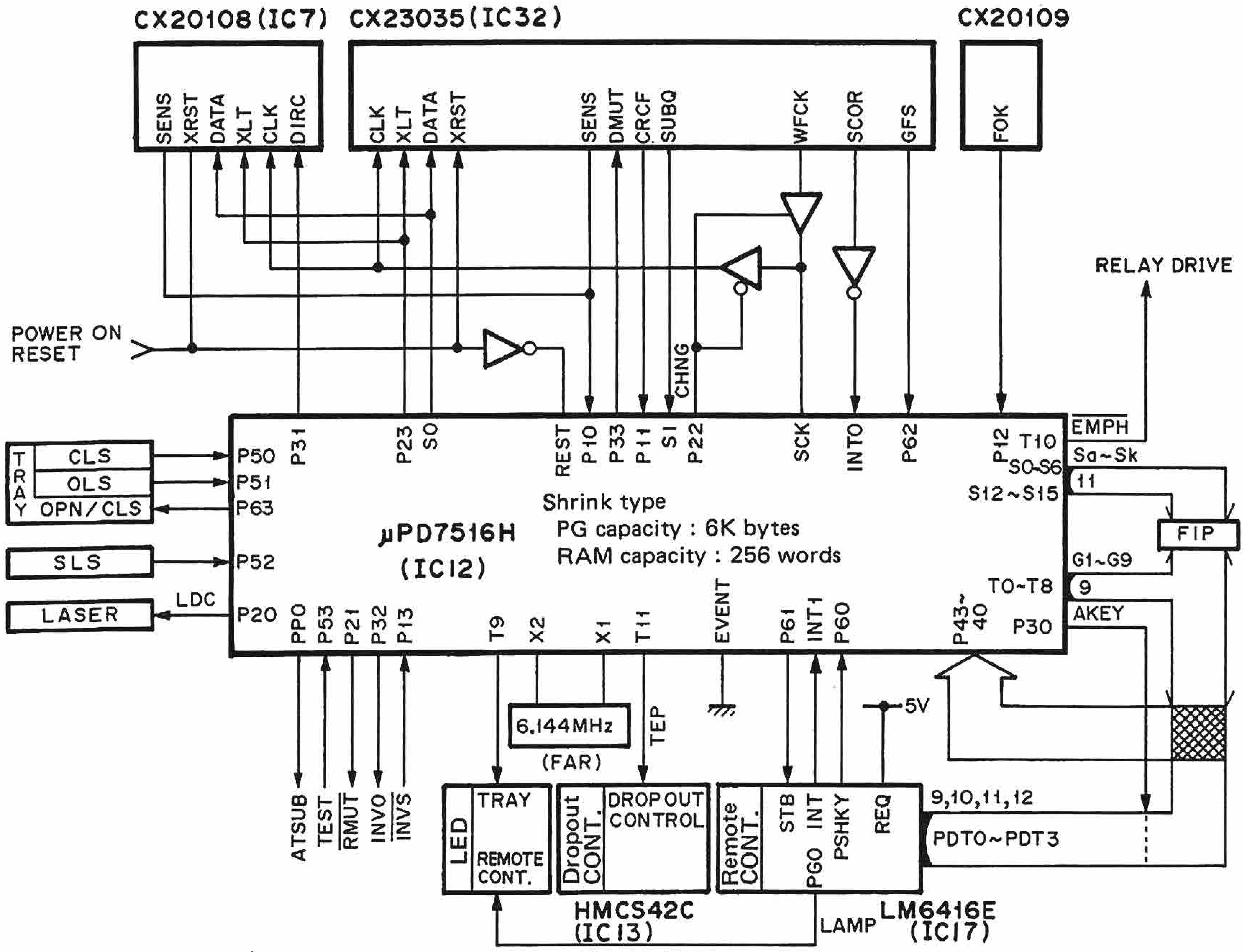


Fig. 5–3

5–5. DP-1000 microprocessor peripheral circuit block diagram

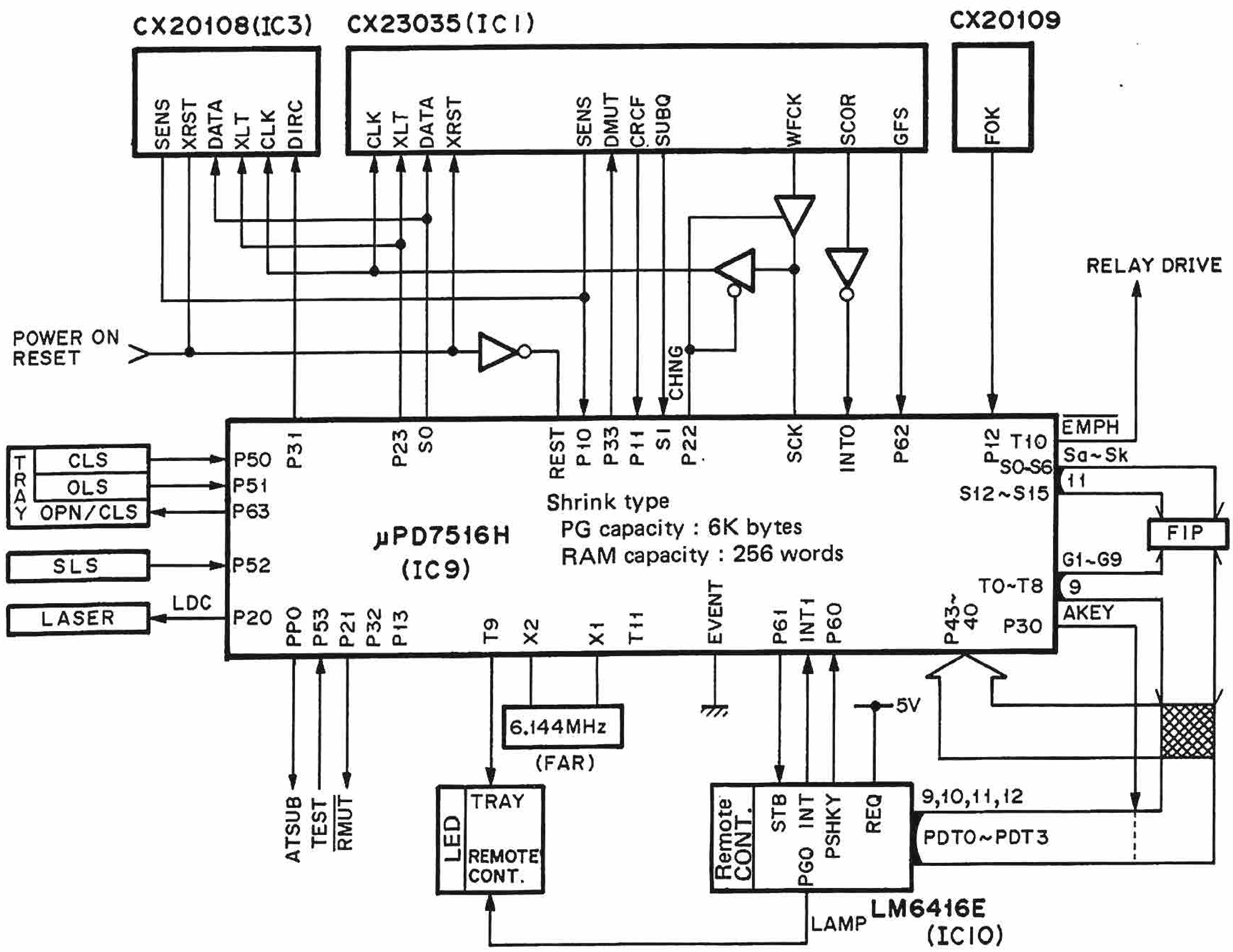


Fig. 5–4

6. RF Amplifier IC1 (CX20109)

CX20109 is a bipolar IC that includes an RF amplifier for optical system pickup output of 3-spot system developed for compact disc players as well as signal processing circuits such as focus, mirror, tracking and EFM comparator which are required for controlling the system.

6–1. Terminal connection diagram (Top view)

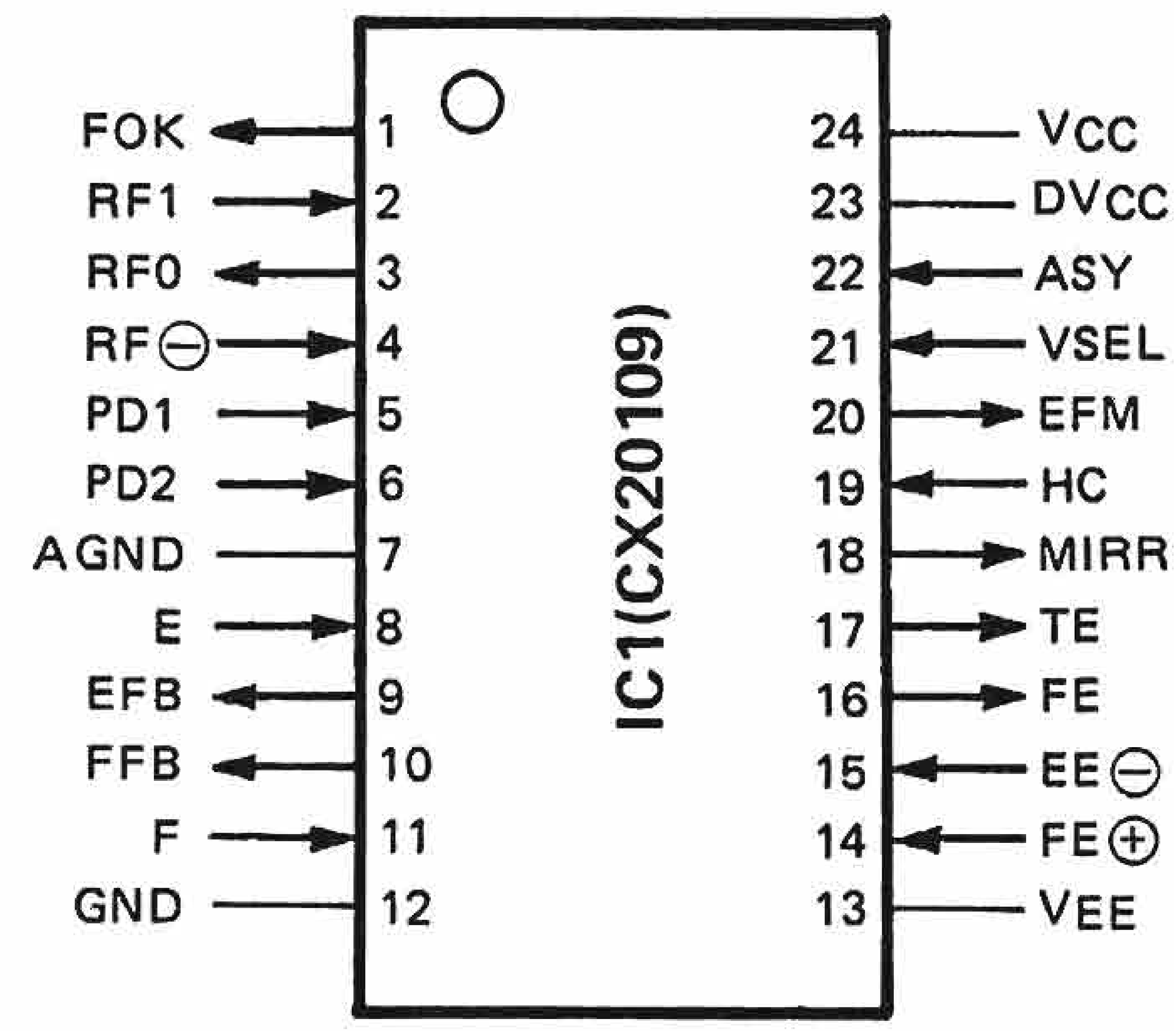


Fig. 6–1

6–2. Block diagram

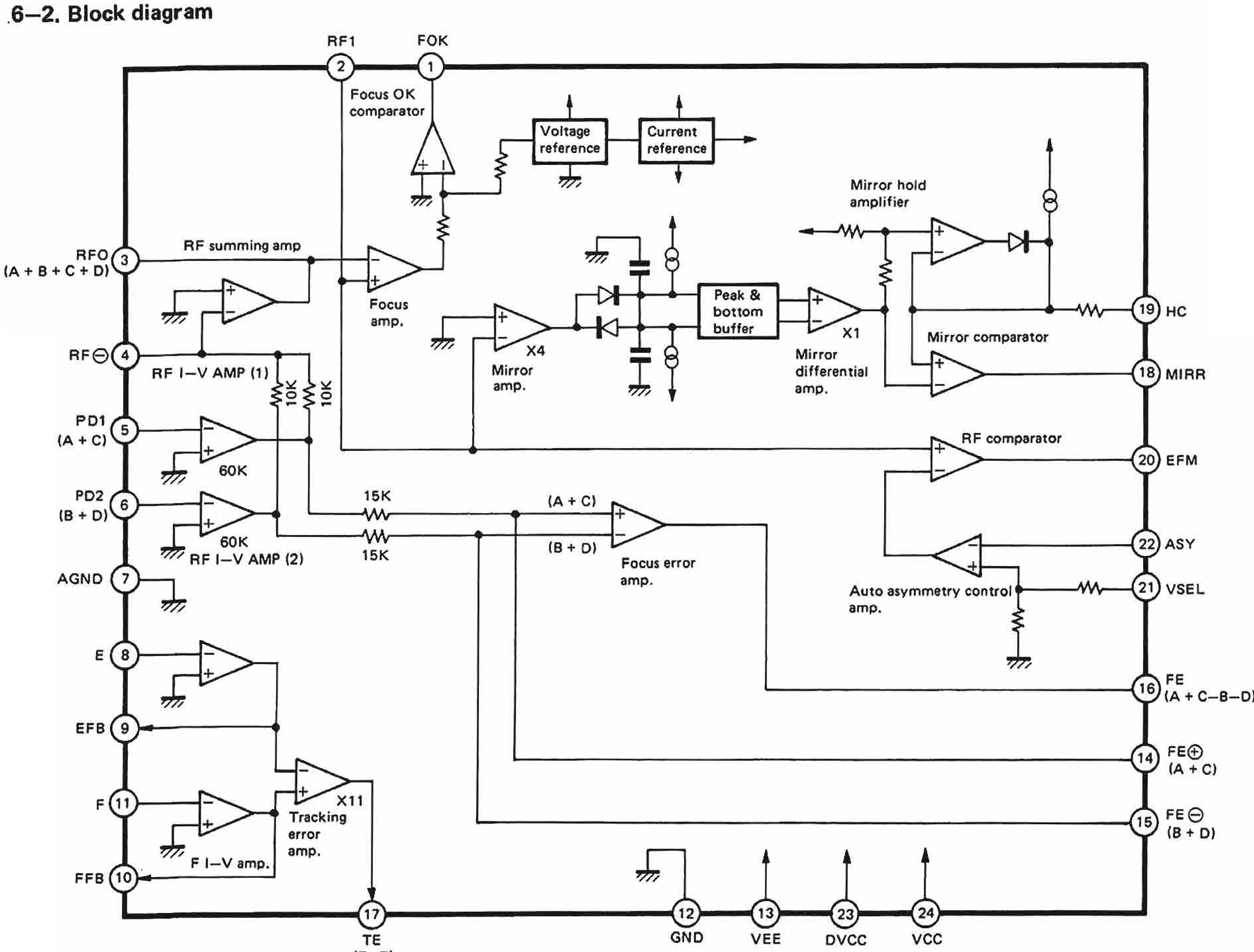


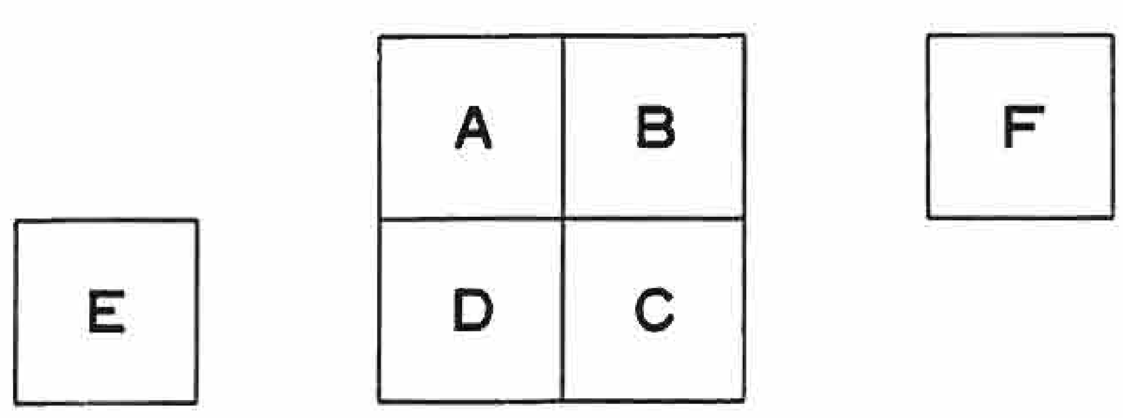
Fig. 6–2

6–3. Explanation of functions of components

Terminal No.	Terminal name		Functions	DC volt
1	FOK	O	Focus, servo permit output. Active at comparator output "H". Connection of load resistance (PNP open collector).	0V
2	RFI	I	The output of the RF summing amplifier is coupled with C10 : 0.01μF.	0V
3	RFO	O	RF summing amplifier output. EYE pattern test point.	VRFO
4	RF ⊖	I	RF summing amplifier inverted input. Connection of feedback CR to 3 – 4	0V
5	PD1	I	RF I–V amplifier (1) inverted input. Current input as connected to PIN diode B + D (Note 1).	0V
6	PD2	I	RF I–V amplifier (2) inverted input Current input as connected to PIN diode A + C (Note 1).	0V 0V
7	A GND	–	Small signal analog system GND.	
8	E	I	E I–V amplifier inverted input. Current input as connected to PIN diode E (Note 1).	0V
9	EFB	O	E I–V amplifier output. Connection of feedback CR to 8 – 9	0V
10	FFB	O	F I–V amplifier output. Connection of feedback CR to 10 – 11	0V
11	F	I	F I–V amplifier inverted input. Current input as connected to PIN diode F (Note 1).	0V
12	GND	–	GND	0V
13	VEE	–	Negative power supply.	–5V
14	FE ⊕	I	Focus error amplifier non-inverted input. Connection of low-pass RC.	0V
15	FE ⊖	I	Focus error amplifier inverted input.	0V
16	FE	O	Focus error amplifier output. Connection of feedback CR to 15 – 16	VFEO
17	TE	O	Tracking error amplifier output.	VTEO
18	MIRR	O	Mirror output comparator output (active at "H"). Connection of laod resistance (PNP open collector).	0V
19	HC	I	Mirror hold condenser (C11 : 0.032μF) connection terminal.	–2V
20	EFM	O	EFM output comparator output.	4.1V (OPEN)
21	VSEL	I	Terminal for setting reference input level of auto asymmetry control amplifier.	+ 5V
22	ASY	I	Auto asymmetry control input	–
23	DVcc	–	EFM comparator system positive power supply.	+ 5V
24	Vcc	–	Positive power supply.	

Table 6–1

Note 1 : Pattern of photodetector



CIRCUIT DESCRIPTION

6–4. Explanation of operation

● RF amplifier

The PIN diode current input to PD1, PD2 is subjected to I–V conversion with RF I–V amplifiers (1), (2) using equivalent input resistance of 60kΩ in each amplifier.

Further more, addition is made with the RF summing amplifier and (A + B + C + D) is output to the RFO. Check of the EYE pattern can be made at this terminal.

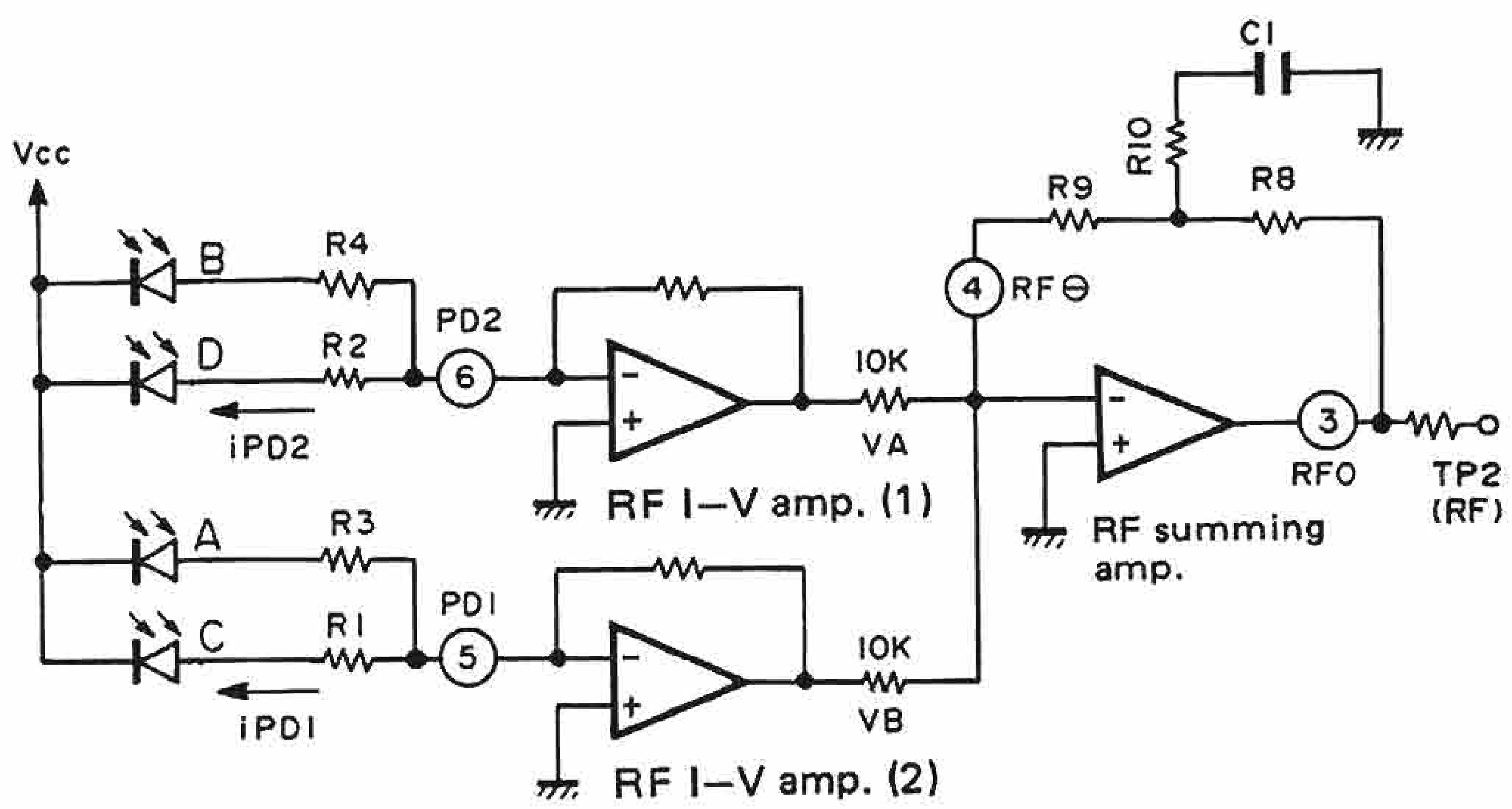


Fig. 6–3 RF I–V amplifier

● Focus error amplifier

The difference between output (B + D) of RF I–V amplifier (1) and output (A + C) of RF I–V amplifier (2) is obtained and (A + C)–(B + D) is output. C15,C16 are provided for preventing leakage of EFM component in the focus error output.

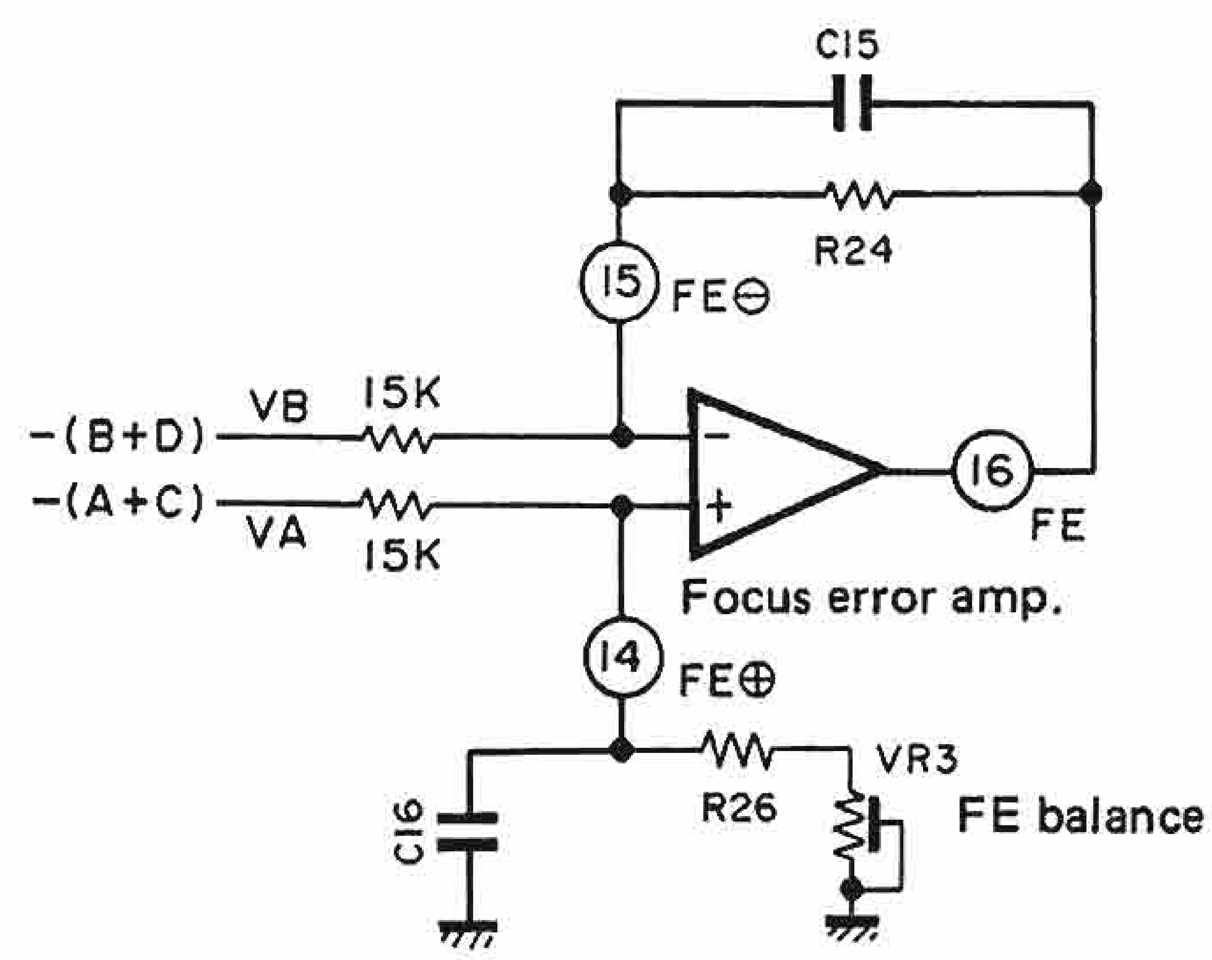


Fig. 6–4

● Tracking error amplifier

The PIN diode current input to E, F is subjected to I–V conversion with E, F I–V amplifiers using R2, VR1, R1 respectively. That is,

$V_D = I_E (R2 + VR1)$

$V_E = I_F\ R1$

is obtained. Further, the difference between E, F I–V amplifiers is obtained with the tracking error amplifier, and output (E–F) is obtained. The gain of the tracking error amplifier is 11 (21dB), and

$V_{TE} = (V_E - V_F) \times 11 = (i_E - i_F) \times (R12 + VR4) \times 11$

is obtained. C3,C4 are provided for preventing leakage of EFM component to the tracking error output.

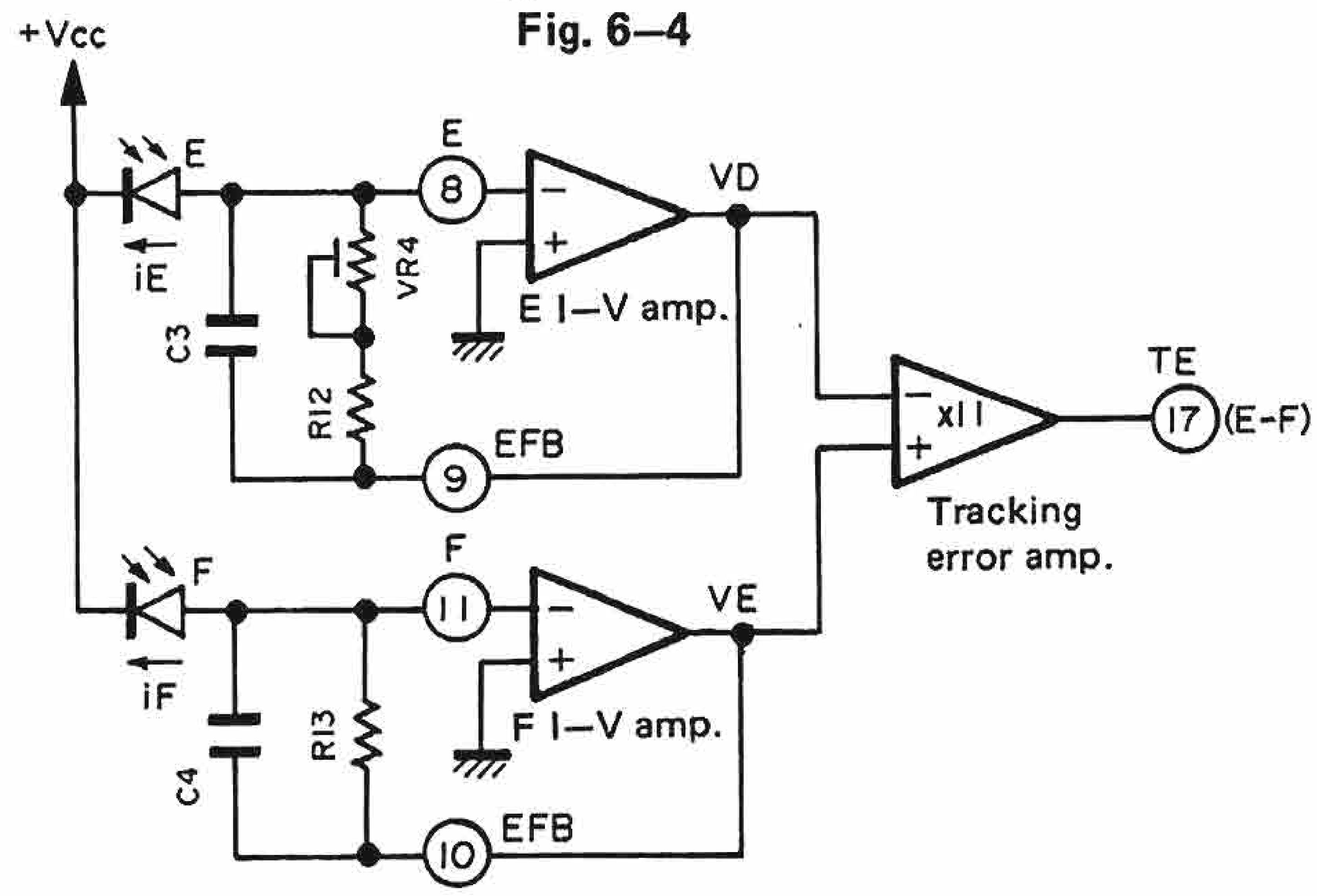


Fig. 6–5

● Focus OK circuit

It is the focus circuit that produces a window of the timing to turn ON the focus servo from focus search status.

Threshold value VTH of the focus OK comparator is inverted with VG = –0.4V, and consequently, the focus OK comparator is inverted when V_{RFO} = VC = 0.4V.

C6 devides the time constants of HPF of the EFM comparator, mirror circuits and L.P.F. of the focus OK amplifier. fc = 1.5kHz is obtained when C6 = 0.01μF, and thus worsening of the block error rate due to envelope defect of RF on a disc due to friction or alike is prevented.

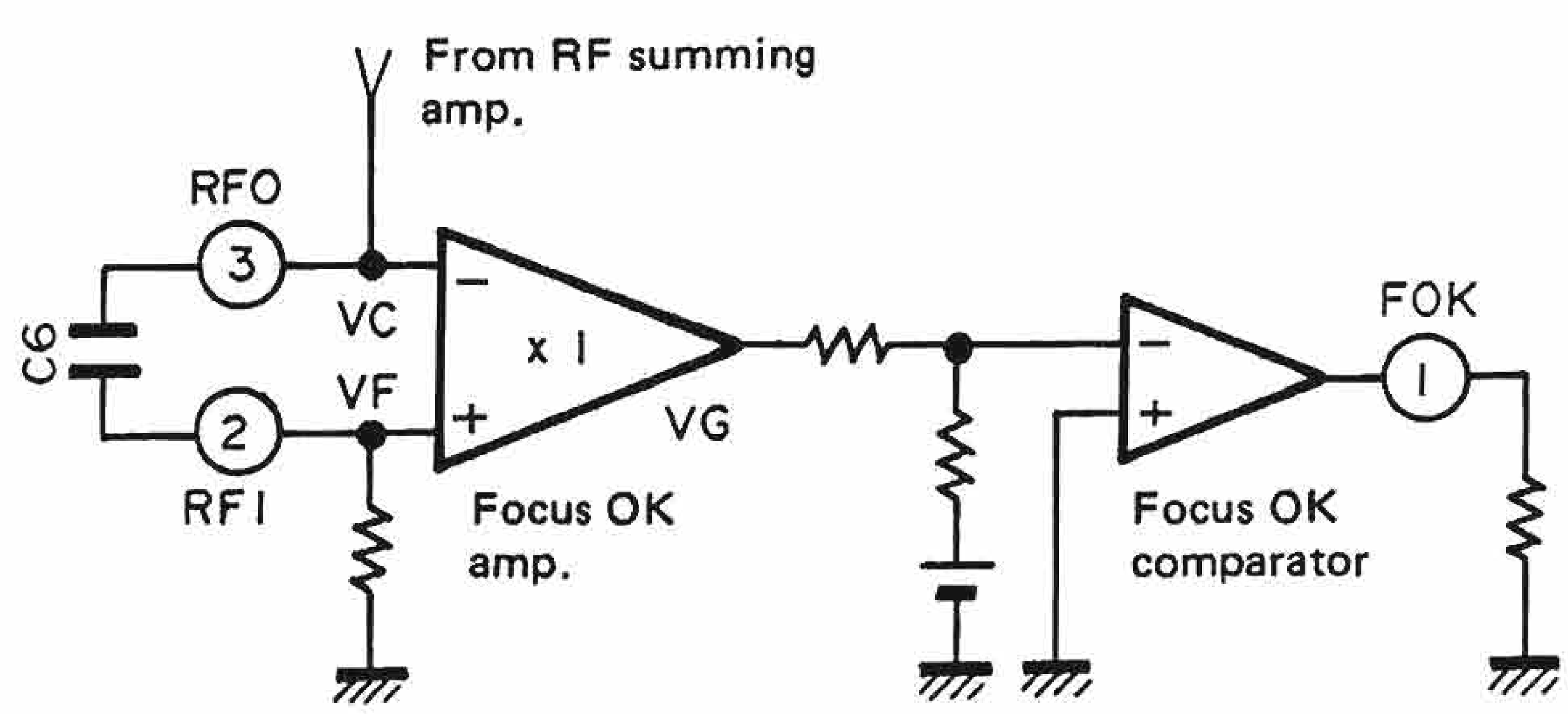


Fig. 6–6

CIRCUIT DESCRIPTION

- **Mirror circuit**

Peak and bottom hold is made after amplification of the RFI signal. Peak hold is held with a time constant that is capable of following traverse at 30kHz and bottom hold is held with a time constant that is capable of following envelope variation of rotational period.

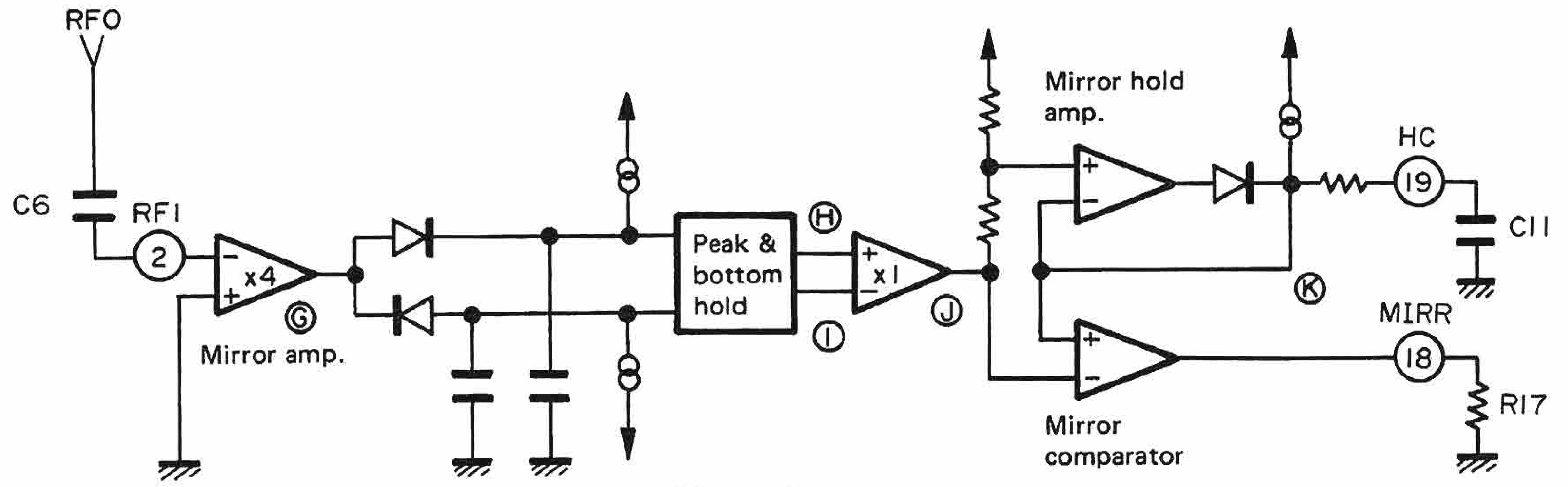


Fig. 6–7

DC regenerated envelope signal Ⓙ is obtained through difference amplifier between these peak/bottom hold signals Ⓗ and Ⓘ. The mirror output is obtained by comparing signal Ⓙ with signal Ⓚ, peak held at the level of 2/3 of the peak level. That is, the mirror output is "L" on a track of the disc, "H" between tracks (mirror portion) and "H" also when a defect is detected.

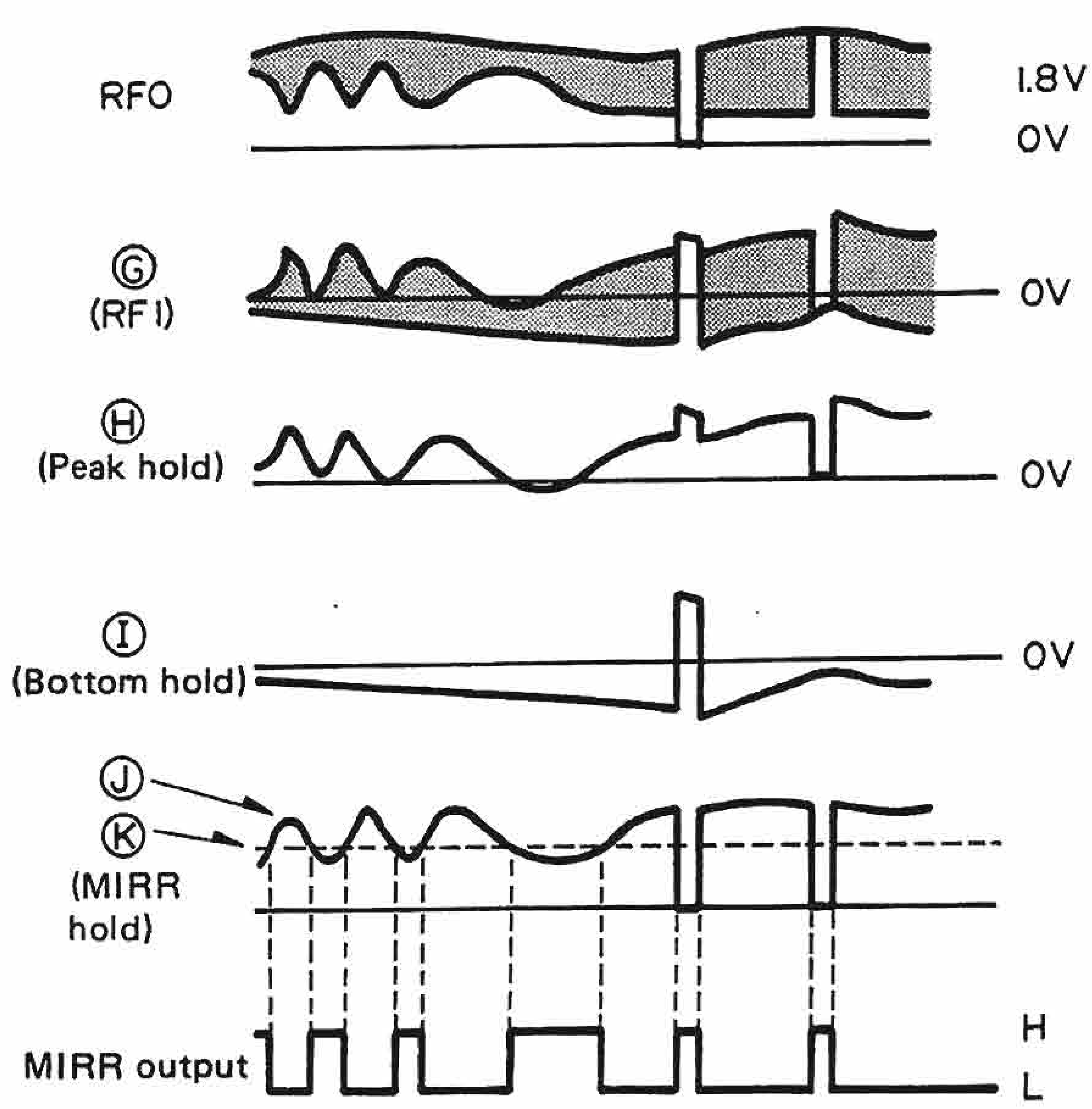


Fig. 6–8

- **EFM comparator**

The EFM comparator is used for binary-coding RF signals. As the asymmetry produced due to dispersion in the production of discs cannot be removed by AC coupling only, and therefore, the reference voltage of the EFM comparator is controlled by use of the fact, that probability of occurrence of I–O in binary-coded EFM signals is 50% each.

R16, C12 are L.P.F's for obtaining DC of + 2.5V, and they are for preventing worsening of the block error rate.

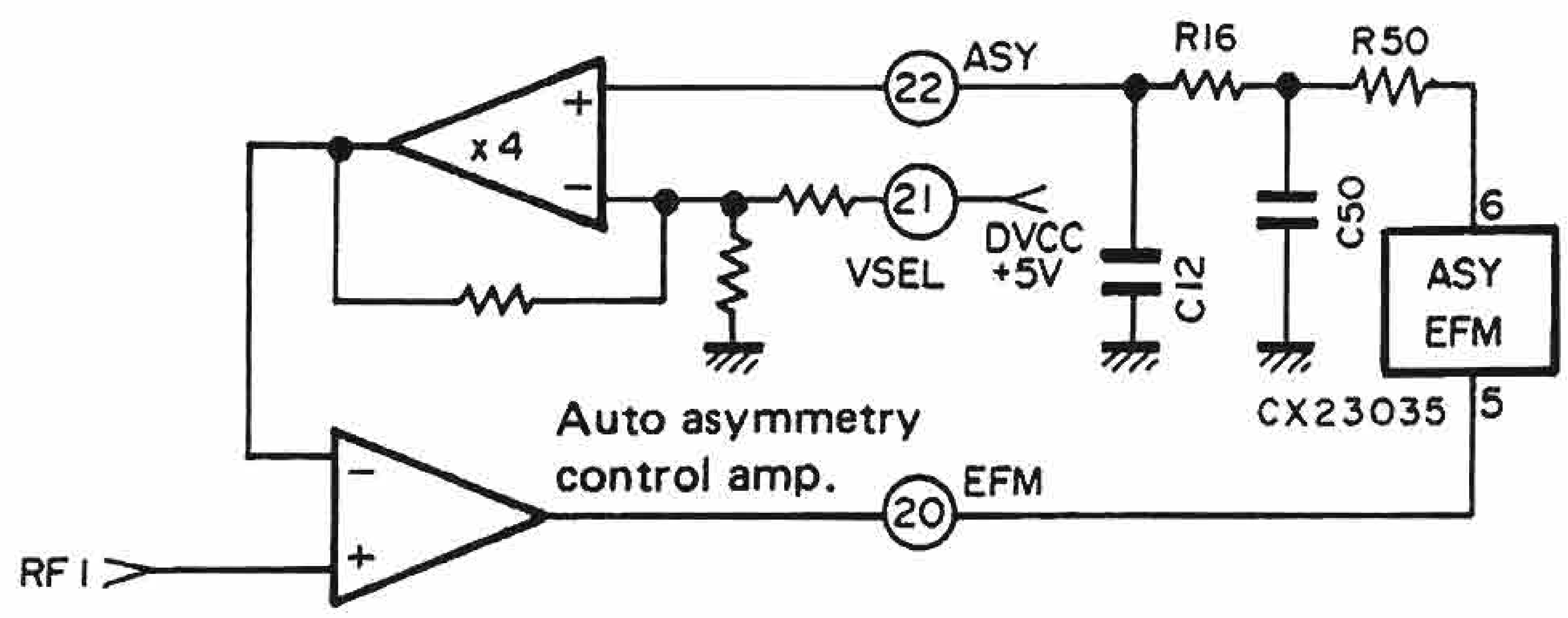


Fig. 6–9

CIRCUIT DESCRIPTION

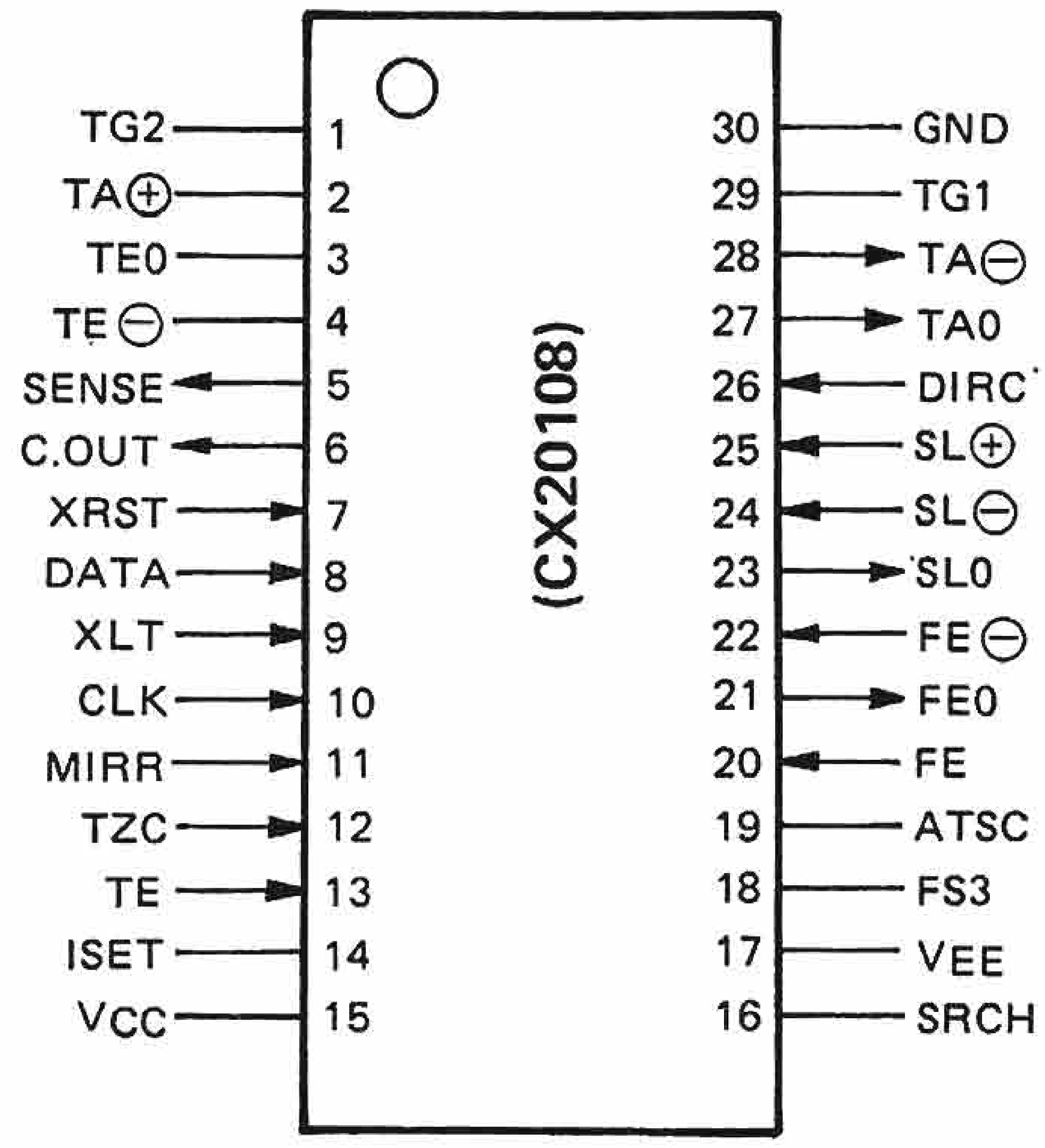
7. Servo signal processor (CX20108)

CX20108 is a bipolar IC developed for servo of compact disc (CD) players, and it provides the following functions.

- ○Focus control (search ON/OFF, gain control)
- ○Tracking control (servo ON/OFF, single track jump, multiple track jump, gain control, phase compensation control, brake circuit)
- ○Sled control (servo ON/OFF, fast forward, fast reverse)

Servo function of each of focus, tracking and sled as well as random access operation are realized through control by microcomputer. Furthermore, the serial data bus can be shared with CX23035.

7–1. Terminal connection diagram



7–2. Block diagram

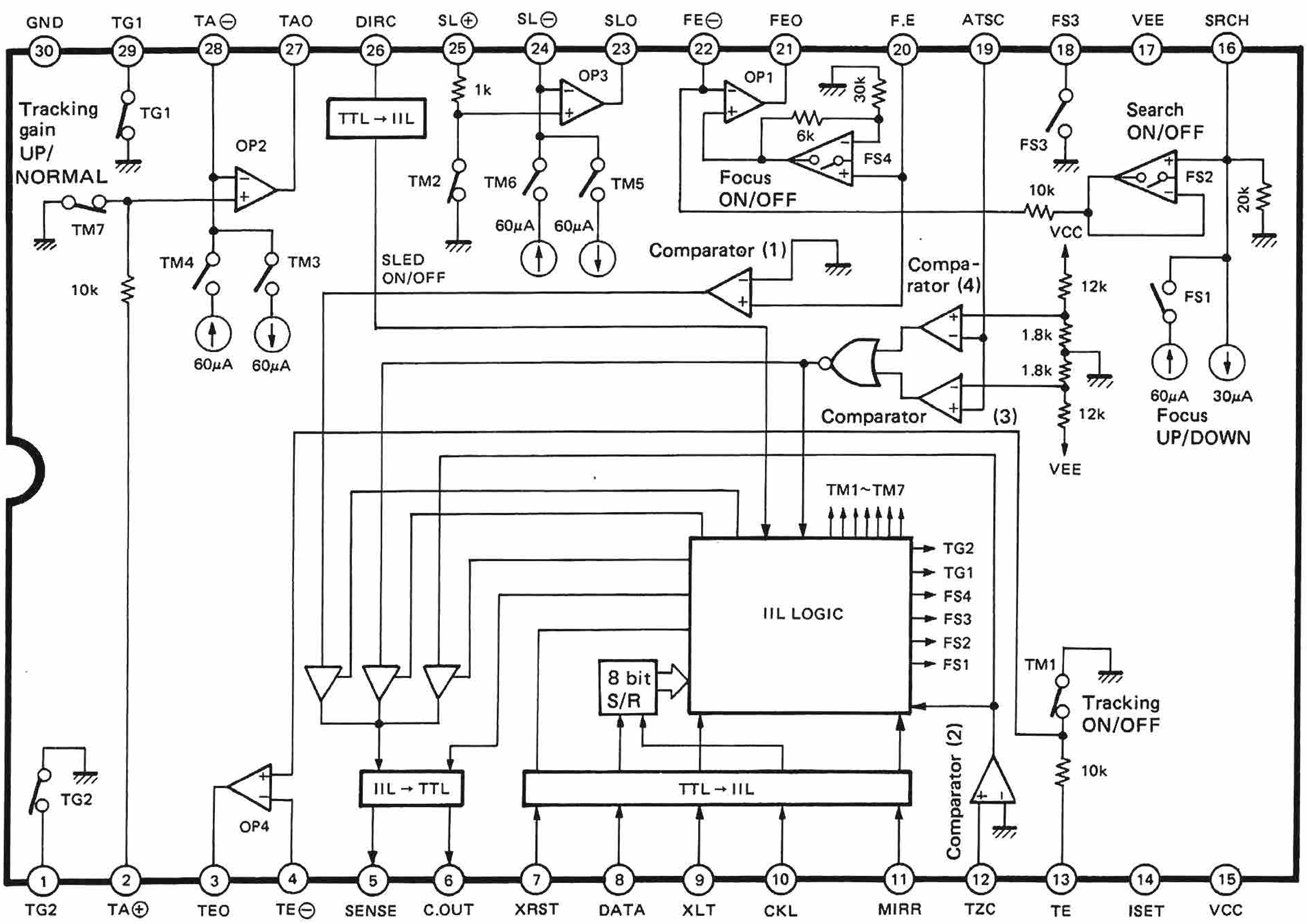


Fig. 7–2

CIRCUIT DESCRIPTION

7–3. Explanation of terminals

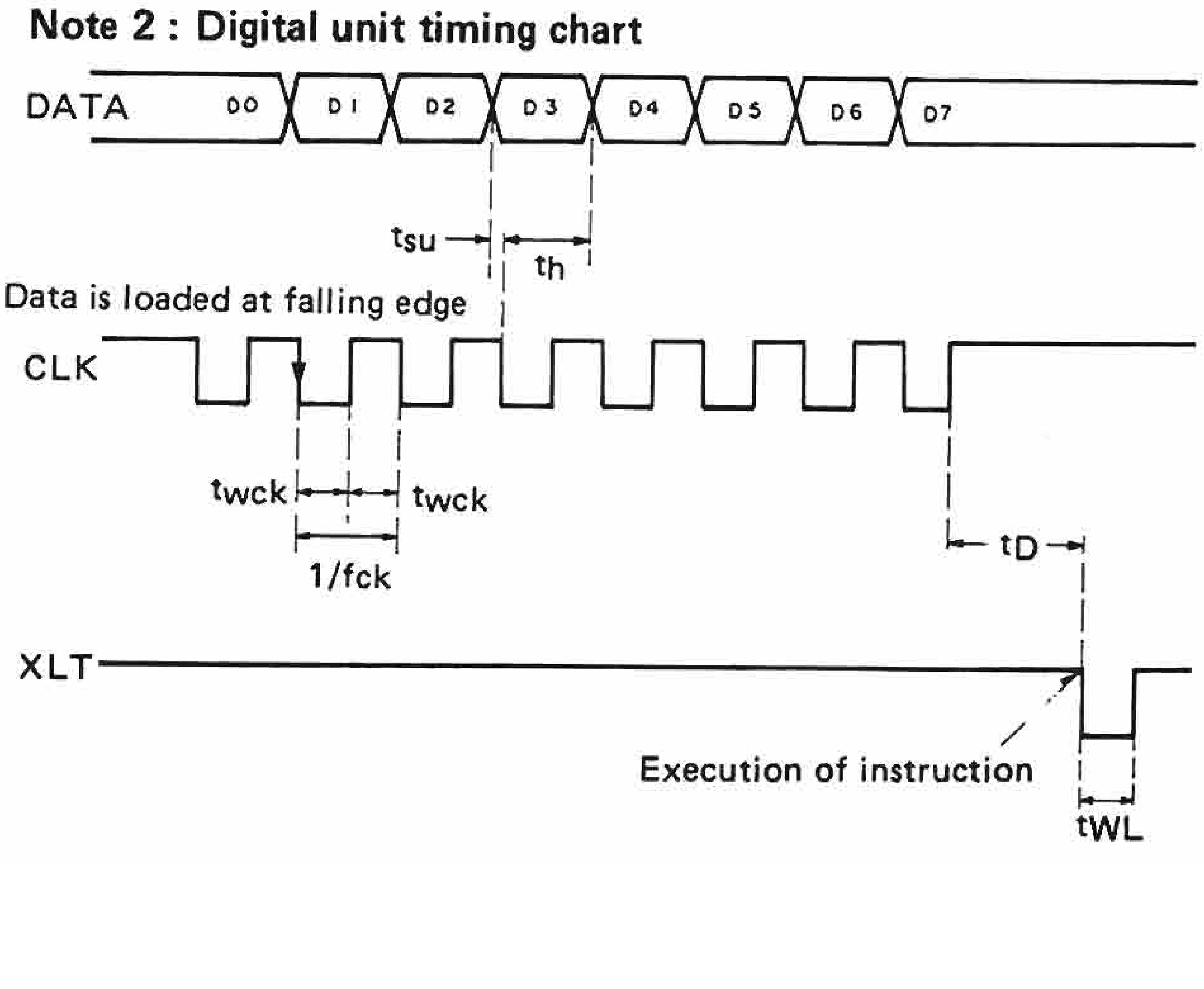
Terminal No.	Terminal name	I/O	Functions
1	TG2		Tracking amplifier gain switching terminal.
2	TA ⊕		Non-inverted input of operational amplifier 2.
3	TEO		Output of operational amplifier 4.
4	TE ⊖	O	Inverted input of operational amplifier 4.
5	SENSE	O	Output of SSP internal status that corresponds to ADDRESS of CPU → SSP. (Changes in accordance with ADDRESS content of internal serial register.) See Note 1.
6	C. OUT	O	Signal output for counting number of tracks at the time of high speed access.
7	XRST	I	All internal registers are cleared when CPU → SSP "L". Connected with CPU RESET. See Note 2.
8	DATA	I	Serial data transmission of CPU → SSP. Input is made from LSB. D0~D7.
9	XLT	I	Latch of serial data of CPU → SSP. (The contents of internal serial register are transmitted to each address decoded latch.) Transmission at "L". Change to "H" occurs immediately after execution because no edge trigger is produced.
10	CLK	I	CPU → SSP serial data transmission block. Data is read at falling edge. "H" level before and after transmission.
11	MIRR	I	Mirror signal input from RF amplifier.
12	TZC	I	Tracking error signal is input with C couple. The time constant is determined by one single track jump, but it is usually around 2kHz.
13	TE	I	Tracking error signal input.
14	ISET		Setting of current level for determining focus search voltage, tracking jump voltage and thread feed voltage.
15	Vcc		Power supply terminal. Normally –5V.
16	SRCH		The condenser for determining the time constant of charge/discharge waveform for focus search is connected.
17	VEE		Power supply terminal. Normally –5V.
18	FS3		Focus amplifier gain switching terminal. GND level.
19	ATSC		Such information that a mechanical shock was applied to the player is input. Simply, a tracking error is input through BPF. In this equipment it is connected to GND level and is not used.
20	FE	I	Input of focus error signal.
21	FEO	O	Output of operational amplifier 1.
22	FE ⊖	I	Inverted input of operational amplifier 1.
23	SLO	O	Output of operational output 3.
24	SL ⊖	I	Inverted input of operational amplifier 3.
25	SL ⊕	I	Non-inverted input of operational amplifier 3.
26	DIRC	I	Used at the time of one track jump. Normally "H". The direction of the track jump pulse is reversed with "L". Setting is made in the normal tracking mode by changing to "H". "L" for a fixed length of time with detection of activation, deactivation of TZC.
27	TAO	O	Output of operational amplifier 2.
28	TA ⊖	O	Inverted input of operational amplifier 2.
29	TG1		Tracking amplifier gain switching terminal.
30	GND		GND terminal of IC.

Note 1 : SENSE terminal output

Table 7–1

Serial data upper 4 bits	ADDRESS content	SENSE terminal output	Explanation
0 0 0 0	FOCUS CONTROL	FZC	"H" when focus zero cross. Focus erro voltage is 0V or higher. Used at the time of FOCUS PULL operation.
0 0 0 1	TRACKING CONTROL	AS	"H" when the ATSC input level exceeds the wind comparator level (VTH = ±Vcc x 13%). But this is not used in this equipment.
0 0 1 0	TRACKING MODE	TZC	Judgement output of positive or negative of tracking zero cross, tracking error. When used at the time of single track jump, DIRC is reduced to "L" on detection of TZC ↑, in FWD JUMP or on detection of TZC ↓ in REV JUMP.

Note 2 : Digital unit timing chart



7–4. System control

COMMAND	ADDRESS				DATA				SENSE
	D7	D6	D5	D4	D3	D2	D1	D0	
FOCUS CONTROL	0	0	0	0	FS4 FOCUS ON	FS3 GAIN DOWN	FS2 SEARCH ON	FS1 SEARCH UP	FZC
TRACKING CONTROL	0	0	0	1	ANTI SHOCK	BREAK ON	TG2 GAIN	TG1* SET	AS
TRACKING MODE	0	0	1	0	TRACKING* MODE		SLED* MODE		TZC

Table 7–2

GAIN SET* TG1, TG2 may be set independently.
In the case of ANTI SHOCK = 1 (00011XXX), both TG1, TG2 are inverted when ANTI SCHOCK = "H".

SLED MODE*

	D1	D0
OFF	0	0
SERVO ON	0	1
FWD MOVE	1	0
REV MOVE	1	1

TRACKING MODE*

	D3	D2
OFF	0	0
SERVO ON	0	1
FWD JUMP	1	0
REV JUMP	1	1

Note : The antishock circuit is not used in this equipment.

7–5. Serial data truth value table.

Serial data	Hexa-decimal	Function
FOCUS CONTROL		FS = 4321
00000000	S00	0000
00000001	S01	0001
00000010	S02	0010
00000011	S03	0011
00000100	S04	0100
00000101	S05	0101
00000110	S06	0110
00000111	S07	0111
00001000	S08	1000
00001001	S09	1001
00001010	S0A	1010
00001011	S0B	1011
00001100	S0C	1100
00001101	S0D	1101
00001110	S0E	1110
00001111	S0F	1111

Table 7–3

TRACKING CONTROL		D2	AS = 0 TG = 2 1	AS = 1 TG = 2 1
00010000	S10	0	0 0	0 0
00010001	S11	0	0 1	0 1
00010010	S12	0	1 0	1 0
00010011	S13	0	1 1	1 1
00010100	S14	1	0 0	0 0
00010101	S15	1	0 1	0 1
00010110	S16	1	1 0	1 0
00010111	S17	1	1 1	1 1
00011000	S18	0	0 0	1 1
00011001	S19	0	0 1	1 0
00011010	S1A	0	1 0	0 1
00011011	S1B	0	1 1	0 0
00011100	S1C	1	0 0	1 1
00011101	S1D	1	0 1	1 0
00011110	S1E	1	1 0	0 1
00011111	S1F	1	1 1	0 0

Table 7–4

TRACKING MODE		DC = 1 TM = 654321	DC = 1 654321	DC = 1 654321
00100000	S20	000000	001000	000011
00100001	S21	000010	001010	000011
00100010	S22	010000	011000	100001
00100011	S23	100000	101000	100001
00100100	S24	000001	000100	000011
00100101	S25	000011	000110	000011
00100110	S26	010001	010100	100001
00100111	S27	100001	100100	100001
00101000	S28	000100	001000	000001
00101001	S29	000110	001010	000011
00101010	S2A	010100	011000	100001
00101011	S2B	100100	101000	100001
00101100	S2C	001000	000100	000011
00101101	S2D	001010	000110	000011
00101110	S2E	011000	010100	100001
00101111	S2F	101000	100100	100001

Table 7–5

DC : DIRC input terminal

CIRCUIT DESCRIPTION

7–6. Explanation of functions

The input data for causing this IC to operate is composed of 8 bits. It is hereinafter expressed in two hexadecimal digits like $XX. (X is 0~F.)

Instructions to CX20108 are generally divided into three types, i.e., $0X, $1X and $2X. Standard methods for use of these three types are explained below.

- **$0X (⑤ SENSE is "FZC")**

This instruction is related to control of focus servo, and its bit composition is as follows.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	FS4	FS3	FS2	FS1

Four switches, i.e., FS1~FS4, are what are related to focus, and they correspond to D0~D3 respectively.

1) FS1, FS2 and focus search

The operation of FS1, FS2 is described next. ㉑, ㉒ etc. in Fig. 7–3 indicate terminal numbers of CX20108 (same hereinafter) OP1 is the operational amplifier for focus servo and the output of FS2 is connected to its inversion terminal. FS2 is such a switch that is ON and works as a usual voltage follower at the time of 1; and that its output is of high impedance at the time of 0. FS1 is a simple current switch which is OFF at the time of 1 and works to allow flow of 60μA at the time of 0. This value of 60μA is what is obtained when 240μA is fed to ISET ⑭ terminal. The voltage for focus search is produced using these FS1, FS2.

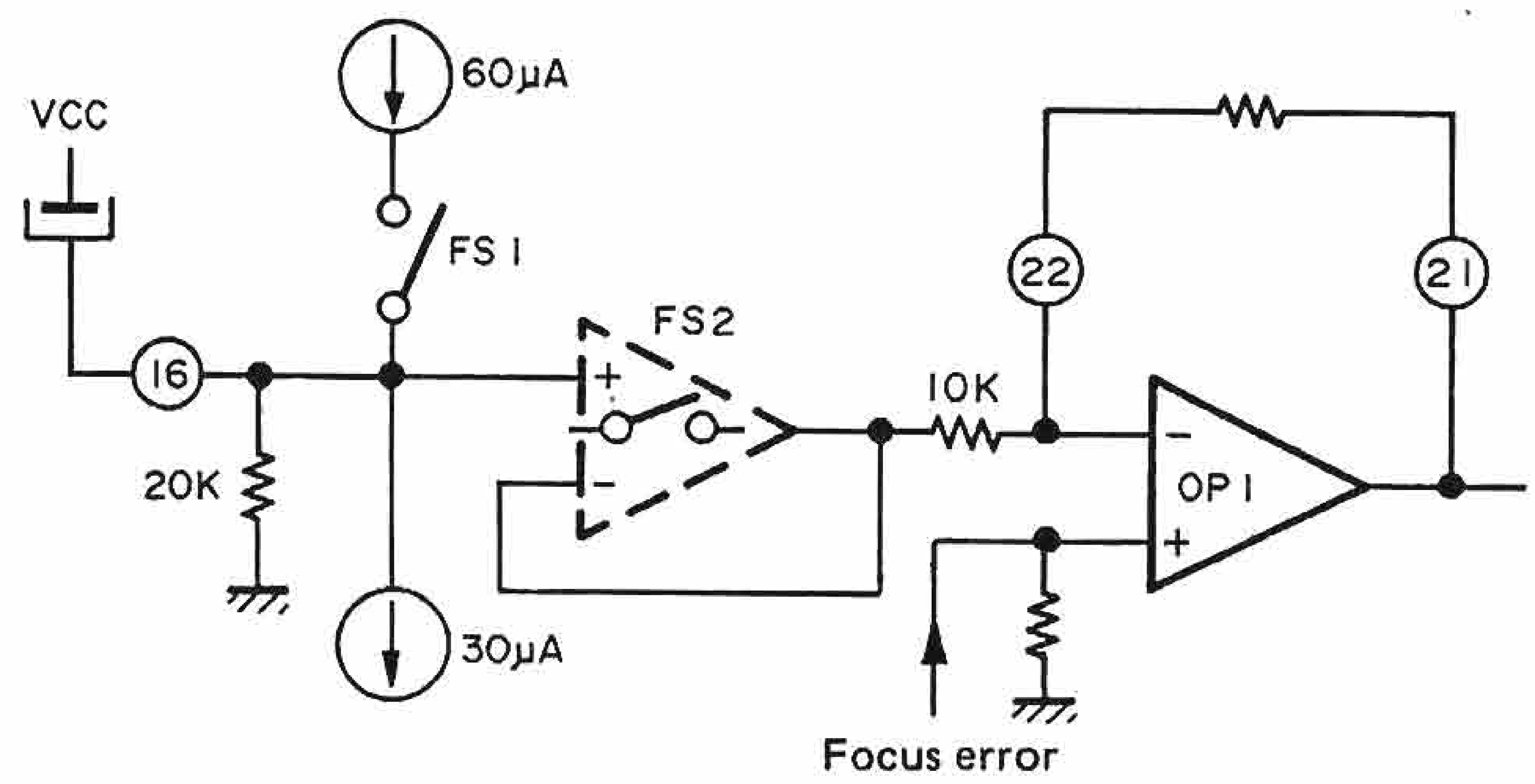


Fig. 7–3 Explanation of FS1, FS2

I $00 ⑯ terminal is charged to (60μA–30μA) x 20kΩ = 0.6V when FS1 = 0. Further, because FS2 = 0, This voltage is not transmitted thereafter, and ouput ㉑ terminal is of 0V.

II $02 FS2 only becomes 1 from the status described above. The output of FS2 is + 0.6V at this time and a negative output is directed to op2. This voltage level is specified as follows.

$$\underbrace{(60\mu A-30\mu A)}_{\uparrow}\times 20k\Omega \times \frac{\text{Resistance value between ㉑ – ㉒}}{10k\Omega} \quad \ldots\ldots \text{Expression (1)}$$

At the time of 240μA (⑭)

III $03 FS1 becomes 1 from the status described above and the current source of + 60μA is disconnected. Then, the CR's charge/discharge circuit is formed and the voltage at ⑯ terminal decreases as the time elapses as shown in Fig. 7–4.

This time constant is specified by internal 20kΩ and external capacitor C101 22μF.

It is possible to produce the focus serach voltage by alternately instructing these II and III. (Fig. 7–5)

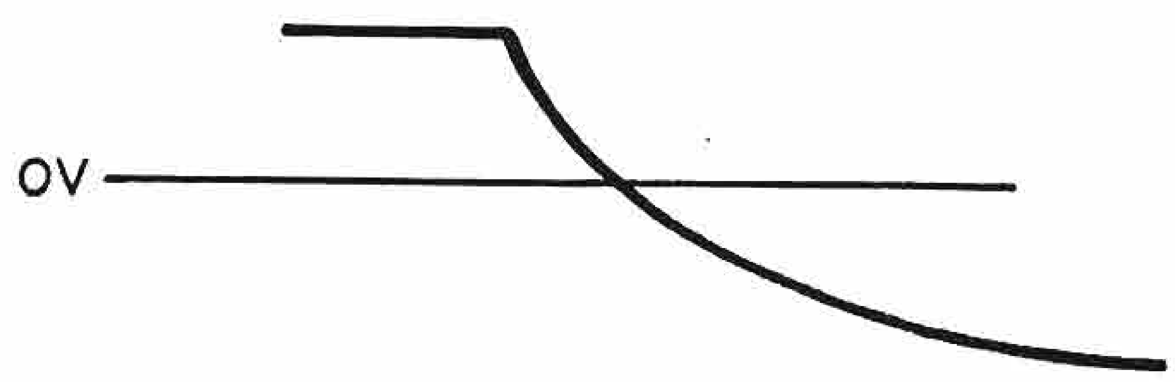


Fig. 7–4 Voltage at ⑯ terminal when FS1 = 0 → 1

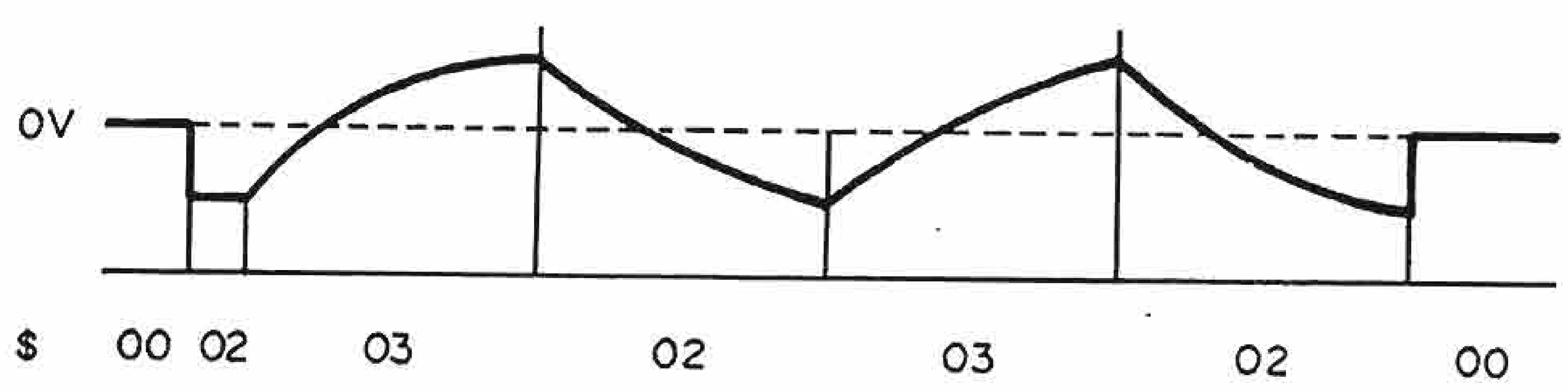


Fig. 7–5 Search voltage is produced by $02 ⇆ $03 (voltage at ⑯ terminal)

2) Explanation of FS4

This switch is a voltage follower (but the gain is 1.2 times) at the time of 1 and the output is open at the time of 0, like FS2 described earlier. This switch bears focus servo ON/OFF as located between focus error input 20 and input of OP1 described earlier.

$00 → $08

Focus OFF ← Focus ON

3) Focusing procedure

The polarity is specified as follows for explanation.

- The lens searches in the direction of far → near to the disc.
- Output voltage ㉑ changes as negative → positive at this time.
- Further, the S curve of focus changes as shown in Fig. 7–6.

Focus servo is applied with point Ⓐ shown in Fig. 7–6 as the actuation point. In general, the time when focus search is made and the focus servo switch is ON during passage through point Ⓐ. Furthermore, ANDing is made with focus OK signal (FOK) in order to prevent malopera-tion.

This IC is of such a design that what is obtained by comparing the focus error with 0V is output out of SENSE ⑤ terminal as the signal passing through point Ⓐ and is named as FZC (Focus Zero Cross).

Focus OK means a signal that indicates that focus is applied (may be applied, in this case), and it is output out of ① terminal of head amplifier IC1 (CX20109) in X29-1632-71.

When the above description is summarized, focus is applied in accordance with a timing chart is as shown in Fig. 7–7.

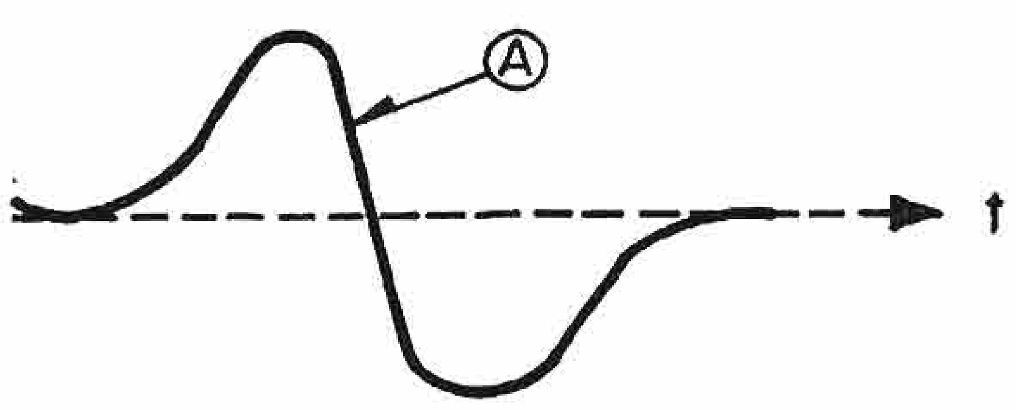


Fig. 7–6 S curve

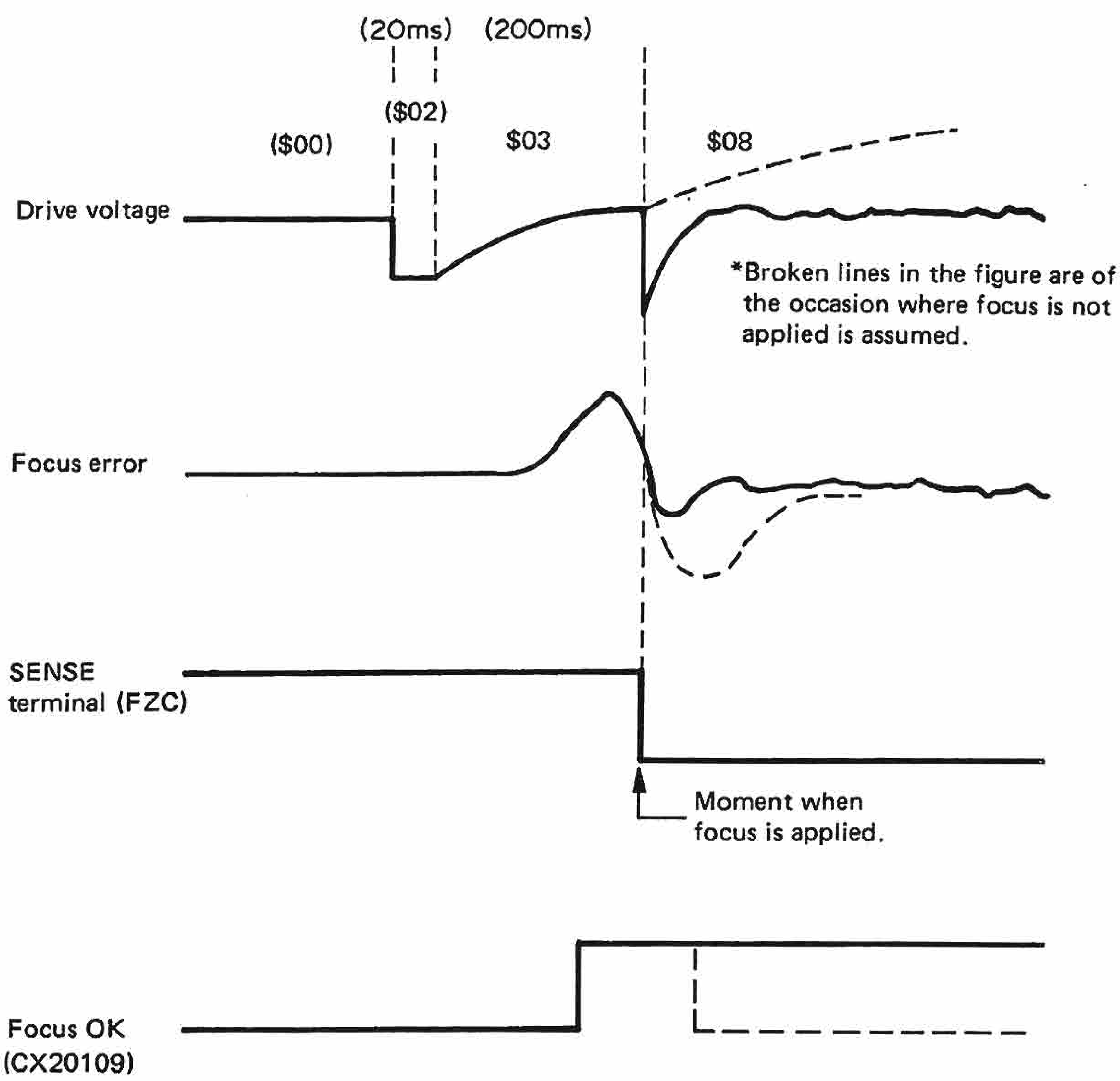


Fig. 7–7 Timing chart of focus OK

CIRCUIT DESCRIPTION

4) SENSE ⑤ terminal

As the output type is open collector of an NPN transistor, it is used with 22kΩ pull up. What is output varies by the input data. That is;

- FZC with $0X
- "H" when the absolute value of the voltage applied to AS terminal exceeds 0.65V, or "L" when it is up to 0.65V, with $1X.
- TZC with $2X

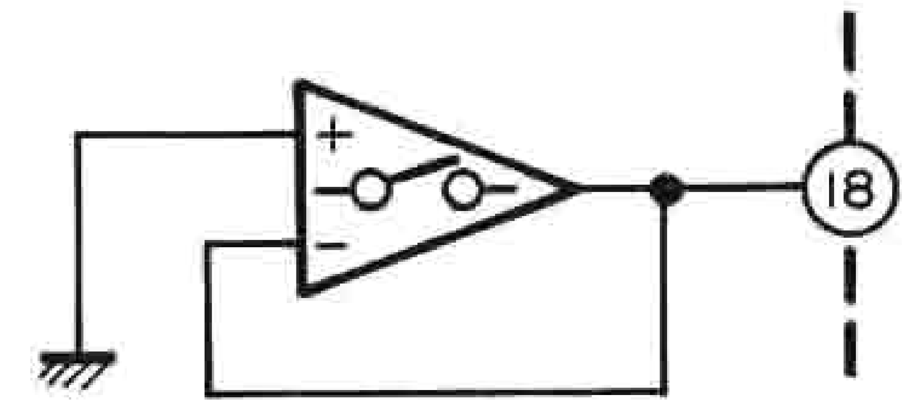


Fig. 7–8 FS3

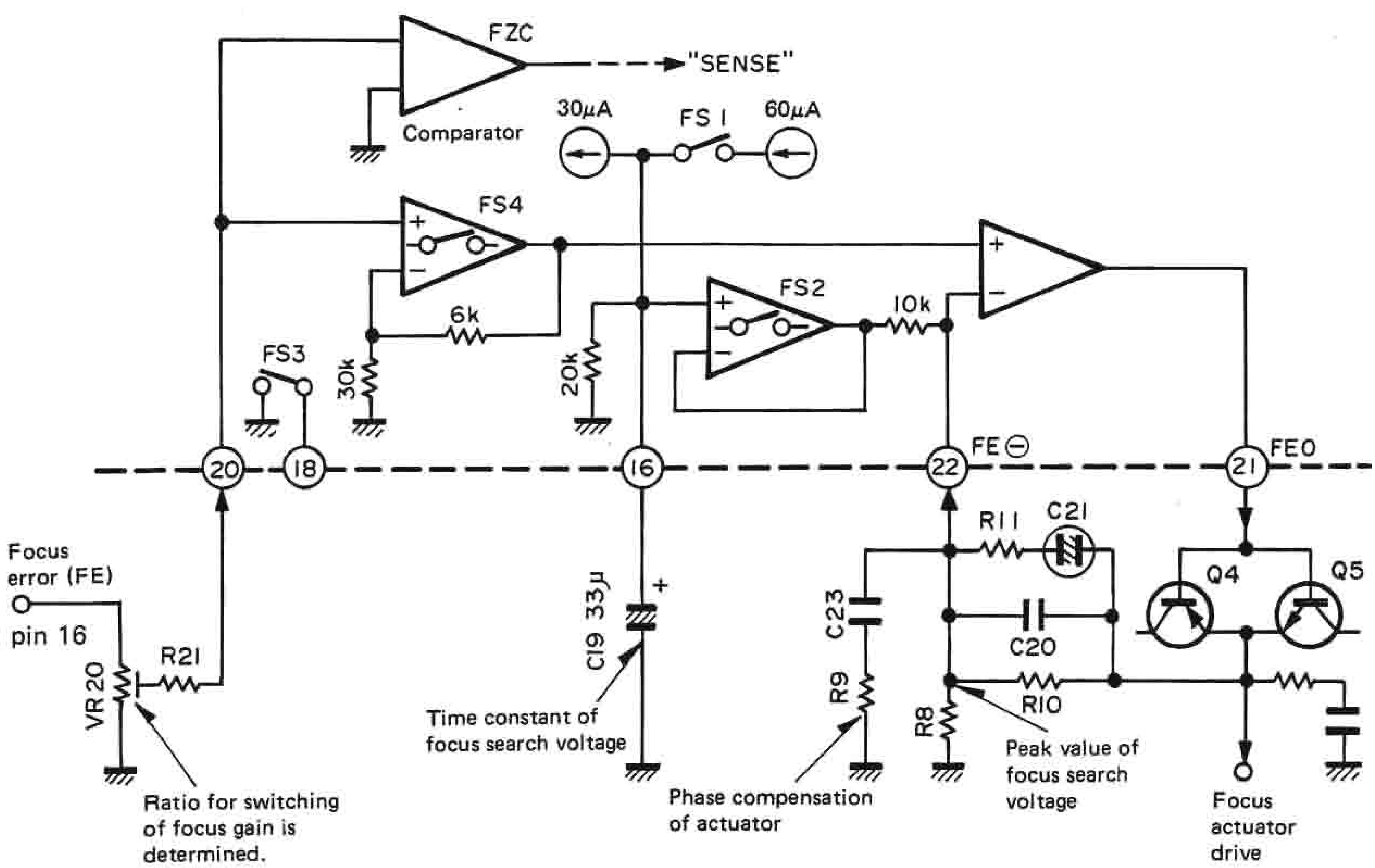


Fig. 7–9

- **$1X (⑤ SENSE is "AS")**

This instruction is related to TG1, TG2 and brake circuit ON/OFF. The bit composition is as follows.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1		Brake circuit ON/OFF	TG2	TG1

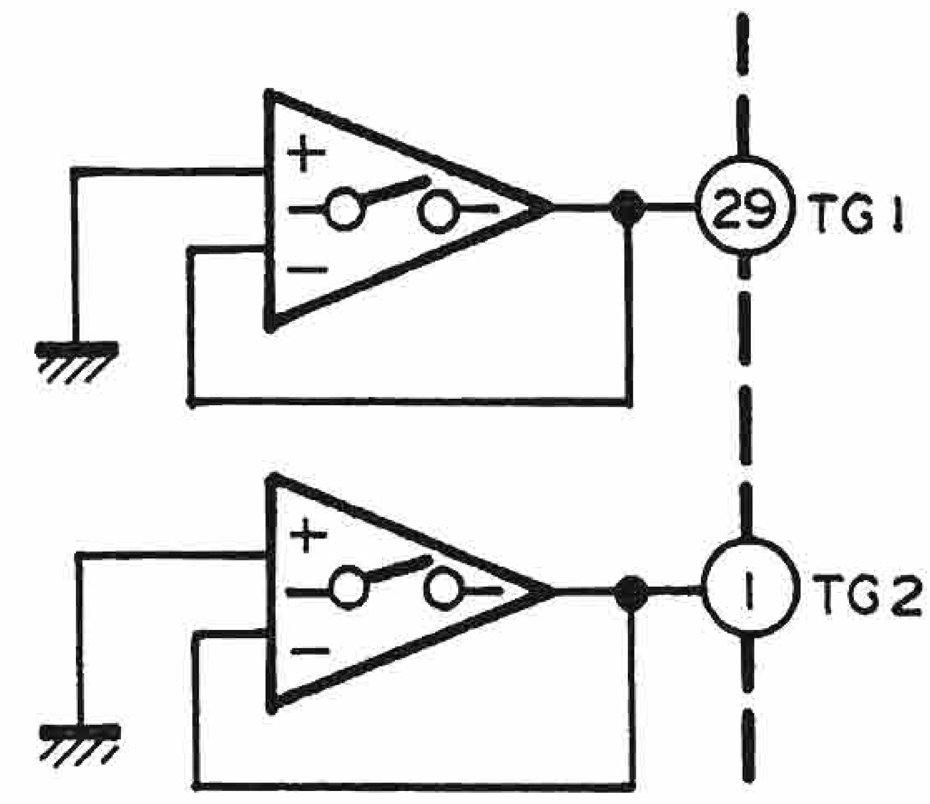


Fig. 7–10 TG1, TG2.

1) TG1, TG2

The circuit type of these switches is same as that of FS3 shown in Fig. 7–8. However, the logic is opposite. High impedance is obtained with 1, and GND level is obtained with 0. The purpose of the switch is switching between UP/NORMAL of the tracking servo gain. One switch is used for switching of the gain and another for switching of the phase. A typical circuit is shown in Fig. 7–11.

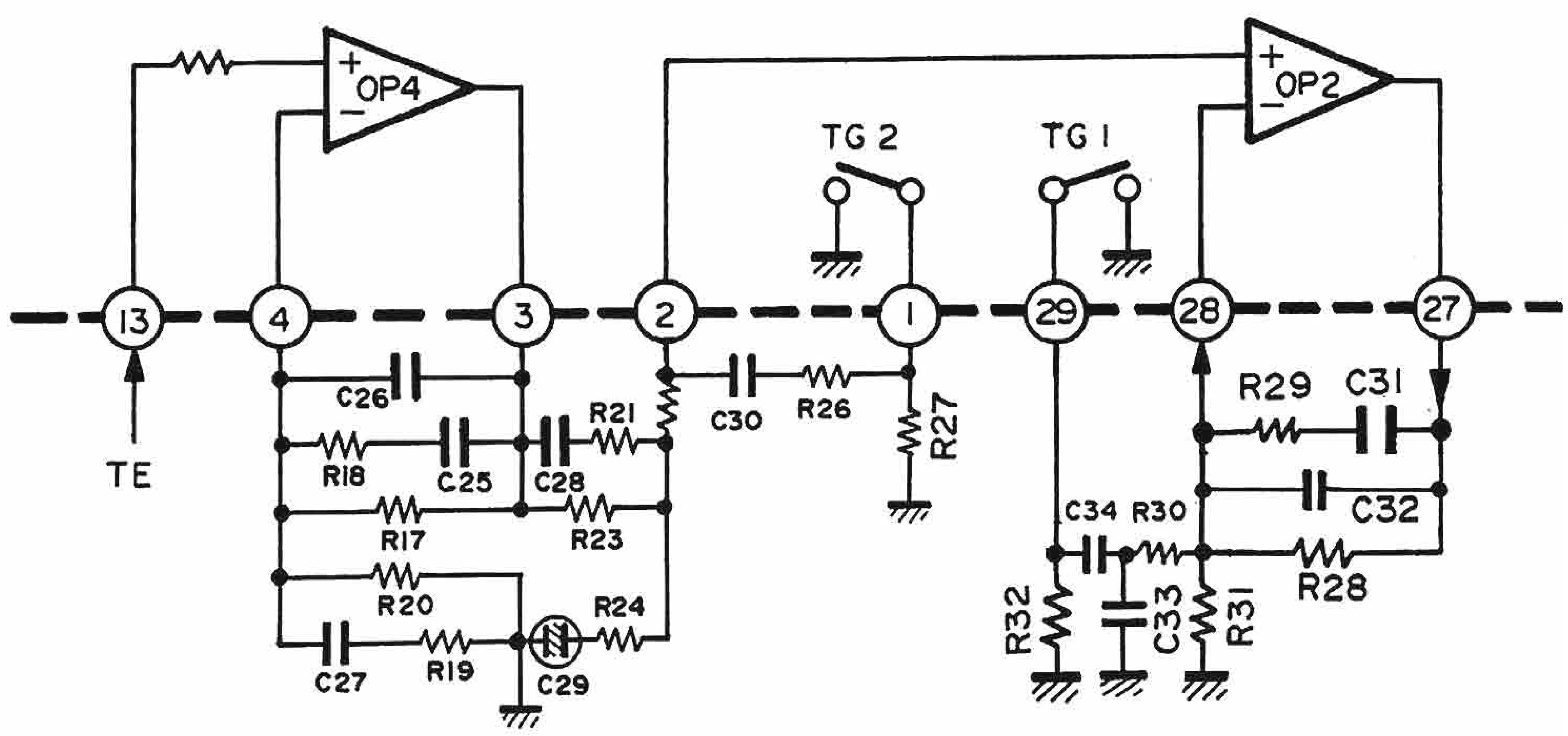


Fig. 7–11 Typical use of TG1, TG2

CIRCUIT DESCRIPTION

2) Brake circuit

The brake circuit is OFF (TM7 is open) when D2 = 0.

The brake circuit is ON (TM7 is open) when D2 = 1.

The brake circuit is explained next. See the section of 100 track jump and 10 track jump as for when the brake circuit is used.

The brake circuit is provided for preventing occurrence of such a phanomenon that only 10 tracks were jumped, even if it was intended to jump 100 tracks, due to the fact that setting of the actuator is exteremely inferior because the servo circuit exceeds the linear range after 100 track jump or 10 track jump. The phase relation between RF's envelope and tracking error is deviated by 180 degrees between the case where the actuator runs across tracks in the radial direction outward and the case where the same runs inward. The unnecessary portion of the tracking error is cut and brake is applied by making use of this nature, for improving setting of the actuator after track jump.

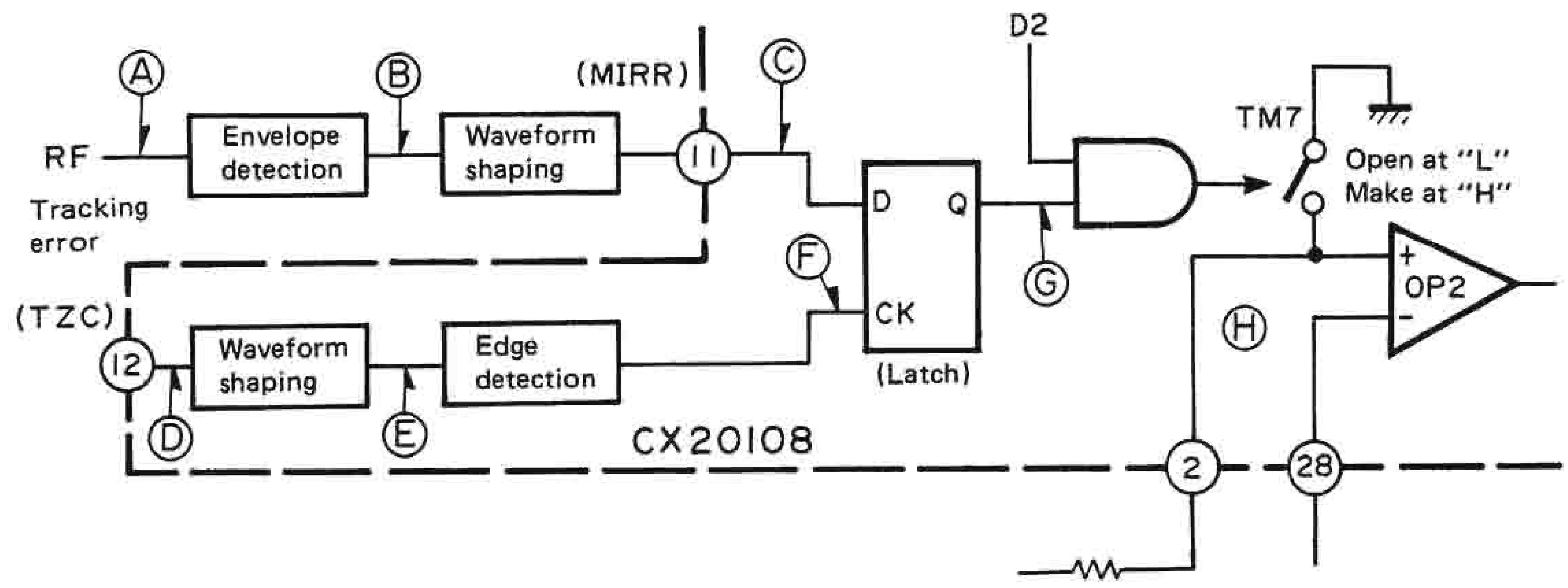


Fig. 7–12 Motion of TM7 (brake circuit)

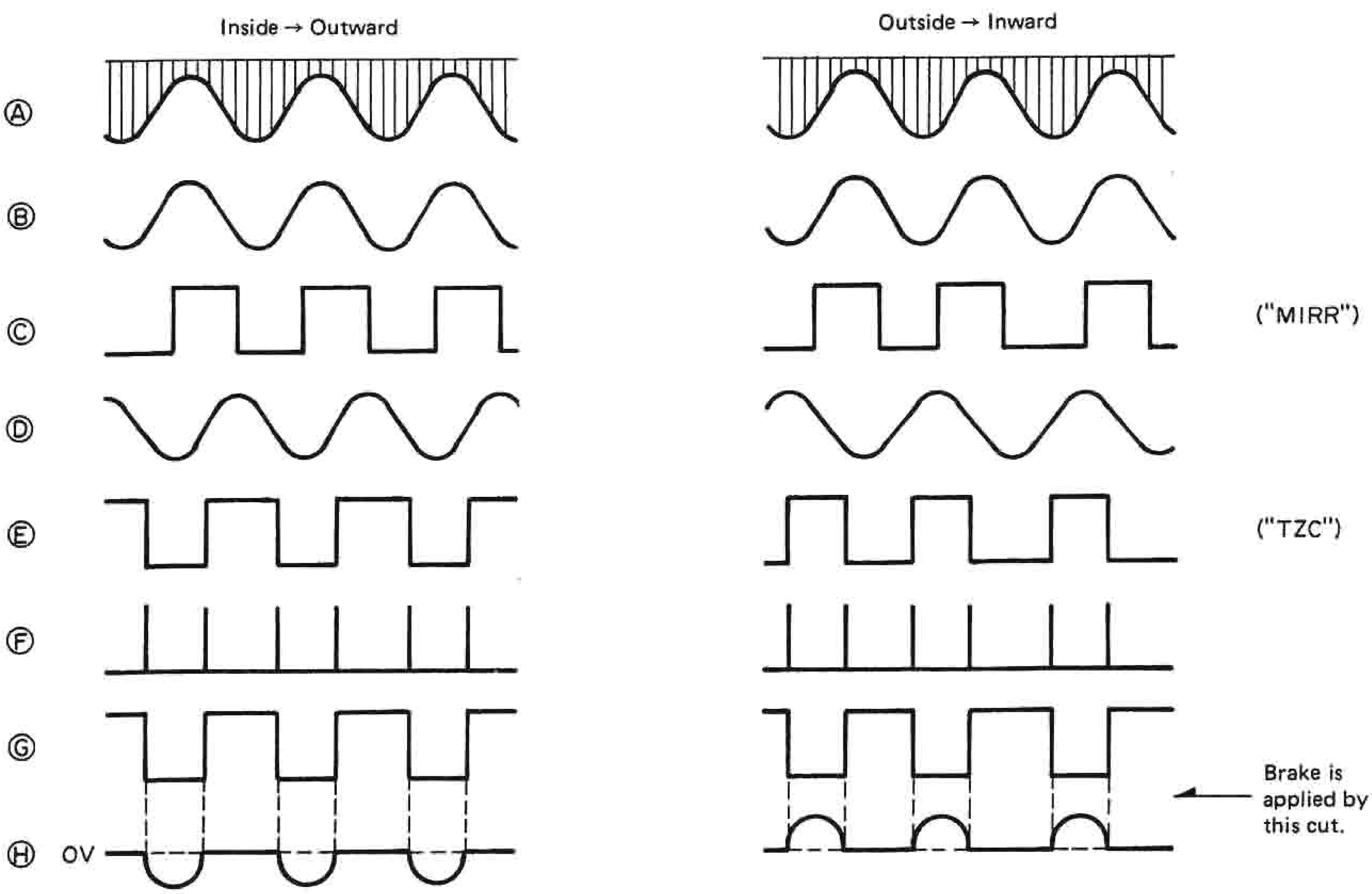


Fig. 7–13 Explanation of Fig. 7–12 (external waveform)

• $2X (⑤ SENSE is "TZC")

This instruction is related to production of jump pulse and fast feed pulse at the time of ON/OFF of tracking servo and sled servo and also at the time of access.

D7	D6	D5	D4	D3 D2	D1 D0
0	0	1	0	Tracking control 00 : OFF 01 : Servo ON 10 : F-jump 11 : R-jump ⇩ TM1, TM3, TM4	Sled control 00 : OFF 01 : Servo ON 10 : F-Fast feed 11 : R-Fast feed ⇩ TM2, TM5, TM6

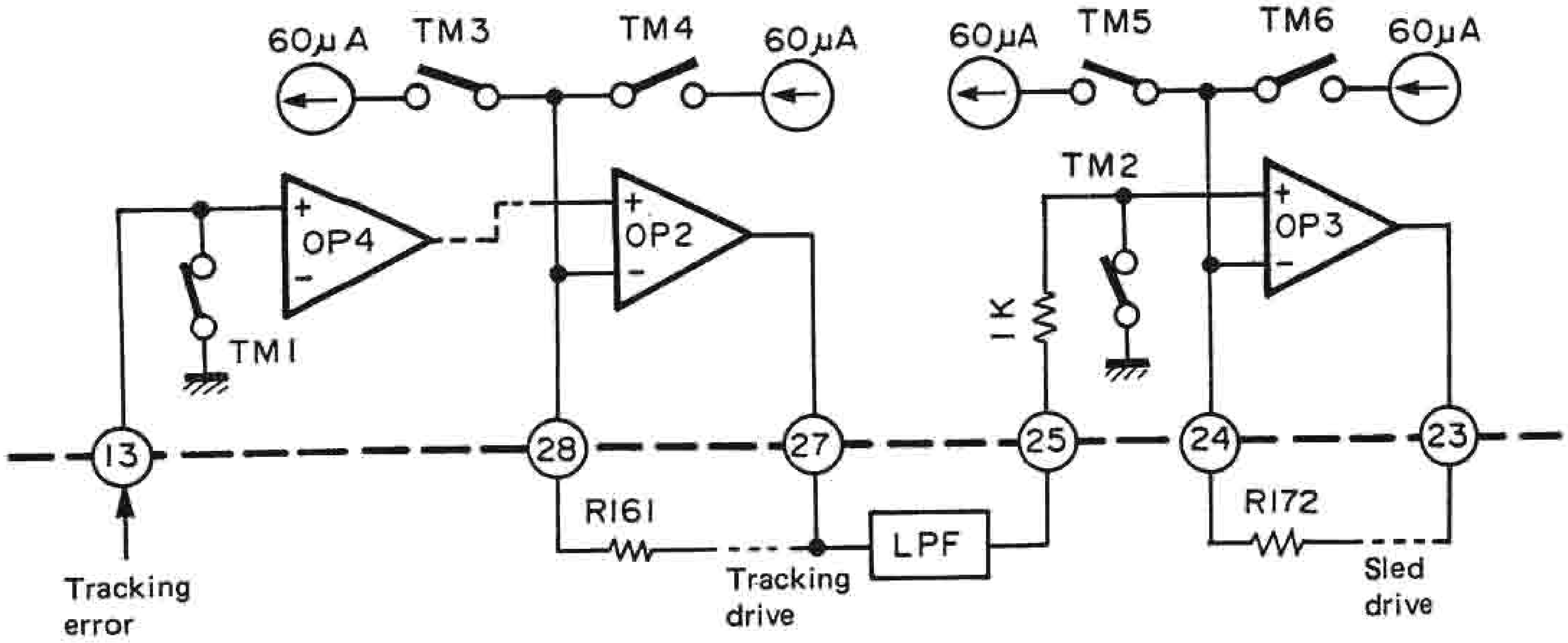


Fig. 7–14 TM1~TM7

The circuit composition is shown in Fig. 7–14. TM1, TM2 make servo ON/OFF, and TM3~TM6 produce jump pulse and fast feed pulse. See truth value table for details.

Figure 60μA is observed in Fig. 7–14. This value is of the case where 240μA is fed to ISET ⑭ terminal like SF1. The circuit of ⑭ terminal is as shown in Fig. 7–15. Therefore, the potential is around (–)VEE + 0.9V.

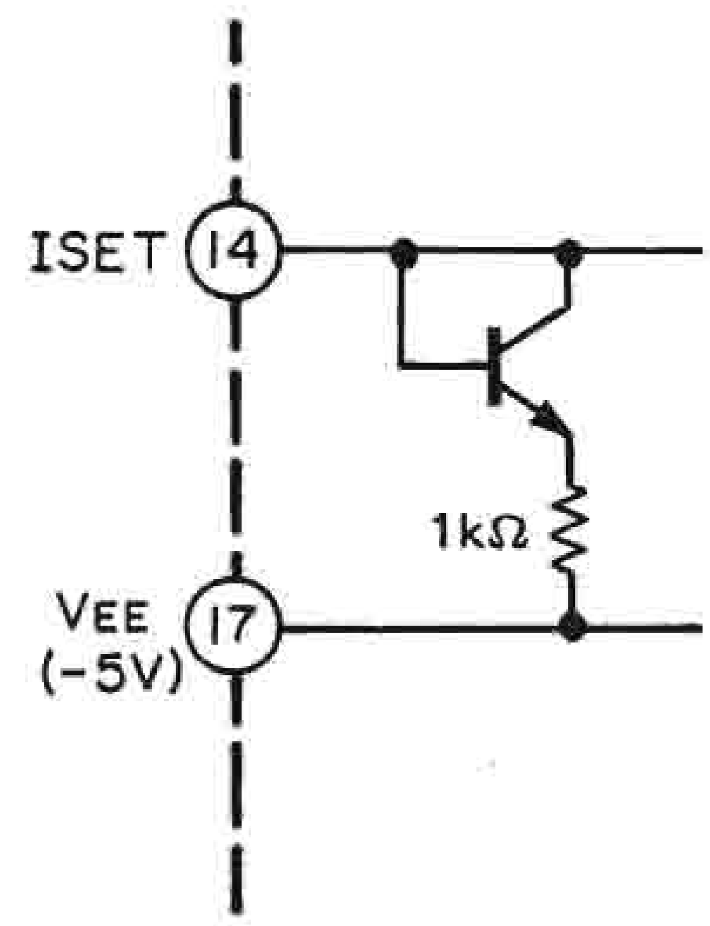


Fig. 7–15 ISET terminal

1) DIRC ㉖ terminal and single track jump

1 track jump usually gives an acceleration pulse, and then observes the tracking error; gives deceleration pulses for a fixed length of time from the time when the tracking error ran across 0 point, and again turns ON the tracking servo. 100 track jump to be explained in the next paragraph is satisfactory if approximately 100 tracks are jumped, but 1 track jump should be absolutely 1 track jump. Therefore, such a complicated measure is taken.

Therefore, DIRC (Direct Control) terminal is provided for this IC in order to facilitate single track jump by its operation. That is, for performing single track jump using DIRC (DIRC is usually "H")

- ○An acceleration pulse is produced. ($2C if REV; or $28 if FWD)
- ○DIRC is changed to "L" by TZC ↓ (or TZC ↑). (⑤ SENSE is "TZC".) The polarity of the jump pulse is inverted and deceleration is applied.
- ○DIRC is changed to "H" after a fixed length of time. Both tracking servo and sled servo are ON automatically.

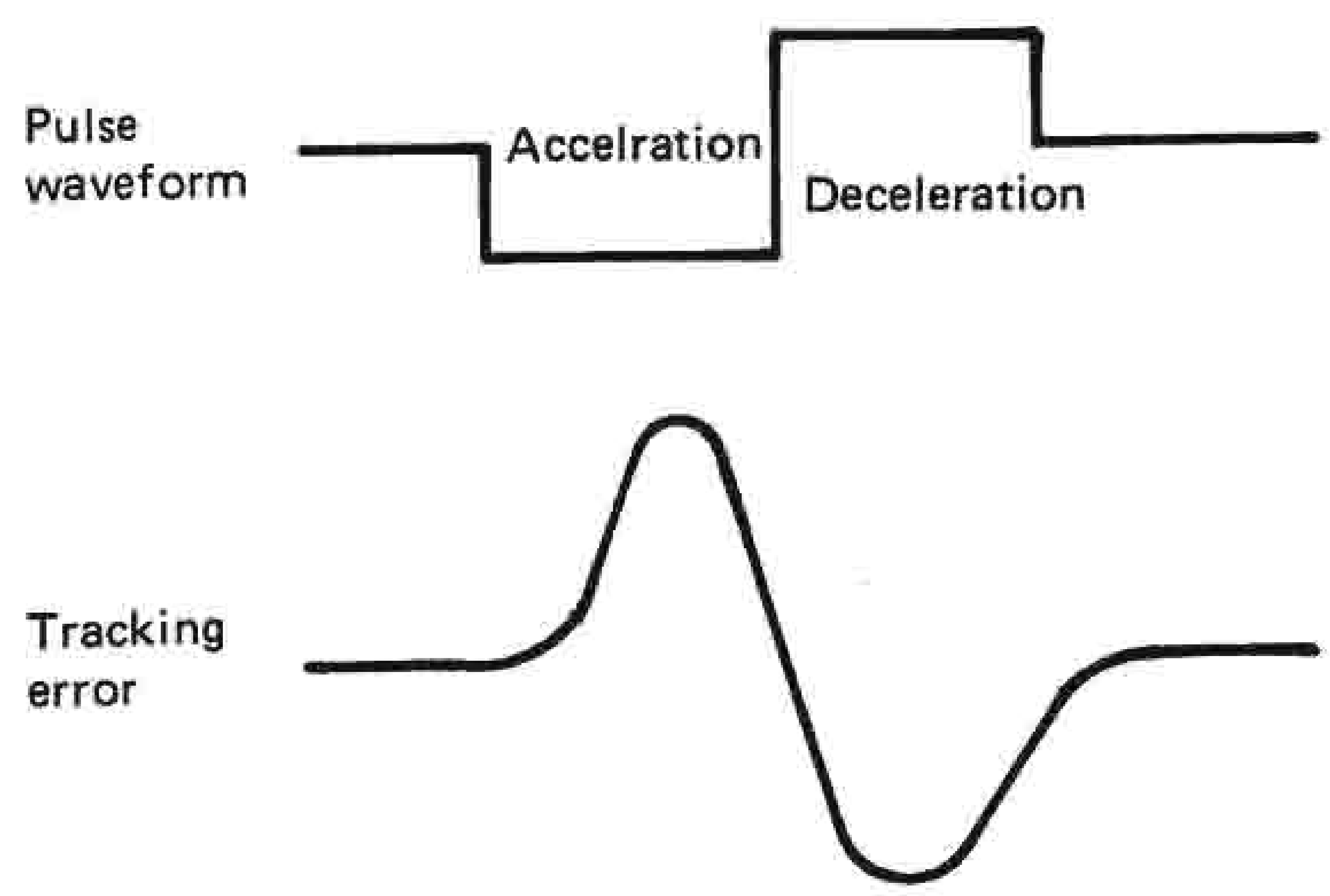


Fig. 7–16 Pulse waveform and tracking error of single track jump

2) 100 track jump

With this IC, basically it is not possible to change the amplitude of the jump pulse between 1 track jump and 100 track jump. (Because the value of the current input to ISET (14) terminal is fixed.)

Therefore, the amplitude is determined by 1 track jump and 100 track jump is controlled by time with the voltage remaining unchanged.

100 track jump is of smooth feed by jointly using sled fast feed (so-called "kick-off") besides drive of the tracking actuator. The length of this kick off is determined so that the access time is the minimum.

Brake circuit ON and tracking gain UP are made to stabilize the setting operation after the jump.

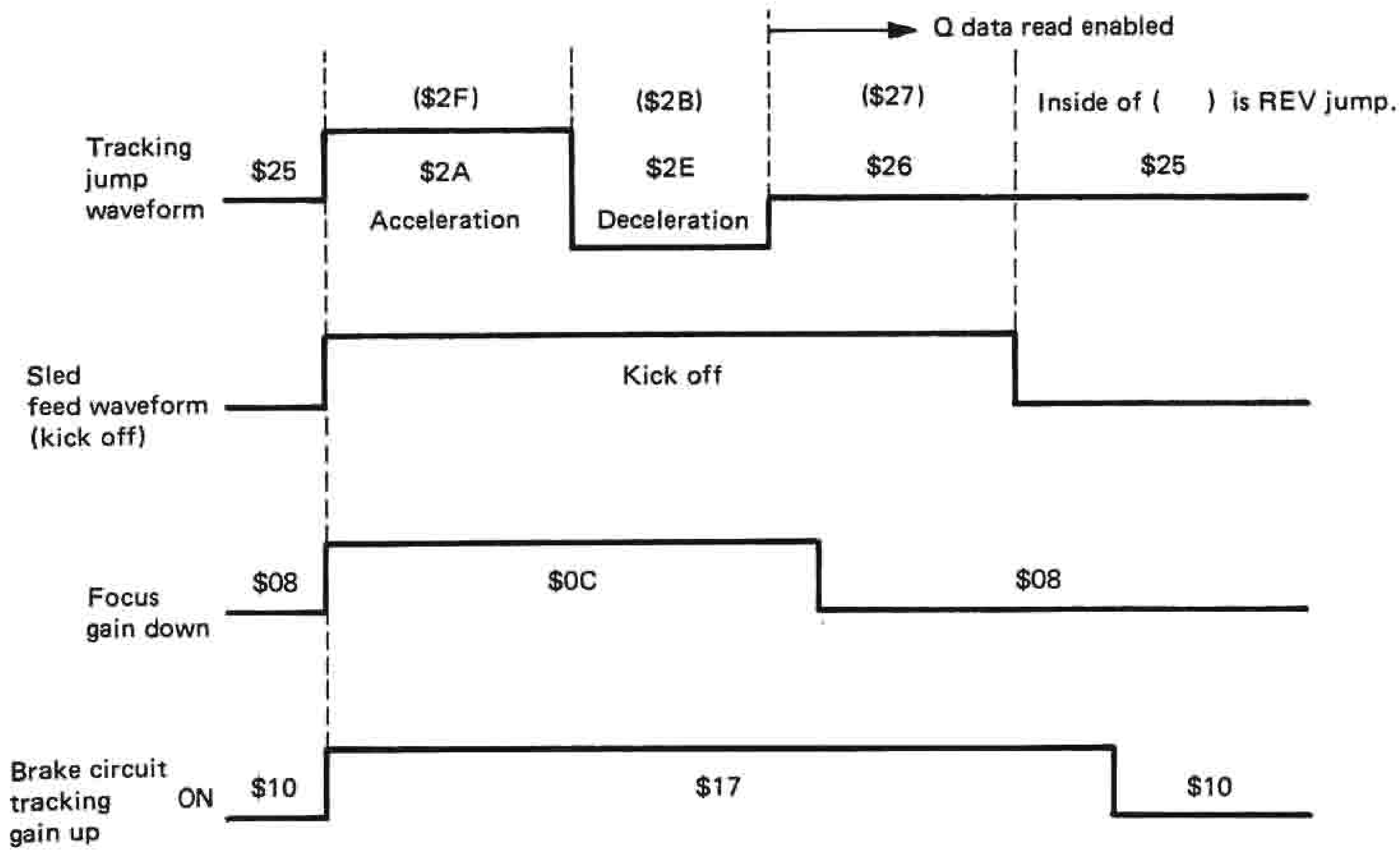


Fig. 7–17 100 track jump timing chart

3) 10 track jump

As this is intermediate between 100 and 1, the required number of tracks is set at a value that is close to 10, and therefore, the jump pulse width is determined by counting the number of jumped tracks.

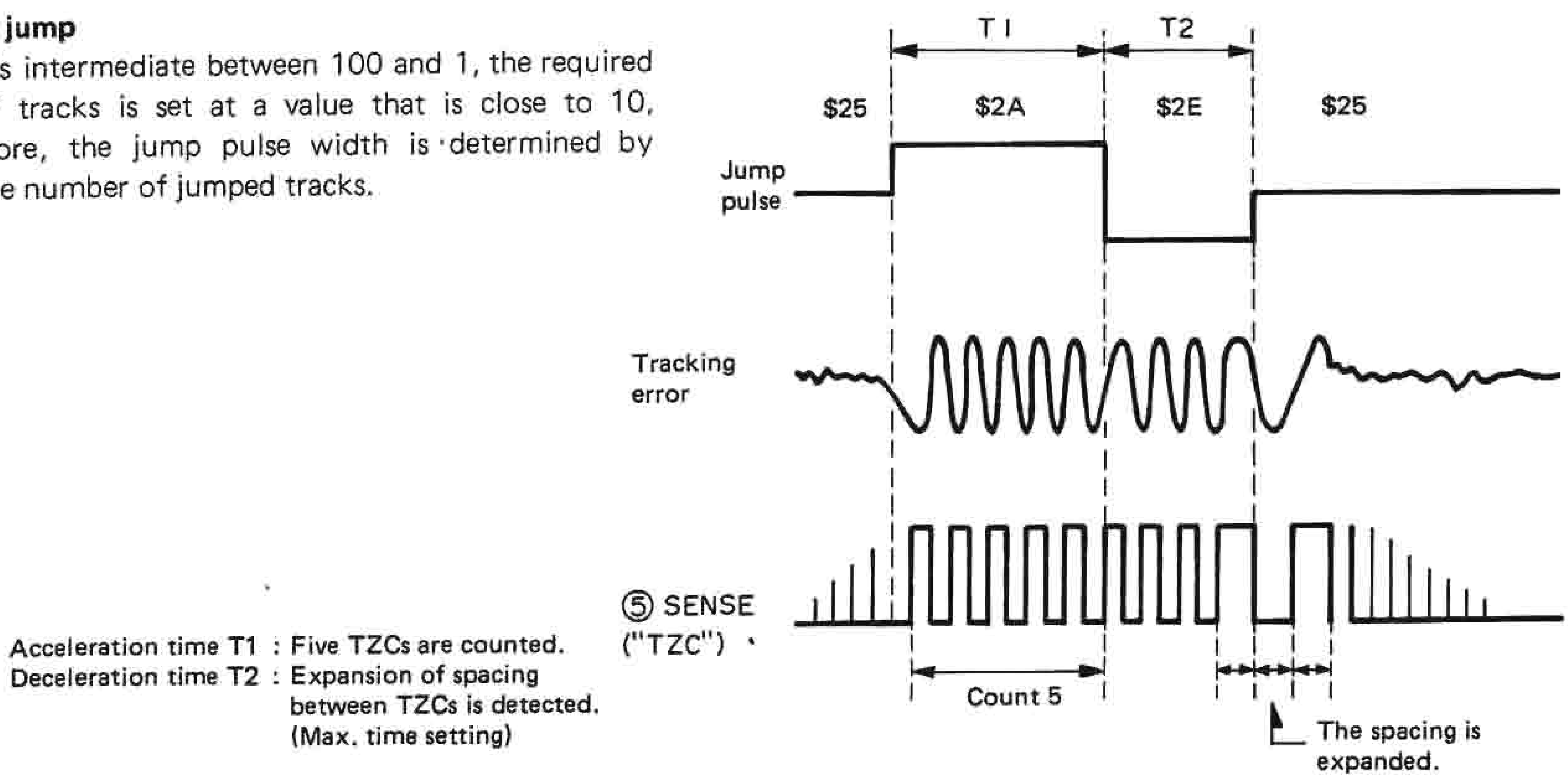


Fig. 7–18 10 track jump

4) Access by making joint use of 100, 10 and 1 track jumps

Jump pulses and kick off pulses (that is, $2X relaiton) are set as described in the paragraph of $2X and subsequent, and as for $1X relation, instructions are output in a batch, as shown in Fig. 7–19.

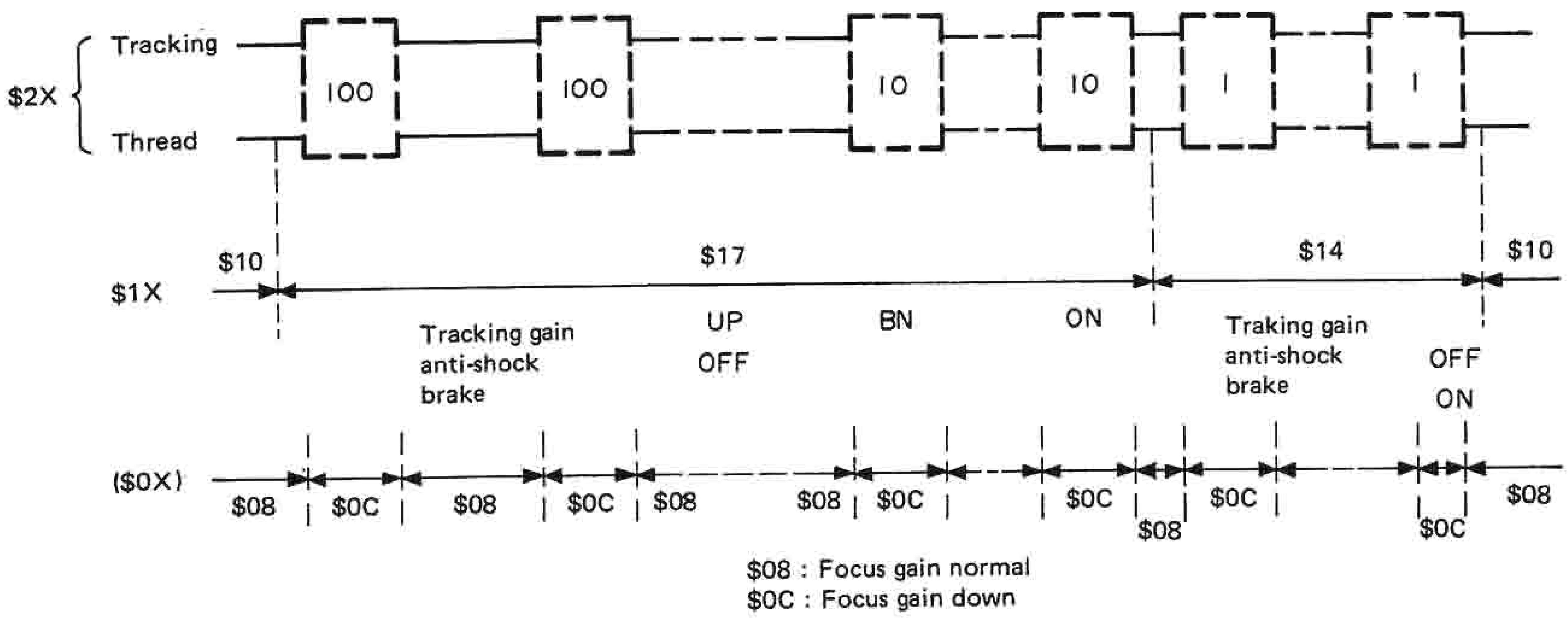


Fig. 7–19 Typical access time instruction codes

- **How to use high speed access and Count Out ⑥**

It is needless to say that access time for head search of a music and so forth is shorter. In the access using 100, 10, 1 track jump, however, about 4 seconds is the limit from the innermost periphery to the outermost periphery of the disc. It is because 100 track jump consumes more than 80% of the time, and it is possible to shorten the time if the length of time of this "major movement" can be shortened. As the distance from the current location to the destination can be learned from the TOC and the absolute time of the current location, rough feed is made for this distance.

Several methods are available as for the means to replace this distance. In general, it is the number of tracks divided by 1.6μm, sled motor revolution (number of steps, if it is a stepping motor) or potentiometer's voltage, if provided.

C.OUT ⑥ , which is a terminal exclusive for counting number of tracks is provided on this IC in order to make correspondence to counting of number of tracks. As this signal is what is obtained by latching MIRROR signal by the edge of TZC (that is, same as the signal used in the brake circuit), and therefore, even if tracking error signal, etc. include noise, such noise is ignored.

CIRCUIT DESCRIPTION

8. DP-2000 Dropout control (IC13)

8–1. Function

Disc flaws or dust may result in a pickup jump so that the correct disc replay is disturbed. To prevent this, the pickup compliance needs to be lowered over such disc areas to allow the servo gain to be reduced with the servo maintained stable.

To accomplish this, the DP-2000 CD player uses a method that radially divides a disc into N sectors which are sequentially numbered. If the signal read from a track in a given sector (i.e., a segment) largely deviates the standard, its number or address is stored in memory. Under a preestimation that the segment fails to produce a proper signal when it is read again, the address is used to lower the servo gain prior to every subsequent read from the segment.

To be precise, the DP-2000 divides a disc into 96 sectors (N = 96) for the purpose of dropout control. This is accomplished with a clock pulse. Each segment corresponds one RAM bit.

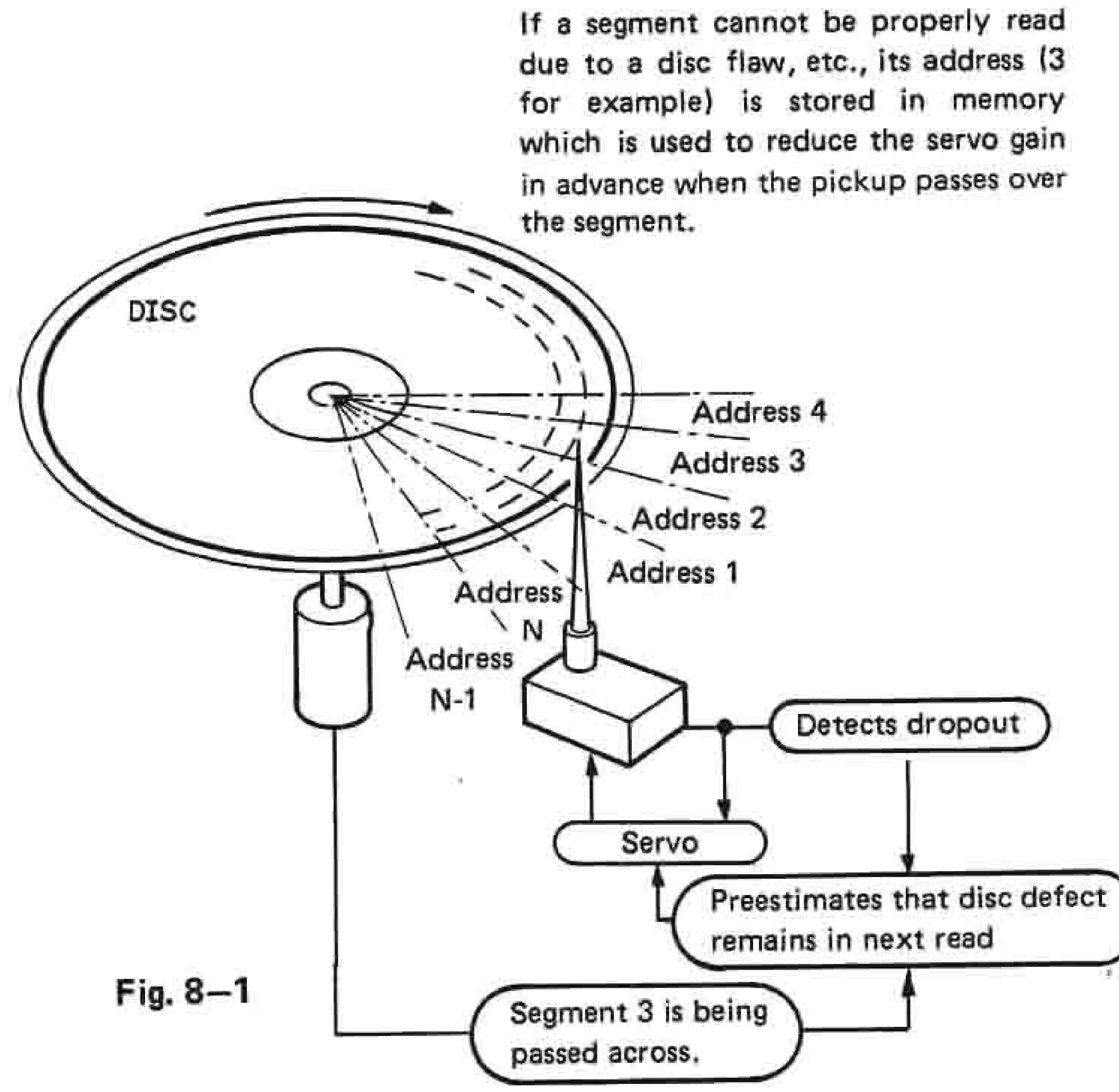


Fig. 8–1

8–2. System control flow

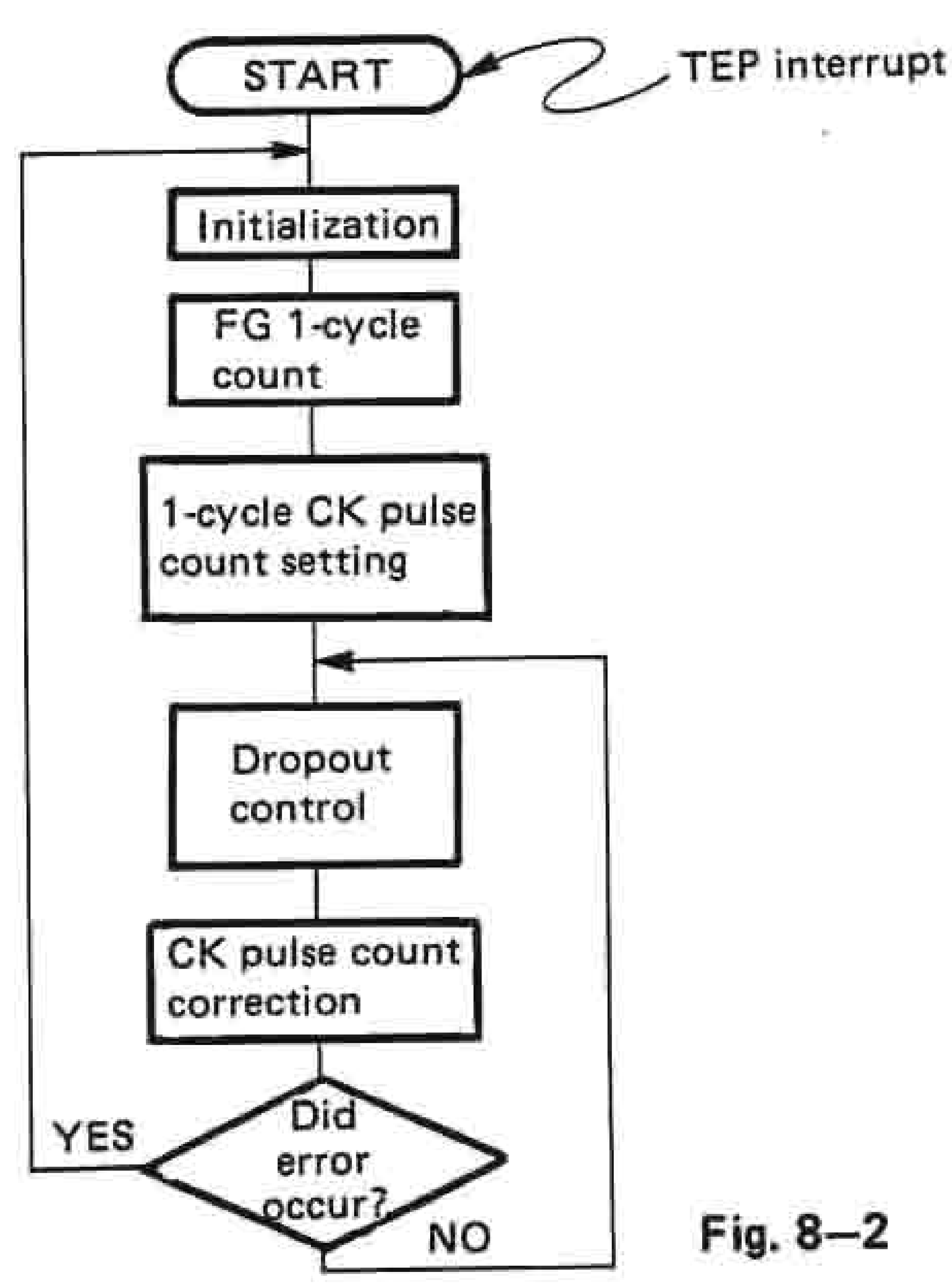


Fig. 8–2

8–3. Dropout control microprocessor (HD44700SA39) and peripheral circuits

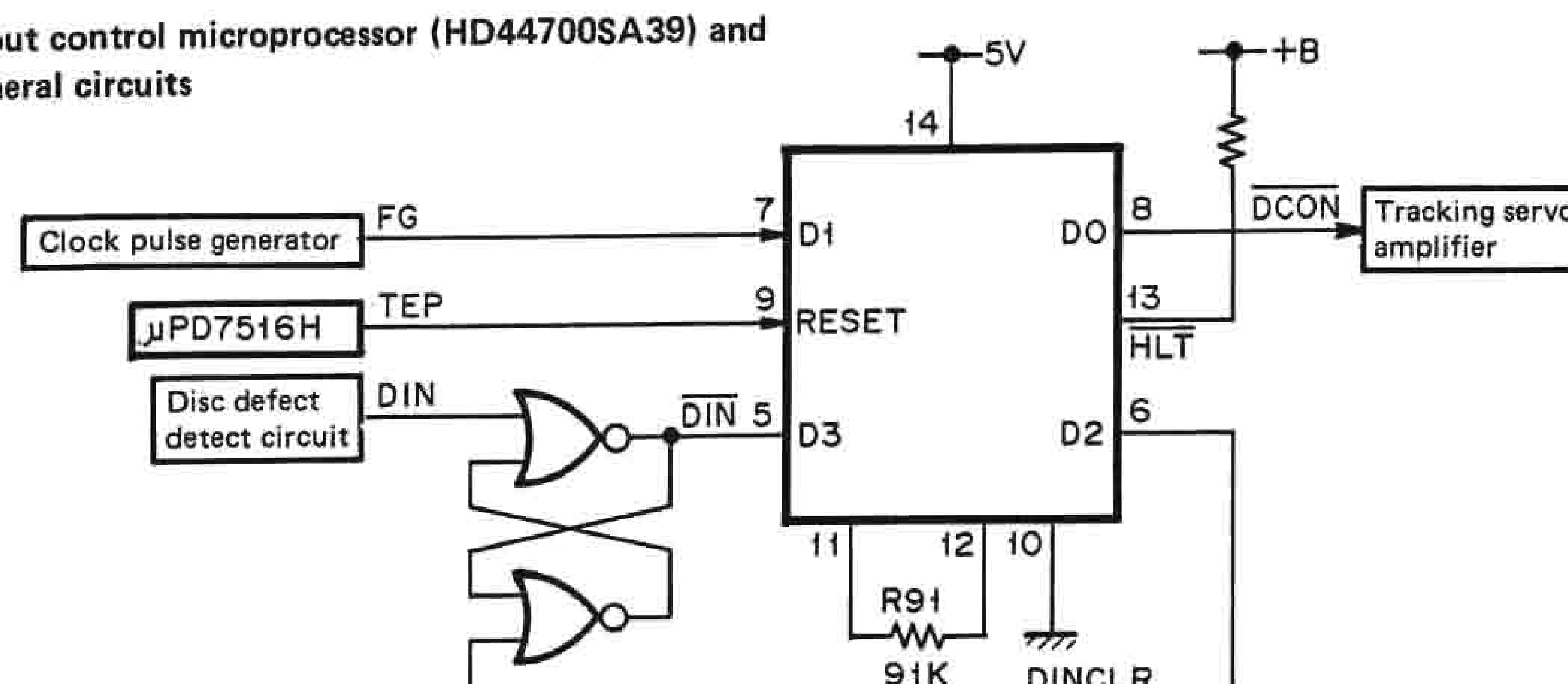


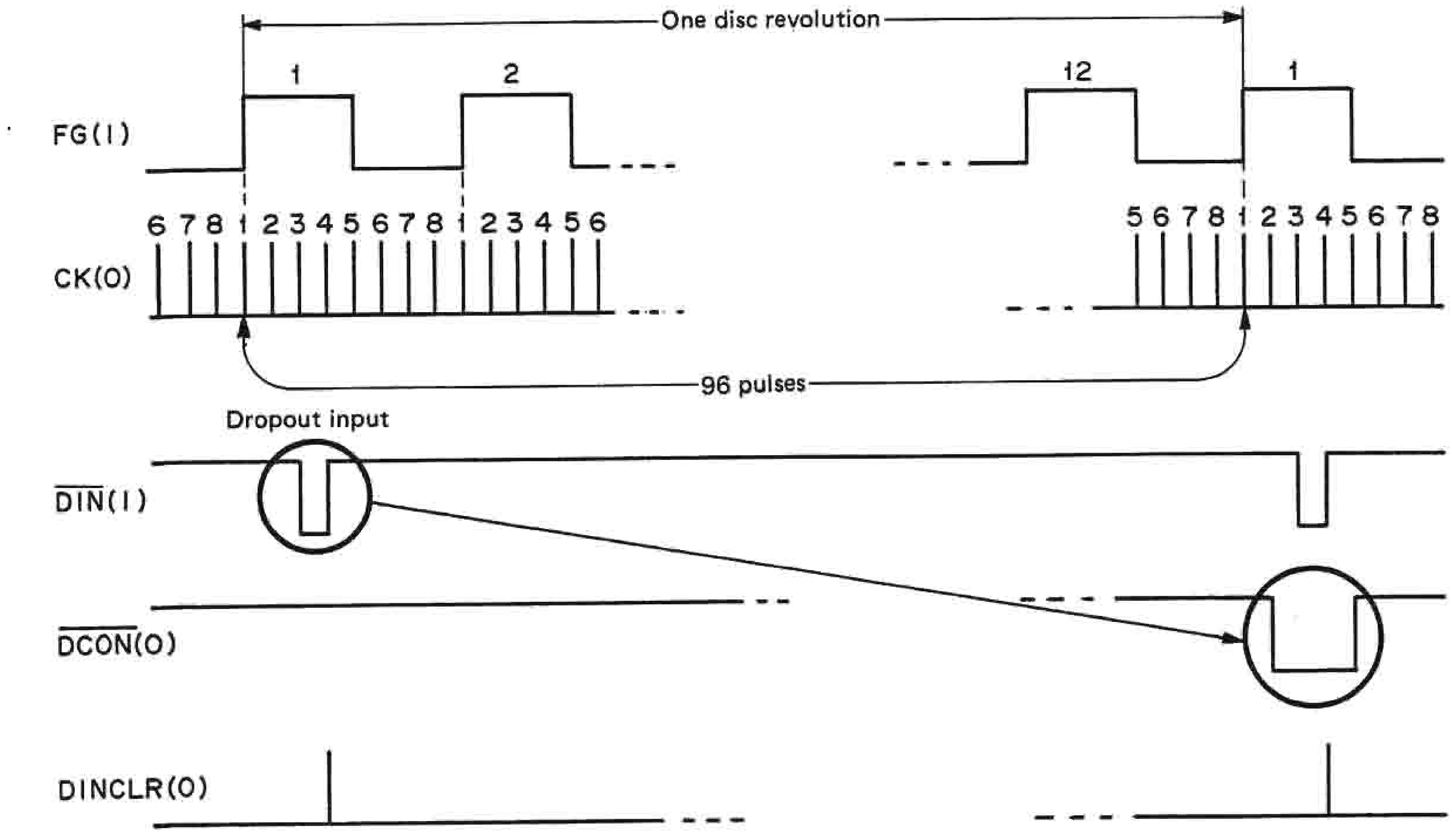
Fig. 8–3

8–4. HD44700SA39 Signals

Terminal No.	Signal name	Terminal name	I/O	Function
5	$\overline{\text{DIN}}$	D3	I	Dropout input generated by disc flaw or dust, etc. which stays latched until cleared by the DINCLR signal.
6	DINCLR	D2	O	$\overline{\text{DIN}}$ input latch reset output pulse.
7	FG	D1	I	Square-wave input signal which equally divides one disc revolution into 12 and has a cycle ranging from approx. 9ms (for inner tracks) to approx. 24ms (for outer tracks).
8	$\overline{\text{DCON}}$	D0	O	Dropout control signal that lowers the pickup servo gain. This signal is delayed by one disc revolution.
9	TEP	RESET	I	Reset signal from the μPD7516H that restores the normal operation of the dropout control circuit after a search or fast feed.

Table 8–1

8–5. HD44700SA39 Signal timing



As shown in the above figure, the DCON signal is activated approximately one clock pulse cycle prior to a preestimated dropout and deactivated approximately one clock pulse cycle after the dropout supposedly goes out.

Fig. 8–4

CIRCUIT DESCRIPTION

9. Digital signal processing (CX23035)

9–1. Functions

CX23035 is an LSI for processing digital signals of a compact disc player. It provides the following functions.

- Reproducing of bit clock by EFM-PLL circuit
- Demodulation of EFM data
- Detection, protection and interpolation of frame synchronizing signals
- Error detection, correction
- Interpolation by mean value or holding of previous value
- Demodulation of sub code signals, detection of errors in sub code Q
- CLV servo of disk motor
- Tracking counter of 8 bits
- CPU interface by serial bus

9–2. Internal block diagram

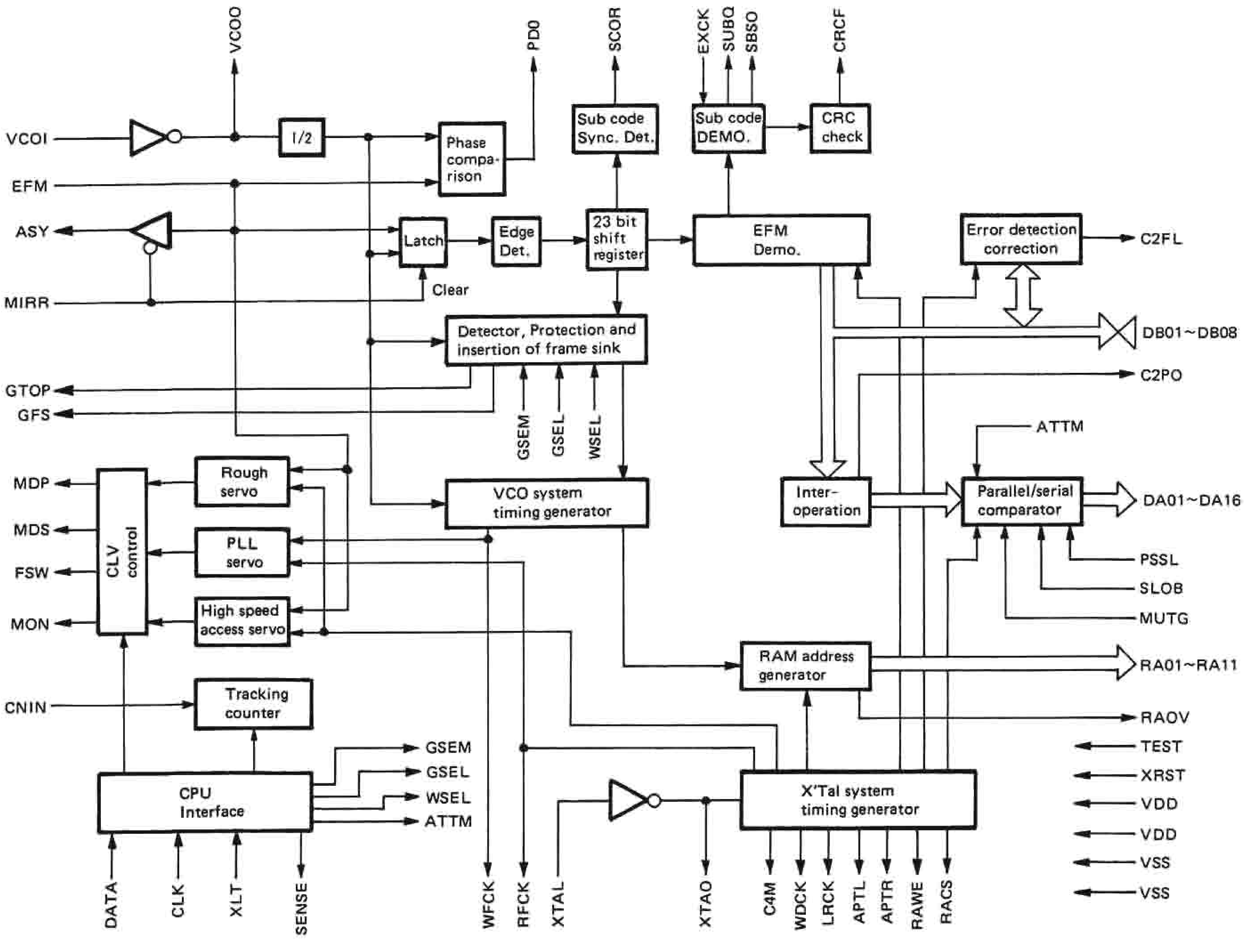


Fig. 9–1

9–3. Typical application circuits

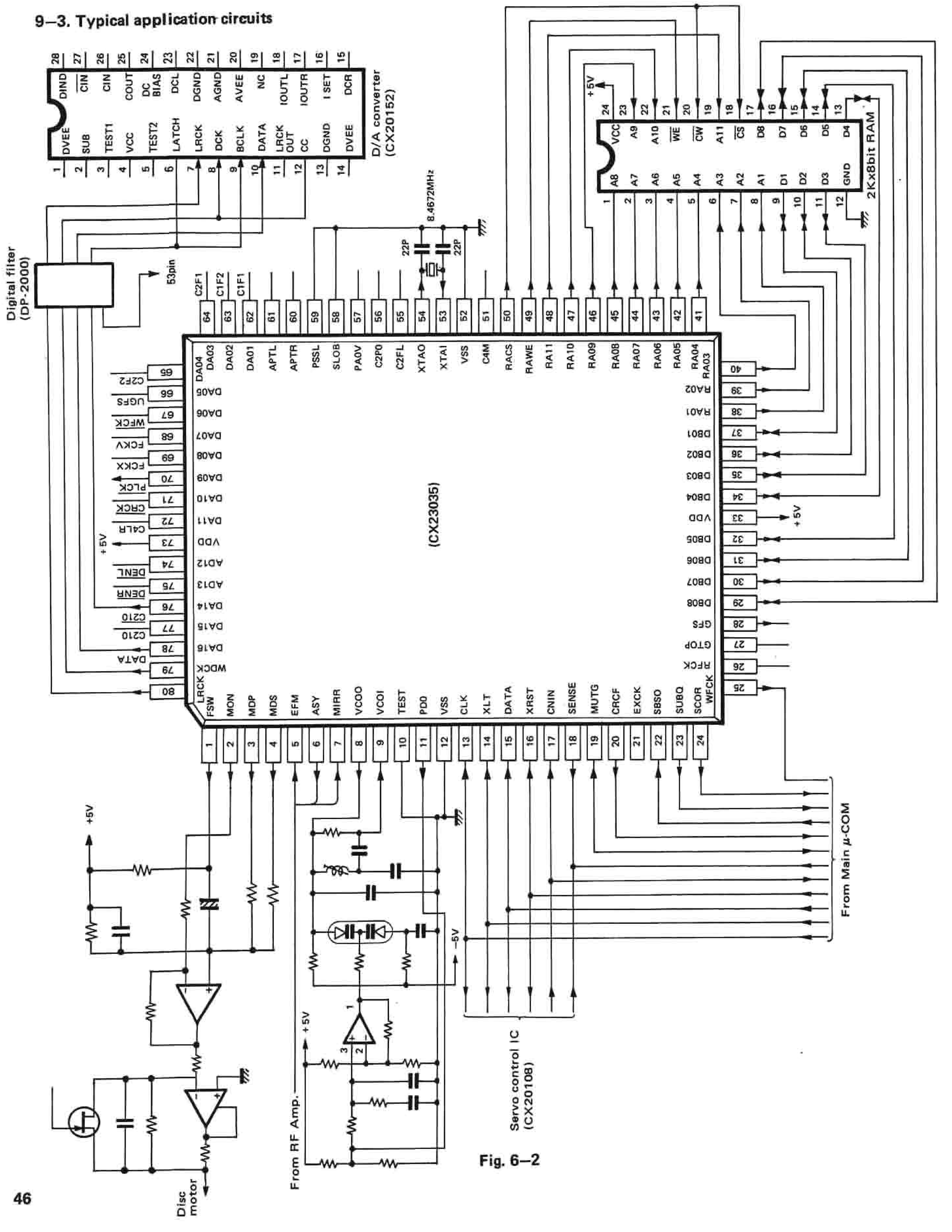


Fig. 6–2

9–4. Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1	FSW	O	Time constant switching output of output filter of spindle motor.
2	MON	O	ON/OFF control output of spindle motor.
3	MDP	O	Drive output of spindle motor. Rough speed control in CLV-S mode and phase control in CLV-P mode.
4	MDS	O	Drive output of spindle motor. Speed control in CLV-P mode.
5	EFM	I	EFM signal input from RF amplifier.
6	ASY	O	Output for controlling the slice level of EFM signal.
7	MIRR	I	MIRROR input from RF amplifier.
8	VCOO	O	VCO output. f = 8.6436MHz when locked to EFM signal.
9	VCOI	I	VCO input.
10	TEST	I	(0V)
11	PDO	O	Phase comparison output of EFM signal and VCO/2.
12	Vss	–	GND (0V)
13	CLK	I	Serial data transmission clock input from CPU. Data is latched at rising edge of a clock.
14	XLT	I	Latch input from CPU. Data (serial data from CPU) from the 8 bit shift register is latched in each register.
15	DATA	I	Serial data input from CPU.
16	XRST	I	System reset input. Reset at "L".
17	CNIN	I	Input of tracking pulse.
18	SENSE	O	Output of internal status in correspondence to the address.
19	MUTG	I	Muting input. In the case where ATTM of internal register A is "L". normal status when MUTG is "L" or soundless state when it is "H".
20	CRCF	O	Output of result of CRC check of sub code Q.
21	EXCK	I	Clock input for "Sub code serial output".
22	SBSO	O	Sub code serial output.
23	SUBQ	O	Sub code Q output.
24	SCOR	O	Sub code sync SO + SI output.
25	WFCK	O	Write Frame Clock output. f = 7.35kHz when the frame sync is locked.
28	CFS	O	Output of display of lock status of frame sync.
29	DB08	I/O	Data terminal of external RAM. DATA 8 (MSB)
30	DB07	I/O	Data terminal of external RAM. DATA 7
31	DB06	I/O	Data terminal of external RAM. DATA 6
32	DB05	I/O	Data terminal of external RAM. DATA 5
33	VDD	–	Power supply (+ 5V)
34	DB04	I/O	Data terminal of external RAM. DATA 4
35	DB03	I/O	Data terminal of external RAM. DATA 3
36	DB02	I/O	Data terminal of external RAM. DATA 2
37	DB01	I/O	Data terminal of external RAM. DATA 1 (LSB)
38	RA01	O	Address output of external RAM. ADDR01 (LSB)
39	RA02	O	Address output of external RAM. ADDR02
40	RA03	O	Address output of external RAM. ADDR03
41	RA04	O	Address output of external RAM. ADDR04
42	RA05	O	Address output of external RAM. ADDR05
43	RA06	O	Address output of external RAM. ADDR06
44	RA07	O	Address output of external RAM. ADDR07
45	RA08	O	Address output of external RAM. ADDR08
46	RA09	O	Address output of external RAM. ADDR09
47	RA10	O	Address output of external RAM. ADDR10
48	RA11	O	Address output of external RAM. ADDR11 (MSB)
49	RAWE	O	Write Enable signal output to external RAM. (active at "L").
50	RACS	O	Chip select signal output to external RAM. (active at "L").

Table 9–1

CIRCUIT DESCRIPTION

Terminal No.	Terminal name	I/O	Function
52	Vss	–	GND (0V)
53	XTAI	I	X'tal oscillation circuit input. f = 8.4672MHz
54	XTAO	O	X'tal oscillation circuit output. f = 8.4672MHz
58	SLOB	I	Code switching input of audio data output. 2's complement output at "L".
59	PSSL	I	Code switching input of audio data output. Serial output at "L".
70	$\overline{\text{PLCK}}$	O	$\overline{\text{PLCK}}$ output when PSSL = "H".
76	$\overline{\text{DA14}}$ (BCLK)	O	$\overline{\text{BCLK}}$ output when PSSL = "H".
78	DATA	O	DATA output when PSSL = "L".
79	WDCK	O	88.2kHz strobe signal output.
80	LRCK	O	44.1kHz strobe signal output.

Table 9–1

Note :

C1F1 : } Monitor output of error correction status
C1F2 : } in C1 decode.
C2F1 : } Monitor output of error correction status
C2F2 : } in C2 decode.
UGFS : Output of unprotected frame sync pattern.
$\overline{\text{WFCK}}$: Inverted output of WFCK.
FCKV : Output of WFCK/4 or WFCK/8.
FCKX : Output of RFCK/4 or RFCK/8.

$\overline{\text{PLCK}}$: VCO/2 output. f = 4.3218MHz when locked to EFM signal.
C4LR : 176.4kHz strobe signal.
$\overline{\text{DENL}}$: Enable signal of L ch serial data.
$\overline{\text{DENR}}$: Enable signal of R ch serial data.
$\overline{\text{DA14}}$(BCLK) : Inverted output of BCLK
$\overline{\text{BCLK}}$: Bit clock output. f = 2.1168MHz
DATA : Serial data output of audio signal.

6–5. Explanation of functions

- **CPU interface**

1) Data input

Each register may be set by input of 4 bit address, and 4 bit data from LSB in the timing that is shown in Fig. 9–3 to three terminals, XLT, CLK and DATA. The address and data of each terminal are as shown in Table 9–2, and their functions are as follows. The contents of each register become entirely 0 when XRST = "L".

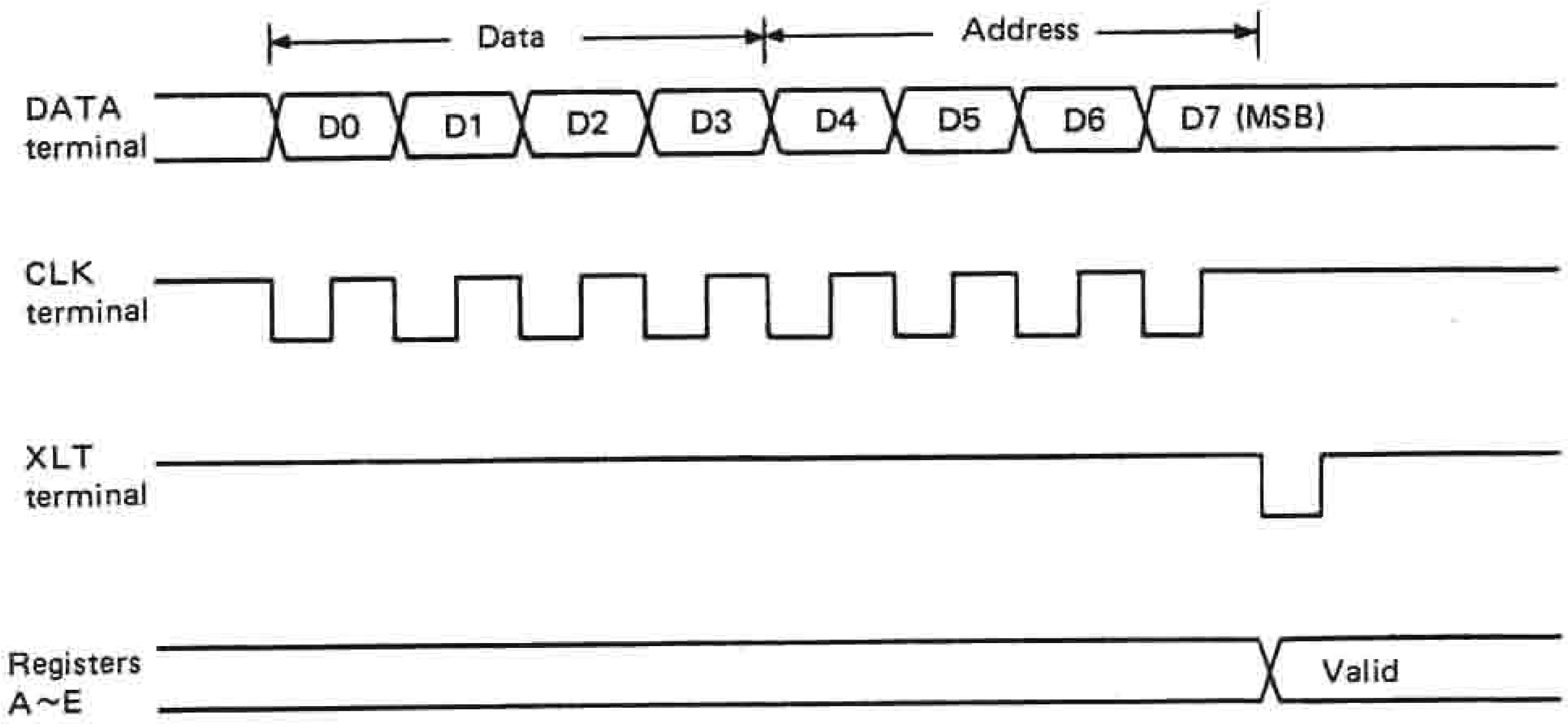


Fig. 9–3 Timing chart for data input

2) Registers

o Register A – Sync. protection, attenuator control

D3 : GSEM, D2 : GSEL, D1 : WSEL — Provided for switching frame sync. protection characteristics in correspondence to the time of playback and time of access. Details will be described in the paragraph of EFM demodulation.

D0 : ATTM Used for attenuating audio signals by 12dB, and the details will be described in the paragraph of D/A interface.

o Registers B and C – Counter set, more significant 4 bits (register C) and less significant 4 bits (register B)

these registers are used for setting the tracking count value, the data of registers B and C are preset in the counter through the 4 bit buffer register assigned by address. Accordingly, when data of either register B or C is input, the contents of both registers are preset in the counter simultaneously as 8 bit data (either buffer register is of "OLD" data.)

o Register D-CLV control

D3 : DIV Used for setting the frequency dividing ratio of RFCK, WFCK in the CLV-P mode. When D3 = 0,, phase comparison of RFCK/4 and WFCK/4 is made, and when D3 = 1, phase comparison of RFCK/8 and WFCK/8 is made, and output is made out of MDP terminal in each case.

D2 : TB Used for determining the period of bottom hold in the CLV-S and CLV-H modes. Bottom hold is made in the period of RFCK /32 when D2 = 0 or in the period of RFCK/ 16 when D2 = 1.

D1 : Tp Used for setting the period of peak hold in the CLV-S mode. Peak hold is made in the period of RFCK/4 when D1 = 0 or in the period of RFCK/2 when D1 = 1.

D0 : GAIN Used for setting the gain of MDP terminal output in the CLV-S and CLV-H modes. It is –12dB (time of 3/4 out of the period of RFCK/2 is of high impedance) when D0 = 0 or is 0dB when D0 = 1.

o Register E-CLV mode

It is as shown in Table 9–2.

The details of each mode will be described in the paragraph of CLV servo control.

When XRST = "L", all of D3~D0 are "0".

Register name	Command	Address D7~D4	Data D3	D2	D1	D0	SENSE terminal
A*1	Sync protection, attenuator control	1 0 1 0	GSEM	GSEL	WSEL	ATTM	Z
B	Counter set, Lowest or least significant 4 bits	1 0 1 1	Tc3	Tc2	Tc1	Tc0	$\overline{\text{COMPLETE}}$
C	Counter set, Most significant 4 bits	1 1 0 0	Tc7	Tc6	Tc5	Tc4	$\overline{\text{COUNT}}$
D*2	CLV control	1 1 0 1	DIV	TB	TP	GAIN	Z
E*3	CLV mode	1 1 1 0	CLV mode				Pw ≧ 64

***1) Register A**

GSEM	GSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTG terminal	dB
0	0	0
0	1	−∞
1	0	−12
1	1	−12

***2) Register D**

DIV	D3	0	RFCK/4 & WFCK/4	Phase comparison frequency in CLV-P mode
		1	RFCK/8 & WFCK/8	
TB	D2	0	RFCK/32	Bottom hold period in CLV-S, CLV-H mode
		1	RFCK/16	
TP	D1	0	RFCK/4	Peak hold frequency in CLV-S mode
		1	RFCK/2	
GAIN	D0	0	−12dB	Gain at MDP terminal in CLV-S, CLV-H mode
		1	0dB	

***3) Register E**

Mode	D3~D0	MDP terminal	MDS terminal	FSW terminal	MON terminal
STOP	0 0 0 0	L	Z	L	L
KICK	1 0 0 0	H	Z	L	H
BRAKE	1 0 1 0	L	Z	L	H
CLV-S	1 1 1 0	CLV-S	Z	L	H
CLV-H	1 1 0 0	CLV-H	Z	L	H
CLV-P	1 1 1 1	CLV-P	CLV-P	Z	H
CLV-A	0 1 1 0	CLV-S or CLV-P	Z or CLV-P	L or Z	H

Z : High impedance

Table 9–2 List of registers

CIRCUIT DESCRIPTION

3) Trakcing counter

This counter is provided for facilitating track jump. Load the number of tracks to be jumped in register B and C. Count of CNIN pulses is started at raising edge of XLT after it was loaded in either register B or C.

When n (n = 256 is meant when register B = register C = 0) is loaded in registers and the address is set at "B", a signal (COMPLETE) that is of HIGH level up to "n" pulses and is of LOW level after "n" pulses is output of SENSE terminal. When the address is set at "C", signal (COUNT) of CNIN/2n (Hz) is output.

The tracking counter timing chart is shown in Fig. 9–4.

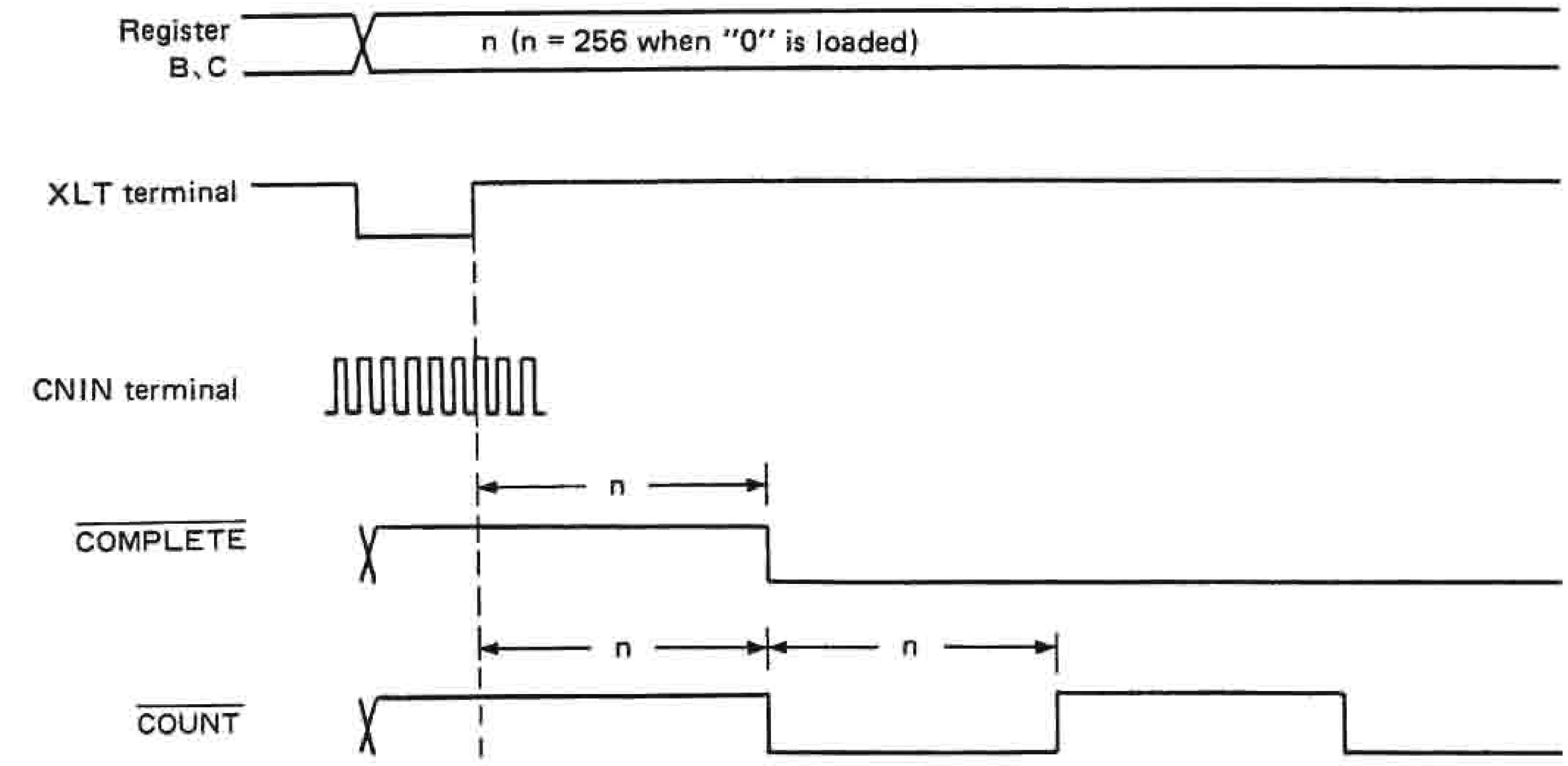


Fig. 9–4 Tracking counter timing chart

4) SENSE

The following signals are output from SENSE terminal depending on the address of D7~D4.

1. $\overline{\text{COMPLETE}}$: Address is "B"; Shown in Fig. 9–4.
2. $\overline{\text{COUNT}}$: Address is "C"; Shown in Fig. 9–4.
3. $\overline{\text{PW≧64}}$: Address is "E"; this signal is of LOW level when the pulse width after bottom hold is more than 64, and is of HIGH level otherwise. It is used for detection of a drop in the speed of the spindle motor after braking and so on.

Note : Address setting is determined only by the data that corresponds to D4~D7 which can be input from DATA terminal shown in Fig. 9–3.

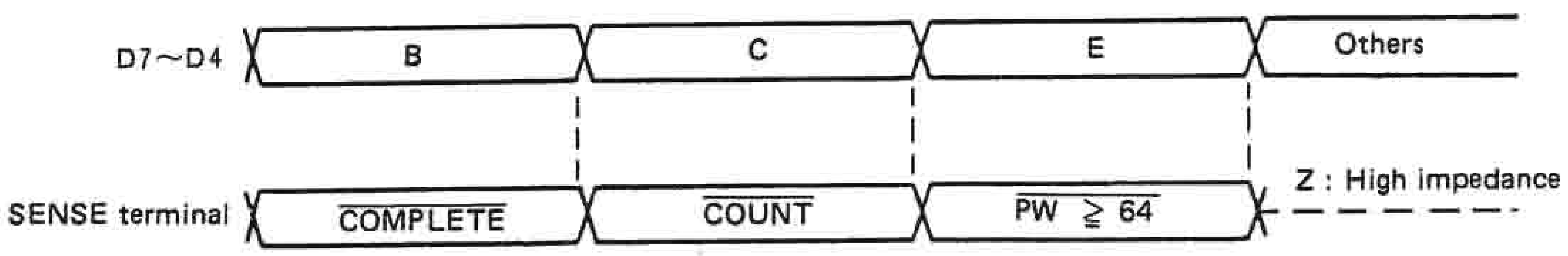


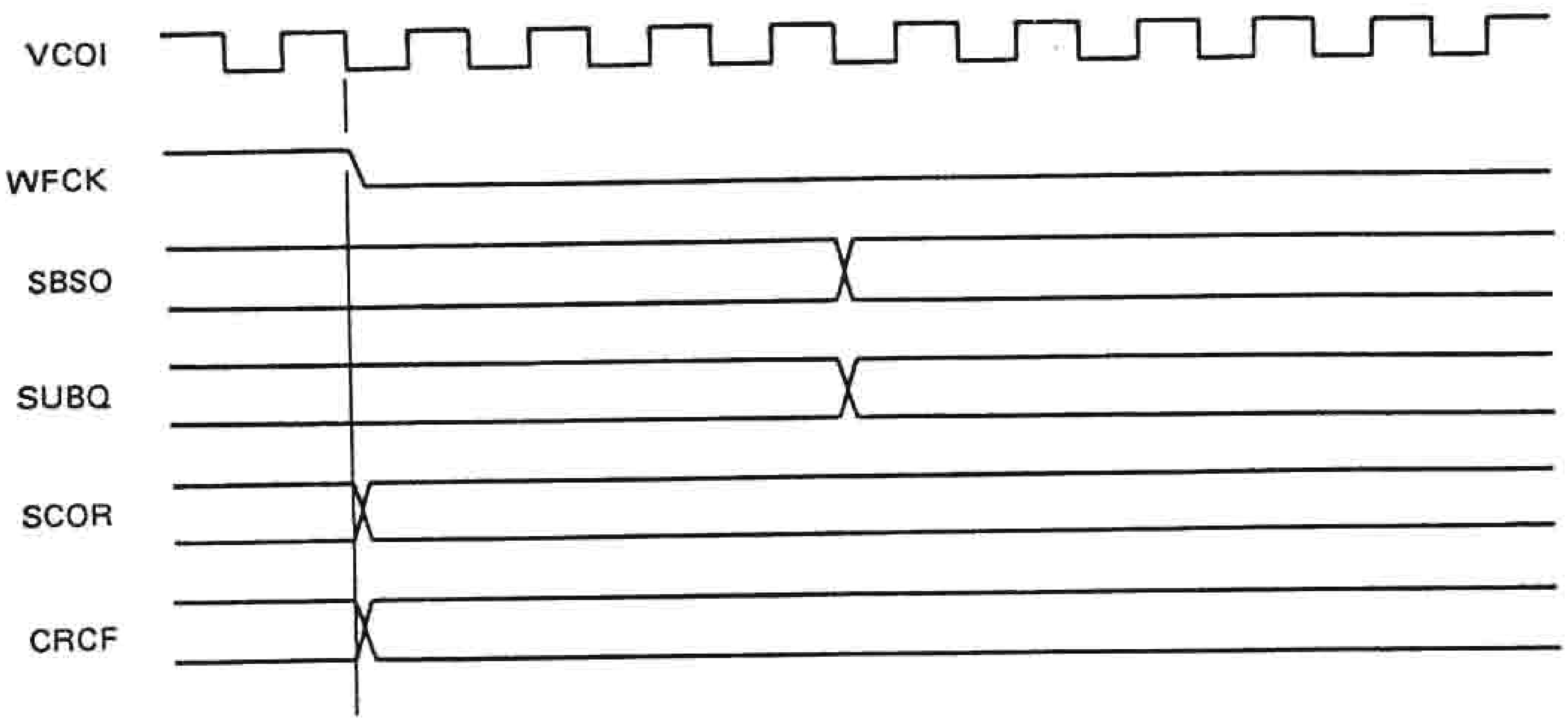
Fig. 9–5 Timing chart of SENSE terminal

5) Sub code output

Sub codes P~W loaded in the 8 bit shift register are output from . SBSO terminal in accordance with the clock input through EXCK terminal. When SCOR terminal is "H", S0 · S1 signal is output.

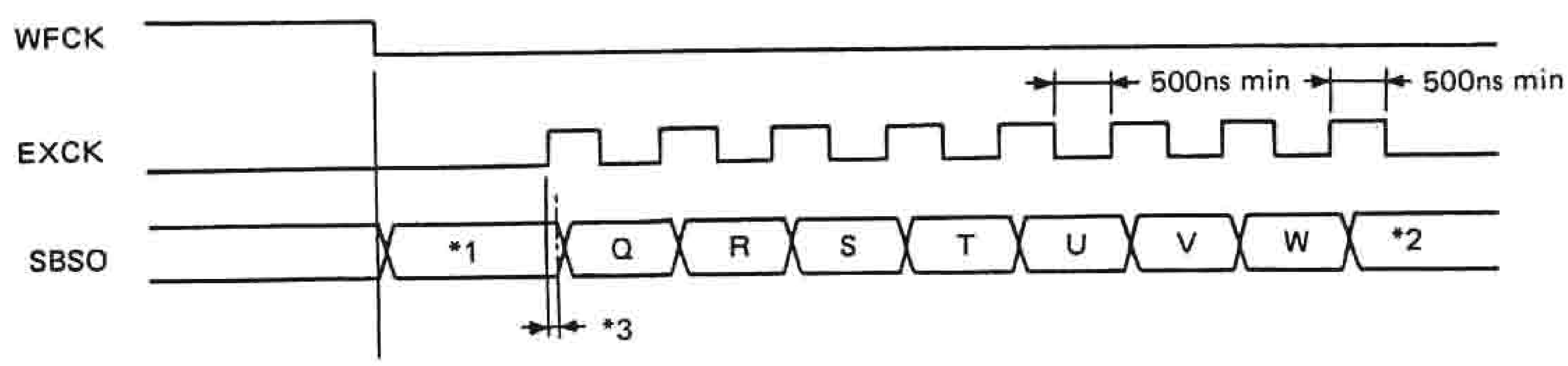
Sub code Q is output from SUBQ terminal in synchronization with WFCK. The result of error detection of sub code Q is output out of CRCF terminal in synchronization with SCOR. These timing charts are shown in Fig. 9–6.

(a) Timing of SBSO, SUBQ, SCOR, CRCF

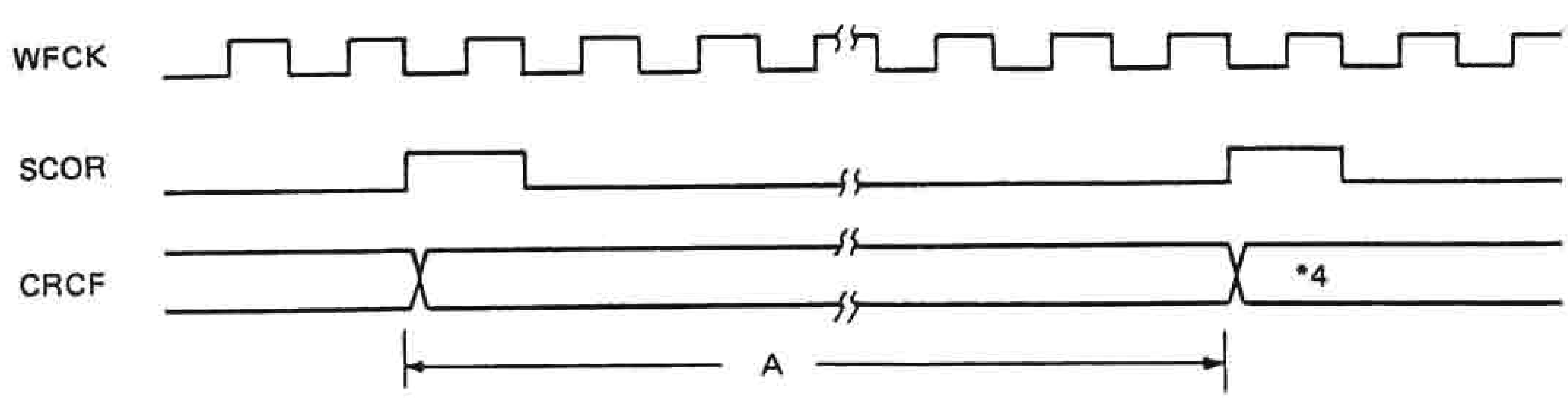


(b) Timing of SBSO, EXCK

*1 : Sub code P is output when SCOR is 0.
S0 · S1 is output when SCOR is 1.
*2 : SBSO is 0 when 8 or more pulses are input to EXCK.
*3 : 4T~6T if the period of VCO is expressed as T.
One period of T = 8.6436MHz.



(c) Timing of SCOR, CRCF



*4 : CRC check is made regarding sub code Q in period A.
CRCF = 1 when OK, or CRCF = 0 when NG.

Fig. 9–6 Timing charts of sub code outputs

CIRCUIT DESCRIPTION

- **EFM demodulation**

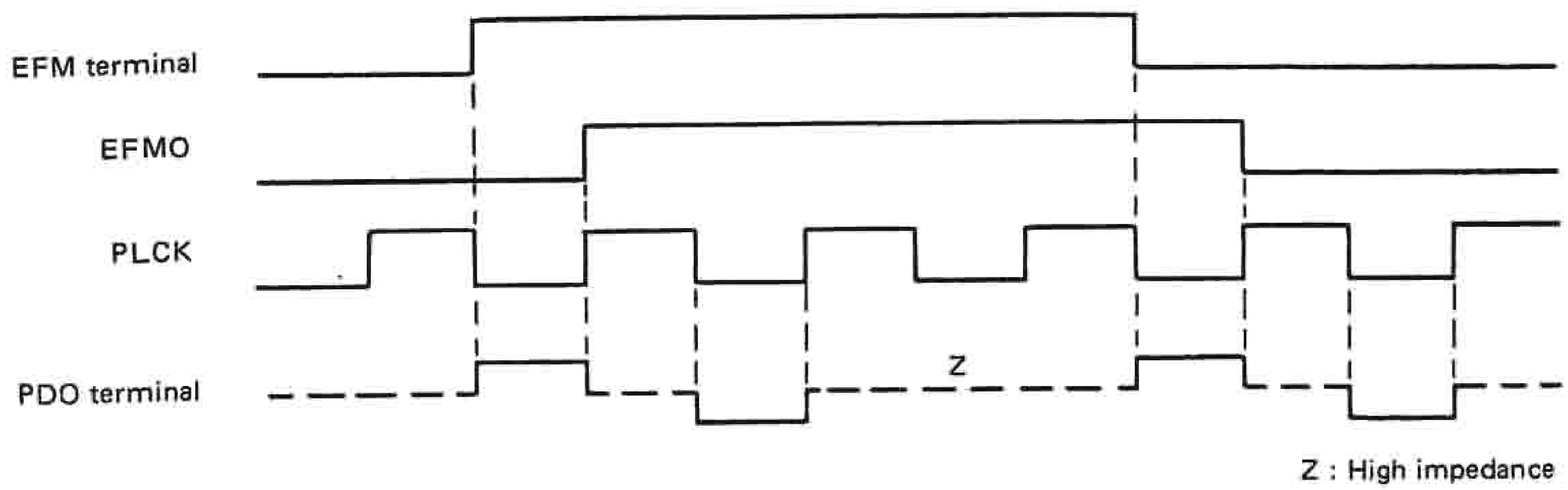
1) Playback of bit clock by EFM-PLL circuit

The EFM signal read out of the optical block contains a clock component of 2.16MHz. Therefore, it is possible to take out a bit clock (PLCK) of 4.32MHz synchronized with this clock by the EFM-PLL circuit.

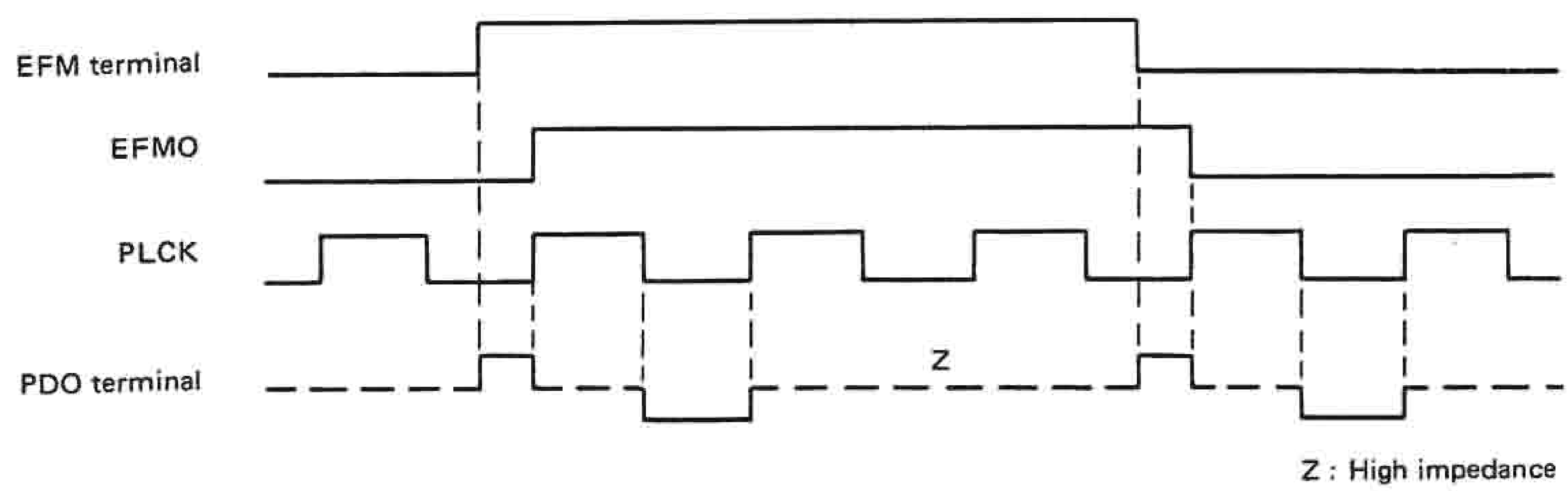
At each edge of EFM signal, phase comparison is made with PLCK, which is 1/2 of VCO, is made and output is made by TRI STATE out of PDO terminal. The mean value of PDO terminal is about 1/2 VDD if synchronized, but the mean value drops when VCO becomes higher. On the other hand, the mean value increases when VCO becomes less.

The timing charts of EFM terminal, EFMO, PLCK and PDO are shown in Fig. 9–7.

(a) When EFM signal and VCO are synchronized



(b) When VCO is higher than EFM signal



(c) When VCO is less than EFM signal

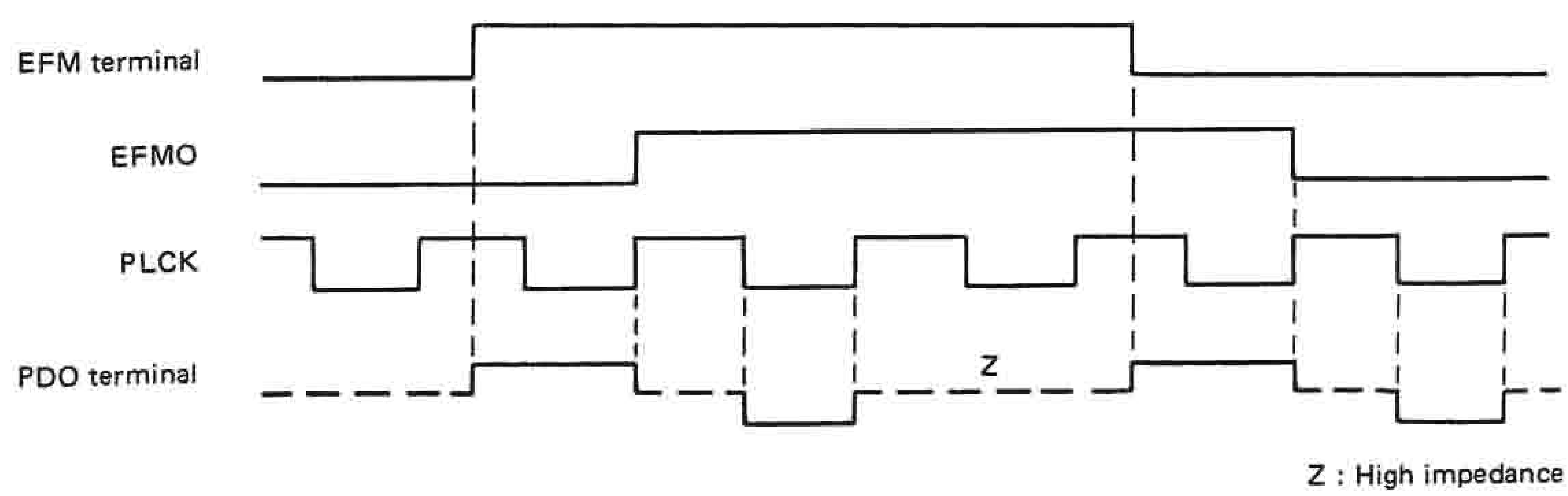


Fig. 9–7 Timing charts of EFM-PLL circuit

2) Detection, protection and interpolation of frame synchronizing signals

There are cases during recording where the same pattern is detected in the data due to the influence of drop-out and jitter, even if a pattern that is same as the synchronizing signal will not appear.

On the other hand, there also are cases where original frame synchronizing signal is not detected. Therefore, protection and interpolation are required besides detection.

The edge portion only of EFM signal (EFMO) latched with PLCK is converted to "1" and the rest to "0", and then input is to a 23 bit shift register and a frame synchronizing signal is detected.

In order to protect a frame synchronizing signal, a window is provided and the same patterns outside of this window are removed. This width can be selected with WSEL. If no frame synchronizing signal is located in this window, interpolation is made with a signal produced by 588-mal counter (4.3218MHz/588 = 7.35kHz)

A 4 bit counter for counting the number of these frames to be interpolated is provided, and when its count reaches the level selected with GSEL, GSEM, the window is ignored and the 4 bit counter is reset with the next frame synchronizing signal. the GTOP terminal is of "H" while this operation is performed. Further, GFS terminal is of "H" when the frame synchronizing signal generated by the 588-mal counter for making interpolation is synchronized with the frame synchronizing signal from the disc.

The frame synchronizing signal before passage through the window or the window is output from UGFS (DA05 terminal at the time when PSSL = L.)

WSEL	Window width
0	±3 clock
1	±7 clock

GSEM	GSEL	Number of frames to be interpolated	UGFS (PSSL = "L")
0	0	2 frames	Window
0	1	4 frames	Window
1	0	8 frames	Frame synchronizing signal before passage through window.
1	1	13 frames	Window

The timing for write request signal (WREQ), Write Frame Clock (WFCK), etc. is generated based on the protected and interpolated frame synchronizing signal.

3) EFM demodulation

14 bit data is taken out of the 23 bit shift register and is demodulated to 8 bit data through 14 → 8 conversion circuit composed of array logics. Then a write request (WREQ) signal is output to the RAM interface block, and the data is then output to the data bus (DB08~DB01) terminals) of the RAM in accordance with the OENB signal transmitted from said block.

- **Sub code demodulation**

1) Sub code demodulation

synchronizing signals S0, S1 of 14 bit sub codes are detected out of the 23 bit shift register, and sampling is made in the timing that is synchronized with WFCK.

After delay of S0 by one frame, S0 + S1 is output from SCOR terminal and S0 · S1 is output from SBSO terminal (only when SCOR = H).

Data (P~W) of sub codes only is input to the register in the timing synchronized with WFCK after EFM demodulation; and sub code Q is output from SUBQ terminal, and at the same time, it is loaded in the 8 bit shift register and is output from SBSO terminal in correspondence to a clock from EXCK terminal.

The detials of this timing will be shown in the paragraph of CPU interface.

2) Error detection of sub code Q

The result of CRC of sub code Q is output from CRCF terminal in synchronization with SCOR terminal. "L" is produced when an error is detected. The details of this timing will be described in the paragraph of CPU interface.

CIRCUIT DESCRIPTION

- **RAM interface (generation of external RAM address)**

1) Request from EFM demodulation block (Write RAM request)

When one symbol of demodulation is complete in the EFM demodulation block, the EFM demodulation block requests to write data to the external RAM to the RAM interface block. This request is WREQ signal. This block gives priority orders to requests from other blocks and processes these requests.

When EFM write request is received, an address is generated to the RAM and Write Enable state is produced. Furthermore, a data output instruction is issued against the EFM demodulation block. This instruction is OENB signal.

Clocks of PLL system are used for EFM block and for requests (WREQ) from EFM block, but clocks of X'Tal system are used for processing thereafter.

2) Request from D/A converter output circuit (Read to D/A request)

This is a de-interleaved data request issued out of the timing generator in this block. This request is of the highest priority among all requests, and addresses of three types are generated against this request.

This request is generated once every 24 periods based on the period of system clock C212 (8.4672MHz/4). The data output from the RAM is C2 pointer first, least or lowest significant 8 bits of 16bits and finally most significant 8 bits.

3) Request from error correction block (C1/C2 correction, pointer R/W)

The error correction block requests the data located on the system (C1/C2) to be corrected. Furthermore, there is a request to rewrite incorrect data to correct data. In addition, there is a request for pointer R/W which indicates reliability of data.

These requests are made by the 8 bit data directed to the RAM interface block from the error correction block. The requests from the error correction unit are of the lowest priority among requests of three types. After acceptance of a request, data from RAM is directed to the 3rd clock of C212.

The data of acceptance of a request is output to the error correction block as a PREN signal. This block generates the address of the requested data, and controls R/W of the RAM at the same time.

4) Address generation

The data after EFM demodulation is data subjected to interleave processing. This interleave processing is subjected to data lag by the unit of a frame. Data of 108 frames are required for de-interleave. In other words, for obtaining one frame of audio data played in a certain length of time, data of 108 frames after EFM demodulation are required. Further, the system data of C1/C2 is of the system in the process of application of interleave, and therefore, is included in 108 frames.

Data in practice are generated continuously. That is, de-interleave should be updated by the unit of a frame. Therefore, Read/Write base counters are required. This base counter performs counting by the unit of a frame.

The writer base counter is used only at the time of EFM data writer. The address directed to the external RAM is determined by the relative lag value to EFM demodulation data and their number of frames.

5) Priority of address generation request

The system control block determines priority of address generation requests made to the RAM interface block.

The priority order is as follows beginning with higher priority.

1. Read to D/A request
2. Write to RAM request
3. C1/C2 request

The number of times of requests is as follows.

1. Requests of 12 times in the frame section
   The number of times of address generation to it is 36 times.
2. Requests of 32 times in the frame section
   The number of times of address generation to it is 32 times.
3. Maximum number of times of request (C1 Double error correction, C2 pointer copy)
   Read R/W 64 times, Pointe R/W 65 times in one frame section
   The number of times ot address generation to it is 129 times.

C212 (clocks) are included 288 PCS in a frame, and the number of times of operation of the RAM in it is 197 times at maximum. In the system control block, against request 1, the timing of its occurrence is reserved in advance. Requests 2, 3 are not accepted in this timing. When requests 2, 3 are generated simultaneously, priority is given to request 2, and if a request is generated during execution of either request, priority is given to the job in execution.

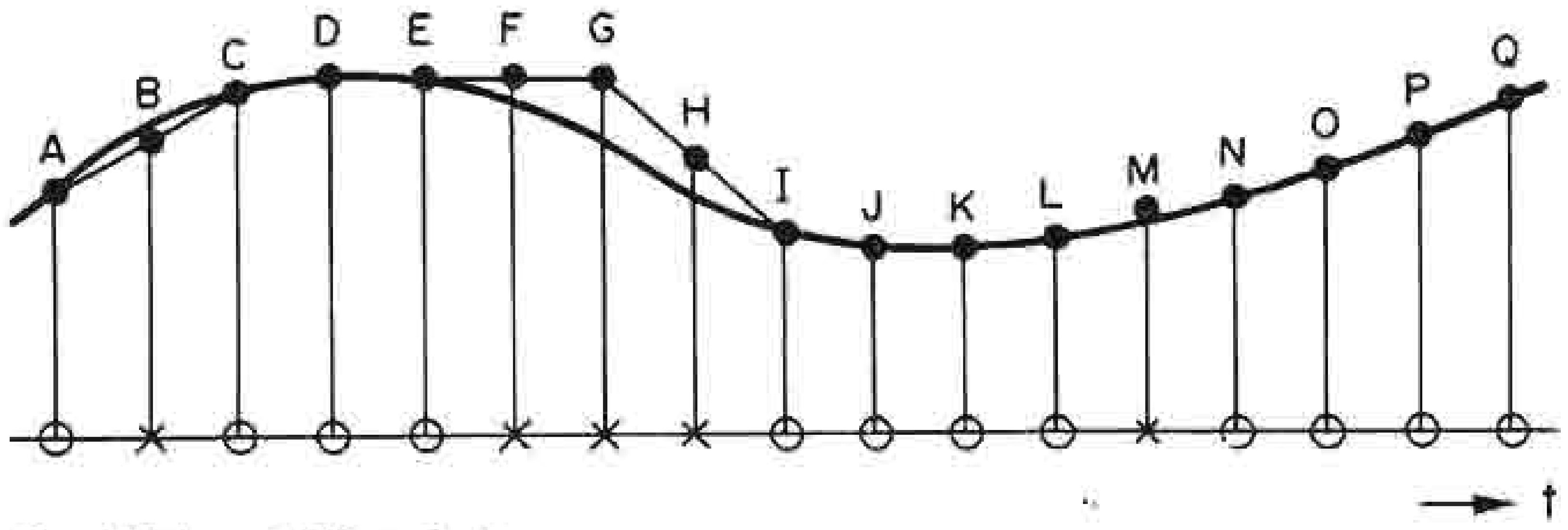
6) Jitter margin

The EFM demodulation data is synchronized with data's playback system (PLL) as described earlier. Accordingly, it includes disturbance (wow, flutter, etc.) of disc rotation servo, etc. It is loaded to the external RAM. As the data taken out of the RAM is synchronized with the clock of X'Tal system, this RAM is subjected to time axis correction.

However, the limit of time axis correction is determined by the capacity of the RAM. In this system, other data is destroyed when read/write frames are spaced apart by ±5 frames. In such a status how the playback sound is cannot be guaranteed. The base counter monitor is provided in order to avoid it.

In other words, when the difference between read base counter and write base counter exceeds ±4 frames, the write base counter is set in the value of the read base counter. As a result, there is no case where data without error correction is output to the D/A.

The RAOV signal is of "H" for one frame (WFCK) section when the difference between base counters exceeded ±4 frames.



O : Without C2 pointer
X : With C2 pointer

Fig. 9–8

- **Interpolation and D/A converter interface**

1) Interpolation circuit block

3 byte data can be obtained with a Read to D/A request. They are C2 pointer, lowest or least significant 8 bits and most significant 8bit. The total 16 bits constitude the data generated per sampling (2's complement.)

The C2 pointer expresses the reliability of this 16 bit data. Therefore, data with C2 pointer is subject to interpolation in this block.

Mean value interpolation

$$B=\frac{1}{2}(A+C)$$

$$H=\frac{1}{2}(E+I)$$: When pointers are continuous

$$M=\frac{1}{2}(L+N)$$

Previous value hold

$$F=G=E$$

16 bit data is alternately output to L-ch and R-ch, R-ch data is output in the section in which LRCK is "L" and L-ch data is output in the section in which LRCK is "H". C2PO signal outputs C2 pointer to the 16 bit data directed to DA01–DA16 (PSSL = H), DA16 (PSSL = L). In other words, it means that the 16 bit data that is output when C2PO is "H" is interpolated data.

CIRCUIT DESCRIPTION

2) Explanation of muting and attenuator

In the muting block it is possible to mute (– ∞ dB) or attenuate (–12dB) the audio signal in accordance with the MUTG terminal and ATTM signal of the CPU interface block.

Note : When MUTG is set at "H", the value of the base counter is forcibly kept loaded to the write base counter besides muting.

ATTM	MUTG	Attenuation value	Remarks
0	0	0dB	
1	0	–12dB	
0	1	– ∞ dB	See Note
1	1	–12dB	See Note

3) D/A converter interface

Various D/A converters and interfaces can be produced using SLOB (terminal) and PSSL (terminal).

○SLOB (offset binary, 2's complement switching)

SLOB = "H" Offset binary
SLOB = "L" 2's complement

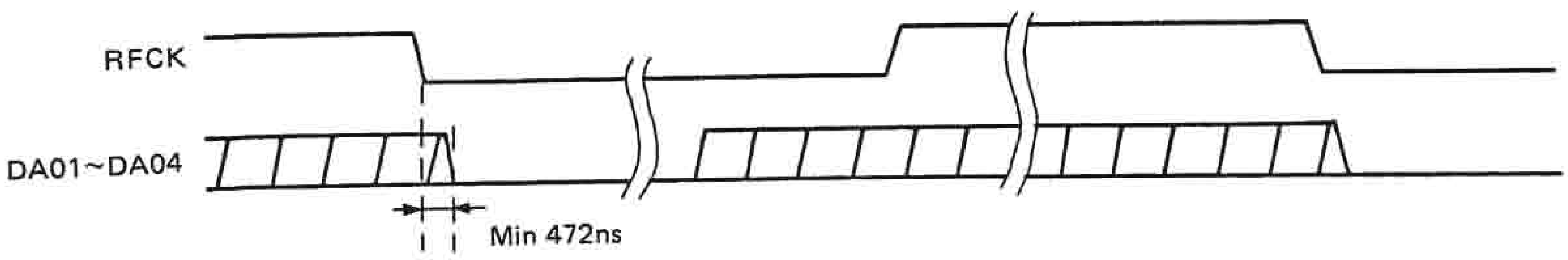
MSB inversion of 2's complement is offset binary.

○PSSL (parallel/serial selection)

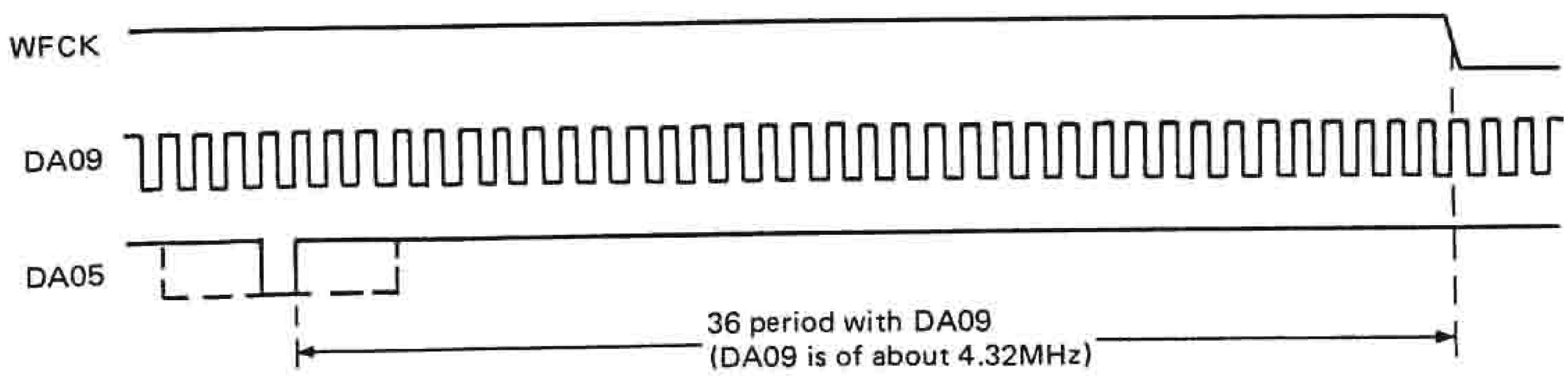
PSSL = "H" 16 bit parallel data output (DA01~DA16)

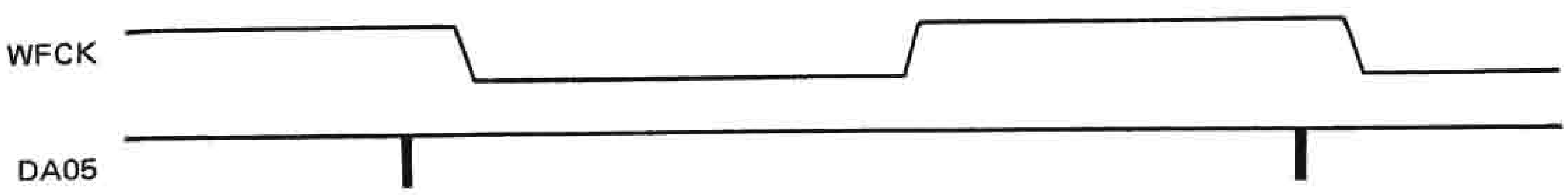
PSSL = "L" Serial data output

DATA (DA16)	Serial data output (MSB first)
C210 (DA15)	Internal system clock (C212) 2.1168MHz
$\overline{\text{C210}}$ (DA14)	C210 inverted signal
$\overline{\text{DENR}}$ (DA13)	R ch's serial data enable signal R ch data 16 bit output section "L"
$\overline{\text{DENL}}$ (DA12)	L ch's serial data enable signal L ch data 16 bit output section "L".
C4LR (DA11)	176.4kHz strobe signal Quadruple signal of LRCK (44.1kHz) Double signal of WDCK (88.2kHz)
$\overline{\text{PLCK}}$ (DA09)	1/2 period signal at VCO terminal When locked with EFM signal f = 4.3218MHz
FCKX (DA08)	RFCK/4 or RFCK/8 is output. Refer to CLV servo control explanation.
FCKV (DA07)	WFCK/4 or WFCK/8(Hz) is output. Refer to CLV servo control explanation.
$\overline{\text{WFCK}}$ (DA06)	WFCK's inverted signal
$\overline{\text{LRCK}}$ (DA10)	LRCK's inverted signal.
UGFS (DA05)	Unprotected frame sinc Refer to EFM demodulation explanation.
C2F2 (DA04) C2F1 (DA03) C1F2 (DA02) C1F1 (DA01)	Monitor in correction status Refer to monitor error correction explanation.



* DA01~DA04 (C1F1, C1F2, C2F1, C2F2) are cleared when a period of minimum 472 ns has elapsed since RFCK was deactivated.
* ANDing signal of C2F1 and C2F2 is output out of C2FL terminal.





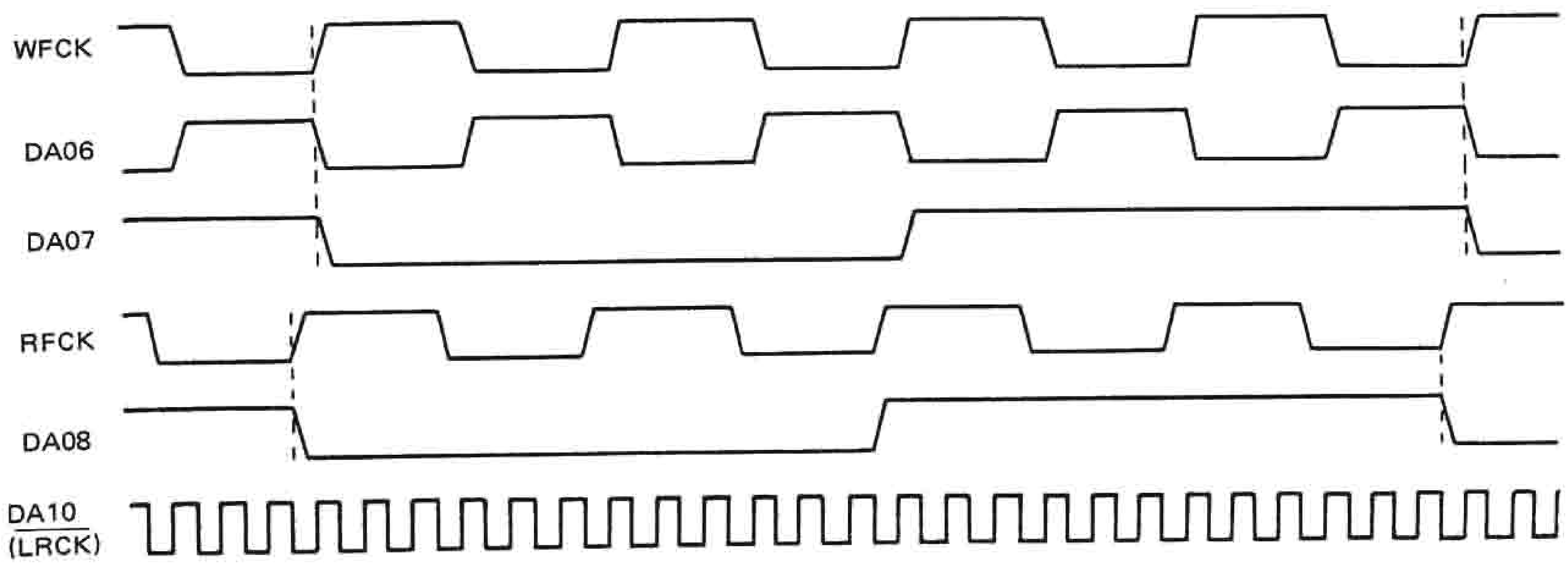


Fig. 9–9 Timing chart of DA01~DA16 output when PSSL = "L"

CIRCUIT DESCRIPTION

* RAOV becomes "H" for one frame (synchronized with WFCK) when a jitter that exceeds ±4 frames is generated between RFCK and WFCK.

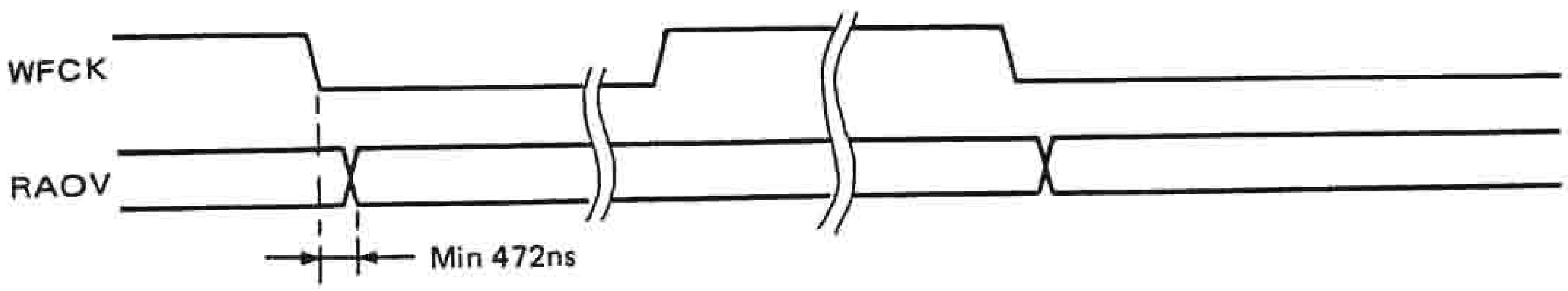
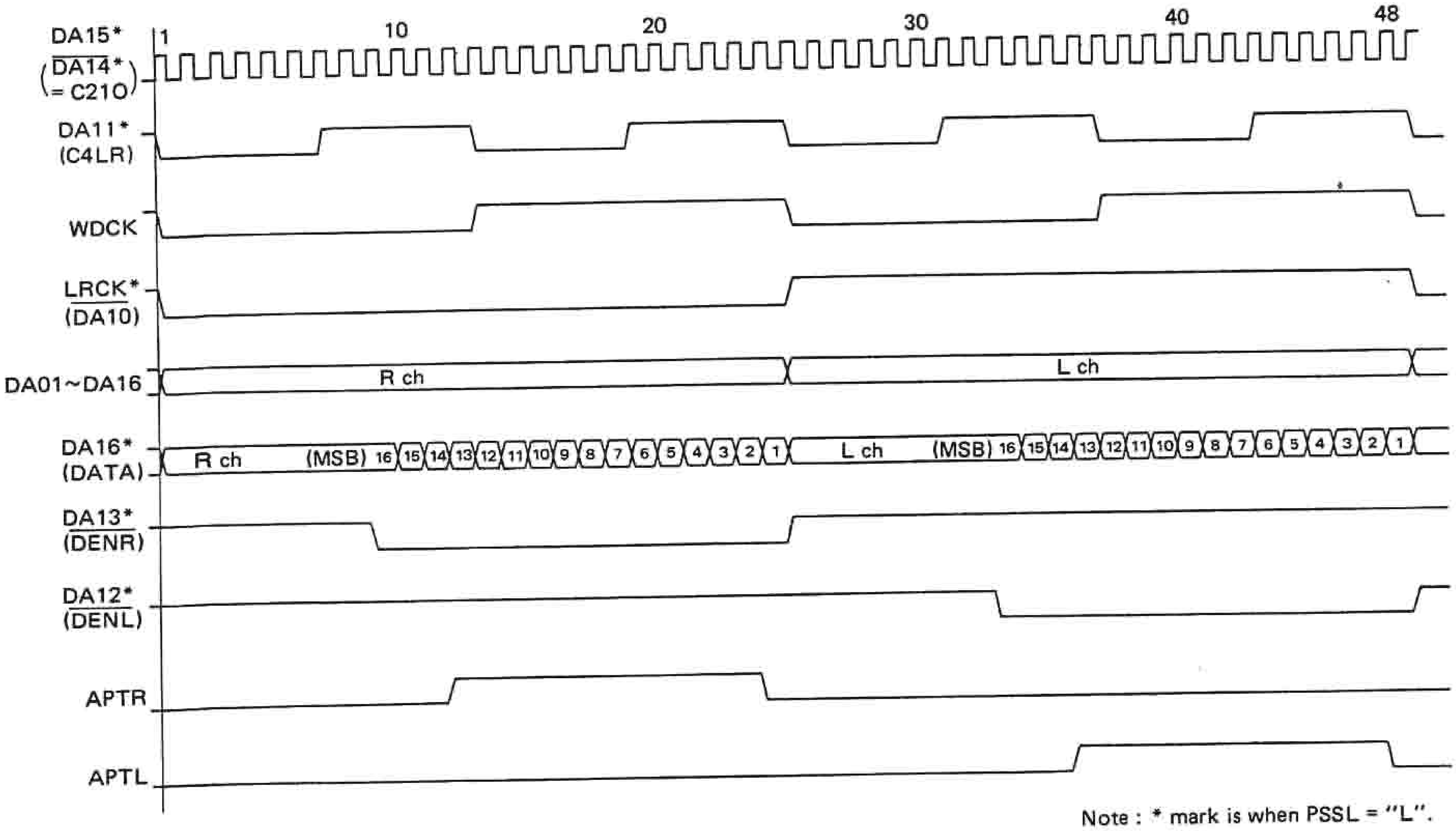
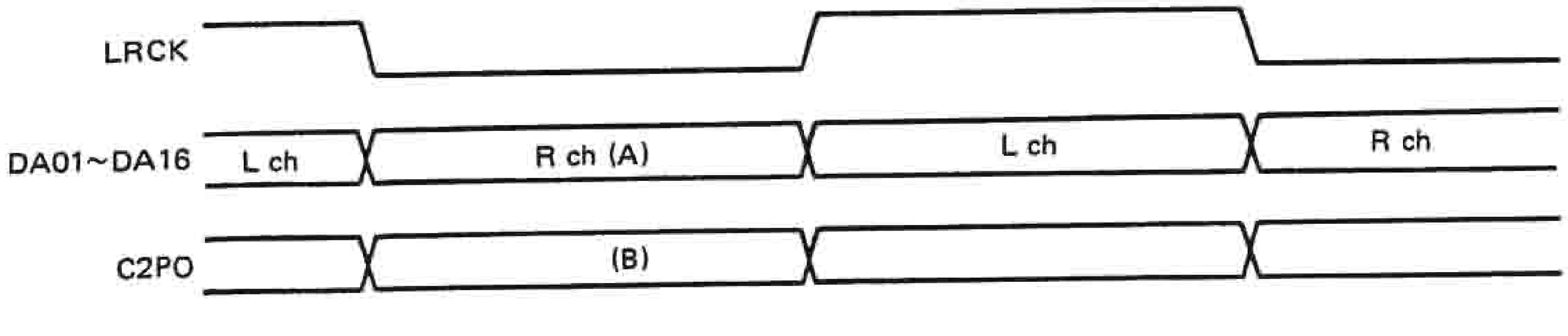


Fig. 9–10 Timing chart of RA0V output



Note : * mark is when PSSL = "L".

Fig. 9–11 Timing chart of audio data output



* C2PO is "L" when DA01~DA16 is reliable data, and is "H" when they are unreliable data. C2PO to data of (A) is generated in the timing of (B).

Fig. 9–12 Timing chart of C2PO output (when PSSL = "H")

CIRCUIT DESCRIPTION

- **Error correction**

1) The error correction block makes correction up to double errors with each of C1 correction and C2 correction.
2) This system adopts a unique pointer erasure method in order to minimize erroneous correction. Accordingly, the external 16k RAM stores these pointer data in addition to audio data.
3) The pointer generated in C1 correction is called C1 pointer and the pointer generated in C2 correction is called C2 pointer.
4) When the data of C1 system is judged as reliable, a C1 pointer is set in this system.
5) During C2 correction, whether correction is to be made or not to be made and whether the data is reliable or unreliable are judged from the error location, locations and number of C1 pointers obtained through computation. A C2 pointer is set against an unreliable word (16 bits).
6) The word in which a C2 pointer was set is subjected to previous value hold or mean value interpolation when it is output from this LSI.
7) Terminal C2FL becomes "H" when one or more C1 pointers are set in the data included in the C2 system at the time of C2 correction. C2FL is reset to "L" when a period of minimum 472ns after deactivation of terminal RFCK. C2FL is the AND of C2F1 and C2F2.

Note : 472ns : One period of 2.1168MHz

8) The flow of data with the external RAM is as follows.

A data request is made from the correction block to the RAM interface block.

↓

The RAM interface block accepts the request with the operating situation of the entire system observed. The address of the requested data is generated to the external RAM.

↓

Read/Write of the correction block and RAM data are enabled.

9) When PSSL is set at "L", a signal that is capable of monitoring error correction is output. C1F1, C1F2, C2F2 output to DA01~DA04 are these monitor signals. This signal is reset to "L" when a period of minimum 472 ns has elapsed since deactivation of RFCK.
The levels and meanings of these signals at the time of deactivaiton of RFCK are as follows.

C1F1	C1F2	C1 correction status
0	0	No Error
1	0	Single error correction
0	1	Double error correction
1	1	Irretrievable error

C2F1	C2F2	C2FL	C2 correction status
0	0	0	No Error
1	0	0	Single error correction
0	1	0	Double error correction
1	1	1	Irretrievable error

CIRCUIT DESCRIPTION

• CLV servo control

The spindle motor revolution is controlled with one selected out of the following seven modes in accordance with a command from the CPU. CLV is the abbreviation of Constant Linear Velocity. The output is composed of MDP terminal for controlling synchronization of velocity and phase, MDS terminal for controlling synchronization of velocity, FSW terminal for making selection of filter constant and MON terminal for controlling motor ON/OFF.

1) STOP : Register E = 0000'B (B means binary)
Mode for stopping the spindle motor.
MDP = FSW = MON = "L", MDS = "Z"

2) KICK : Register E = 1000'B
Mode for running the spindle motor in forward direction.
MDP = MON = "H", MDS = "Z", FSW = "L".

3) BRAKE: Register E = 1010'B
Mode for running the spindle motor in reverse direction.
MDP = FSW = "L", MDS = "Z", MON = "H".

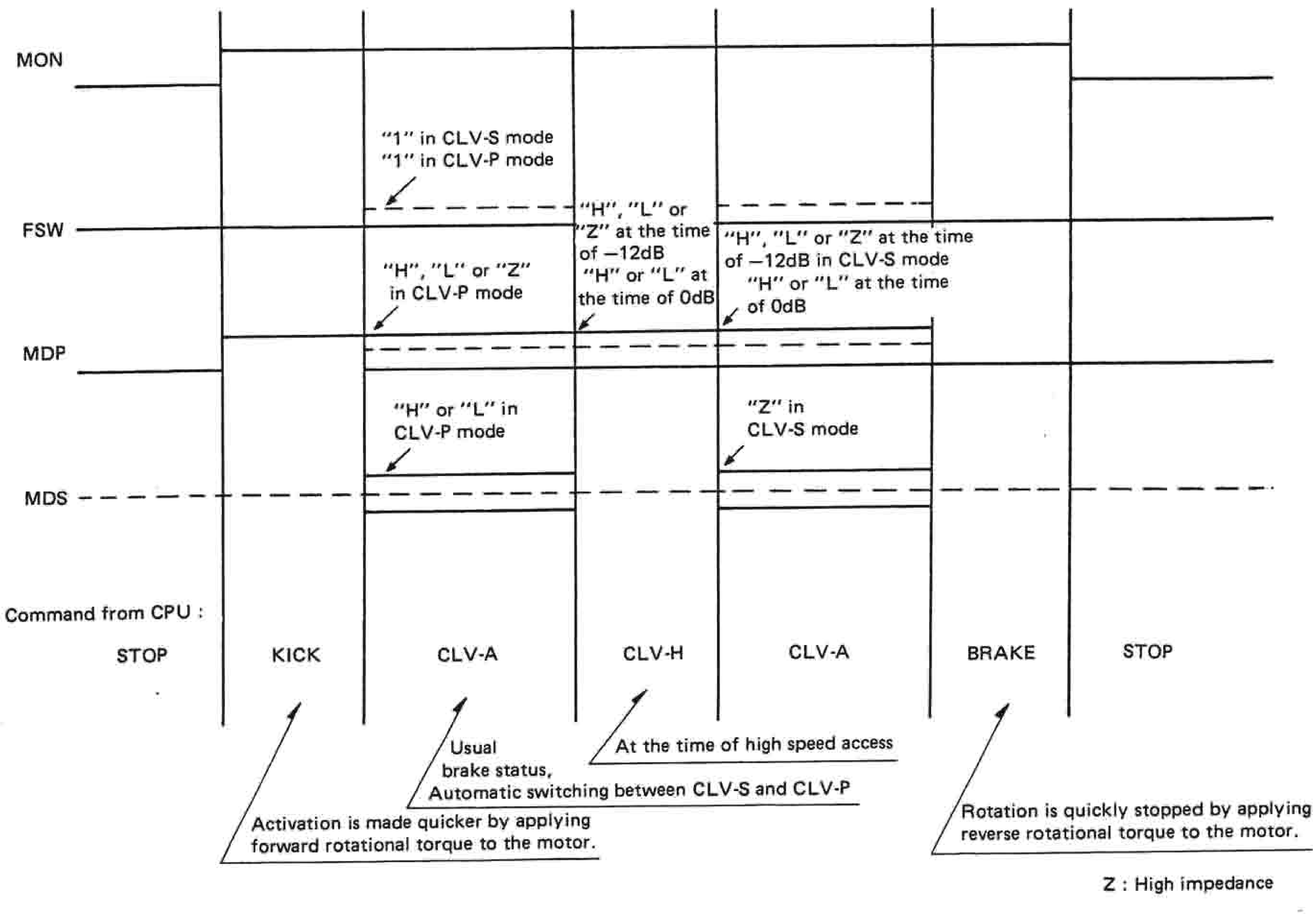


Fig. 9–13 Typical control of spindle motor

CIRCUIT DESCRIPTION

4) CLV-P : Register E = 1111'B

PLL servo mode.

Phase comparison of signals WFCK/4 and RFCK/4 or WFCK/8 and RFCK/8 is made, and output is made out of MDP terminal. "H" when WFCK has delayed, "L" when WFCK is fast, and "Z" when synchronized. When the period of 8.4672/2MHz is expressed at T and the length of time when WFCK is "H" is expressed at tHW, such a signal that is of "H" during (tHW−279T) x 32 with 7.35kHz as a period and that is "L" during the remaining time is produced out of MDS terminal. MDS = "L" when tHW ≦ 279T. MDS = "H" when tHW ≦ 297T. When 280T ≦ tHW ≦ 296T, the MDS terminal changes in 32T steps from 32T to 544T. When synchronized, for instance, that is, when tHW = 288T, a signal of 7.35kHz of DUTY 50% is produced. FSW = "Z", MON = "H".

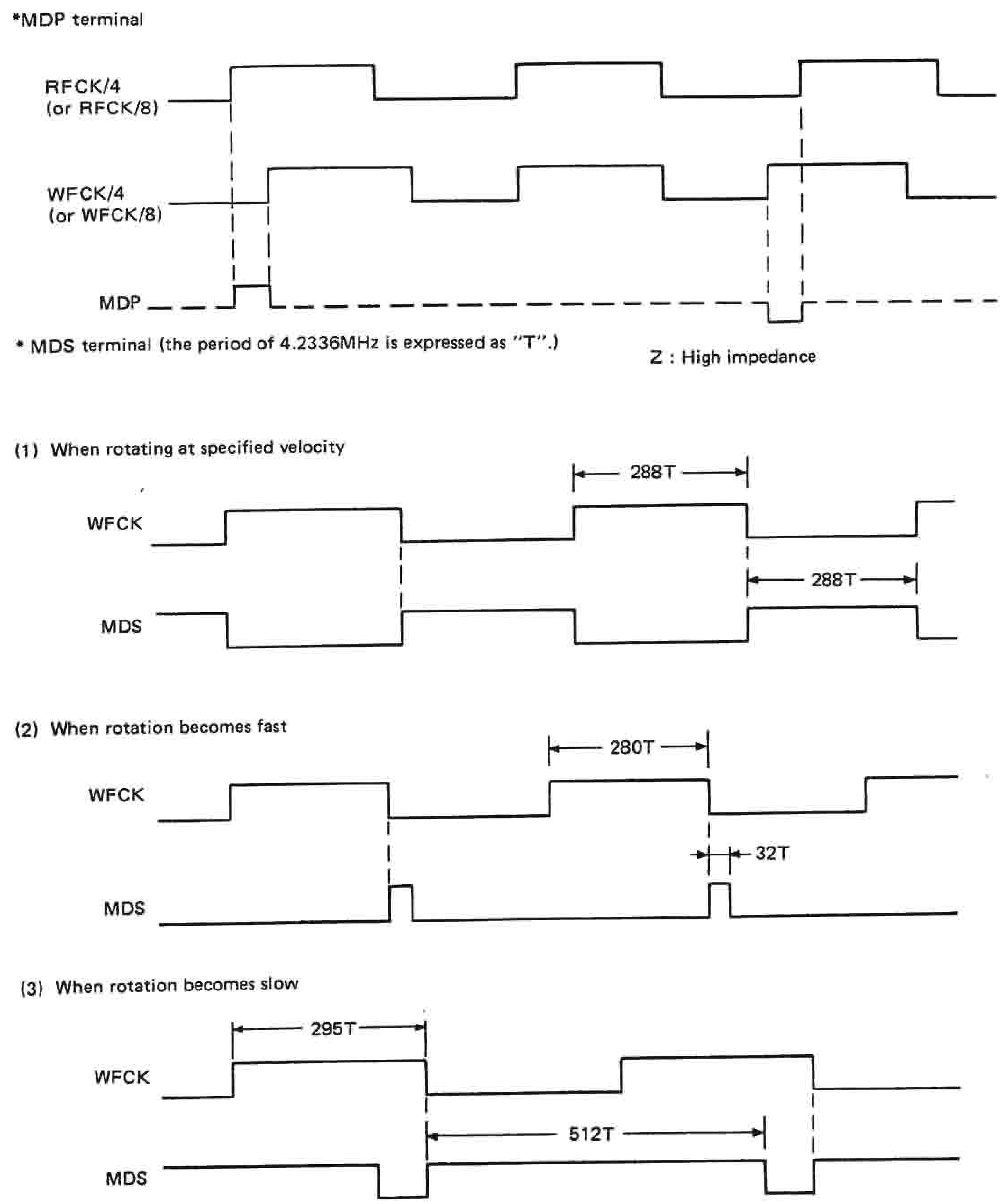


Fig. 9–14 Timing chart in CLV-P mode

5) CLV-S : Register E = 1110'b
Rough servo mode used at the time of start of rotation, at the time of track jump and also when the EFM-PLL circuit is unlocked due to another reason. When the period of VCO's oscillation frequency 8.6436MHz is expressed as "T", the pulse width of a frame synchronizing signal is "22T" during specified revolution, and it is the maximum pulse width in a period of RFCK. In practive, however, there are pulses having widths over "22T" due to drop-off of EFM signal due to other reasons, and the frame synchronizing signal cannot be correctly detected unless such pulses are removed. Therefore, the maximum value (peak) of the pulse width of EFM signal is detected (called peak hold) in the period of RFCK/2 or RFCK/4, than the minimum value in this peak is detected (called bottom hold) in the period of RFCK/16 or RFCK/32, and this value is used as the frame synchronizing signal. "L" is produced out of MDS terminal while the frame synchronizing signal is "21T" or less, "Z" when it is "22T", or "H" when it is "23T" or more.
Either 0dB or 12dB can be selected as its gain.
MDS = "Z", FSW = "L", MON = "H"

6) CLV-H : Register E = 1100'B
Rough servo mode during high speed access. If the number of tracks from the innermost periphery to the outermost periphery is 2000 tracks and access over these tracks is made in 1 second, each mirror (place without pit) portion between tracks is of a signal of 20kHz, andis superposed on the EFM signal. When the above mentioned signal is input in the CLV-S mode, a mirror portion that is longer than the original frame synchronizing signal is detected as the peak value, and servo becomes unstable. In the CLV-H mode, therefore, the mirror portion is eliminated by making peak hold in the period of 8.4672/256MHz about 34kHz) instead of RFCK/2 or RFCK/4 and by making bottom hold in the period of RFCK/16 or RFCK/32 like in CLV-S mode, and thus the servo during high speed access is made stable. Other than the period for detection of the peak is same as CLV-S mode.

Pwmax : Pulse width after bottom hold
TB : Bottom hold period, RFCK/16 or RFCK/32
Z : High imepdance

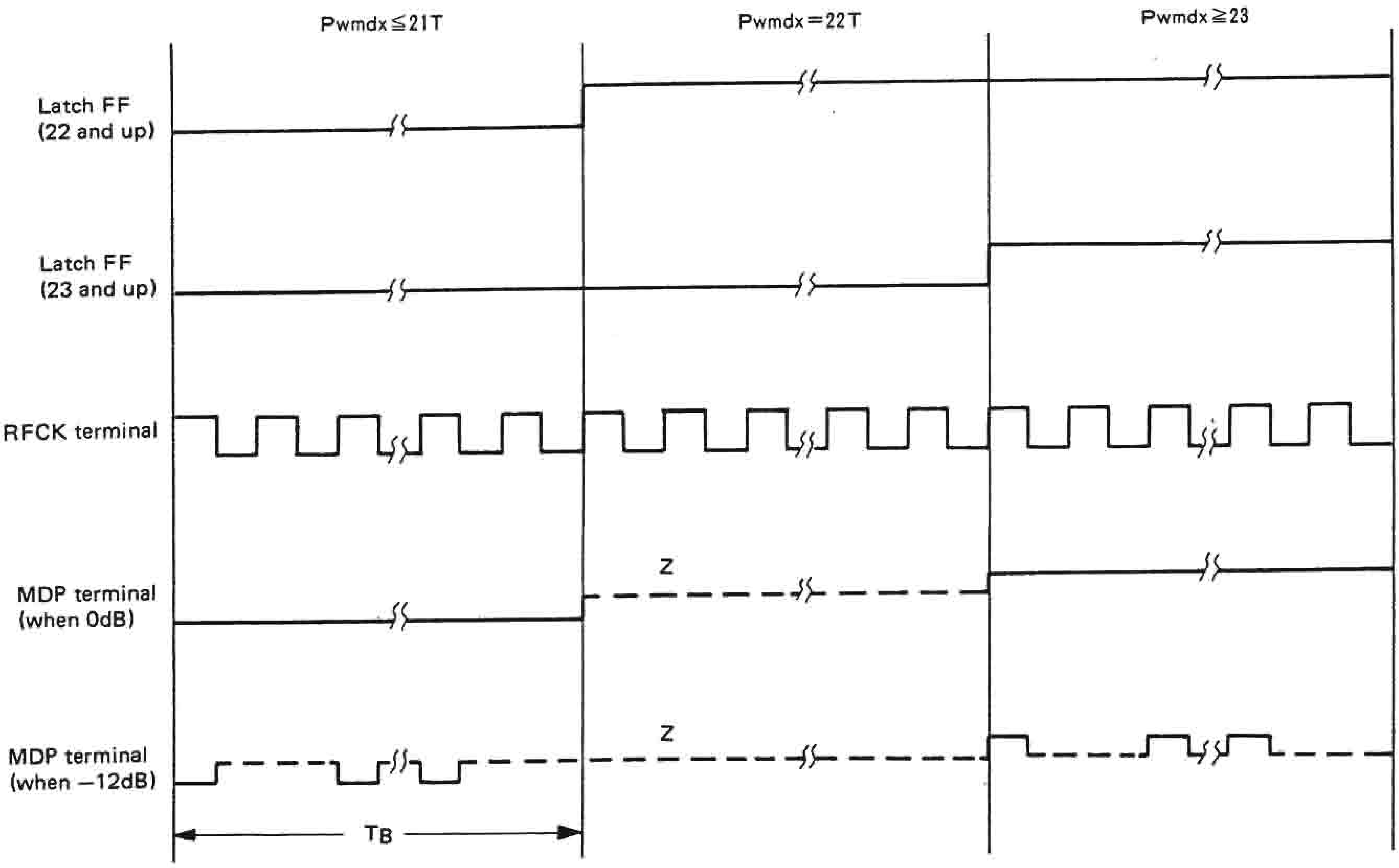


Fig. 9–15 Timing chart in CLV-S, CLV-H mode (1)

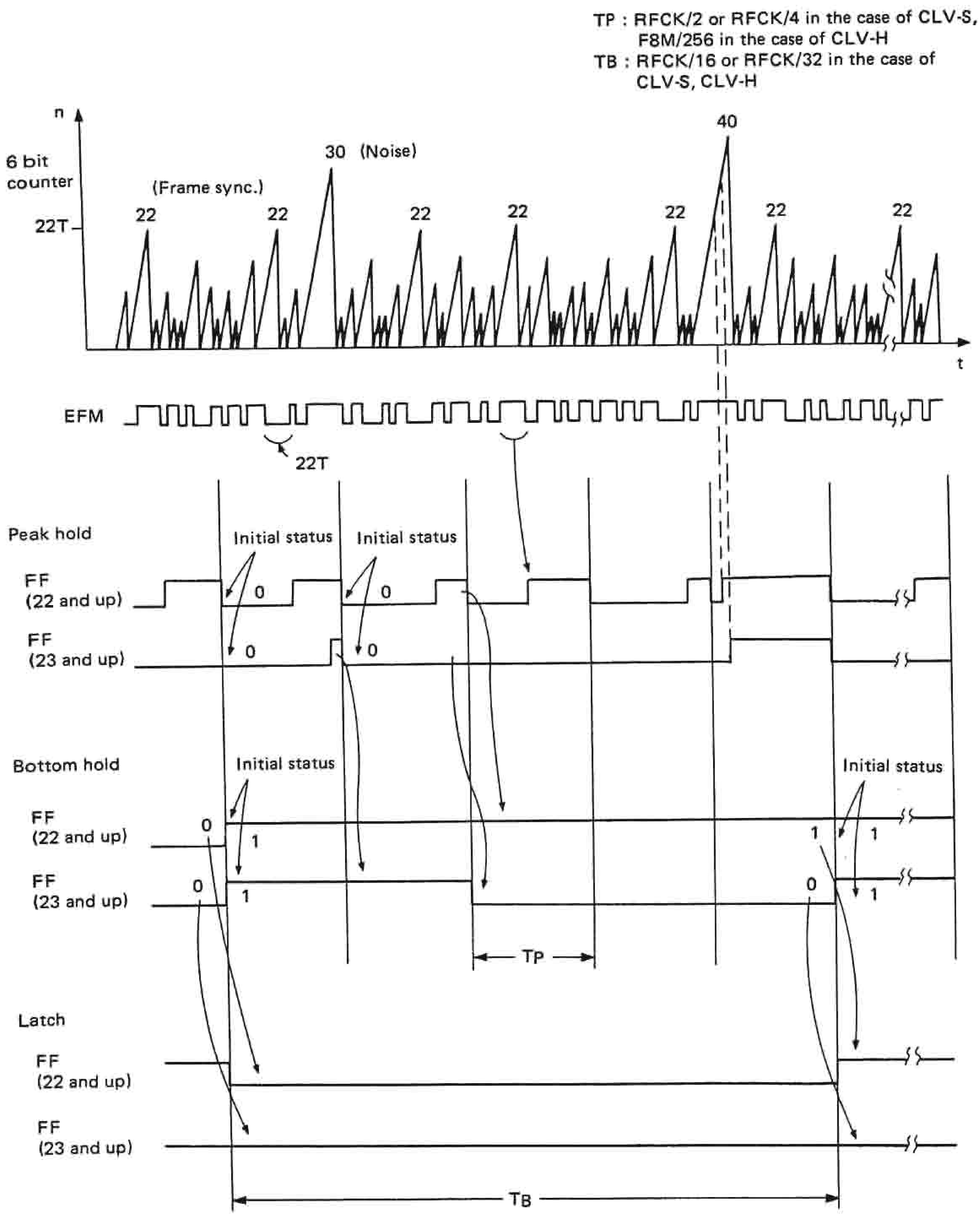


Fig. 9–16 Timing chart in CLV-S, CLV-H mode (2)

7) CLV-A : Register E = 0110'B

Mode used during usual play.

Samples GFS signal ("H" when locked; "L" when unlocked) from the frame sync. detection, protection and interpolation block by WFCK/16, and operates in CLV-P mode in the case of "H". In the case where "L" level is continued for eight times, switching is made to CLV-S mode automatically. Period setting of peak hold in CLV-S mode, bottom hold period setting and gain setting in CLV-S, CLV-H mode and setting of the frequency dividing ratio in CLV-P mode are made by register D, and mode selection is made by register E. The details of these registers will be explained in the section of CPU interface.

Note : Output is made out of DA07 terminal when PSSL = "L" with WFCK/4 or WFCK/8 as FCKV, and output is made out of DA08 terminal with RFCK/4 or RFCK/8 as FCKX.

10. CD over-sampling digital filter LSI (IC16, CX23034)

10–1. Functions

This LSI component provides the following functions:

- Over-sampling digital filter
- 8.4672 MHz clock generation (for use by the CX23035).
- 16-bit serial data input (directly coupled from the CX23035).
- Interface with the D/A converter.
- Overflow limiter.

10–2. Features

- Filter structurre : Capable of processing stereo signal with a single chip.
  Conversion at a doubled rate.
  16-bit coefficient 96th degree FIR type.
- Provides compensation
- Filter characteristics :
  Linear phase
  Pass band ripple : ±0.01 dB or below
  Rejection band attenuation : 80dB or above
- Provides compensation against D/A converter apperture effect (f-characteristics compensation).
- Capable of interfacing with a 16-bit serial input D/A converter.

10–3. Package type

24pin dual in line.

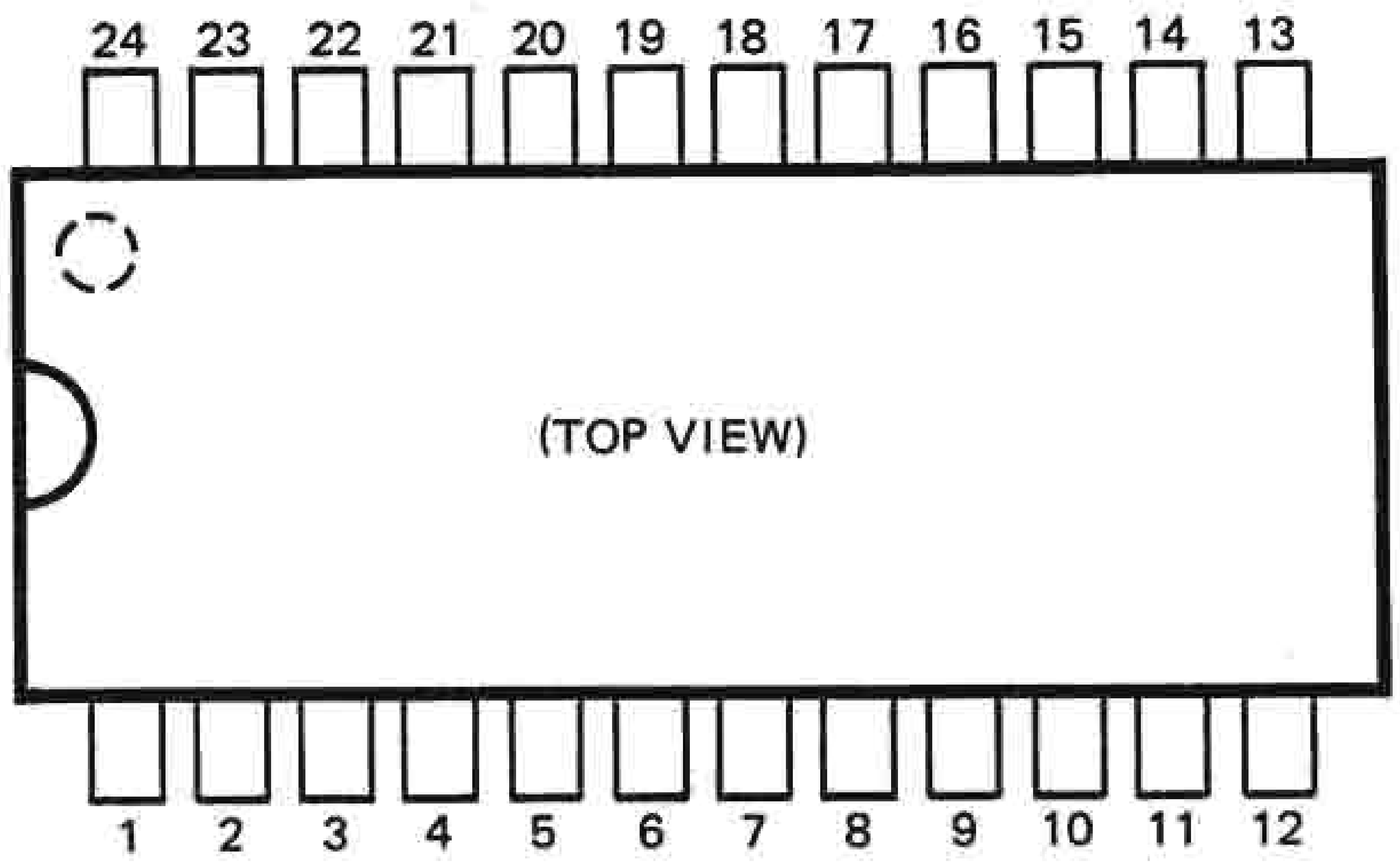


Fig. 10–1

10–4. Internal block diagram

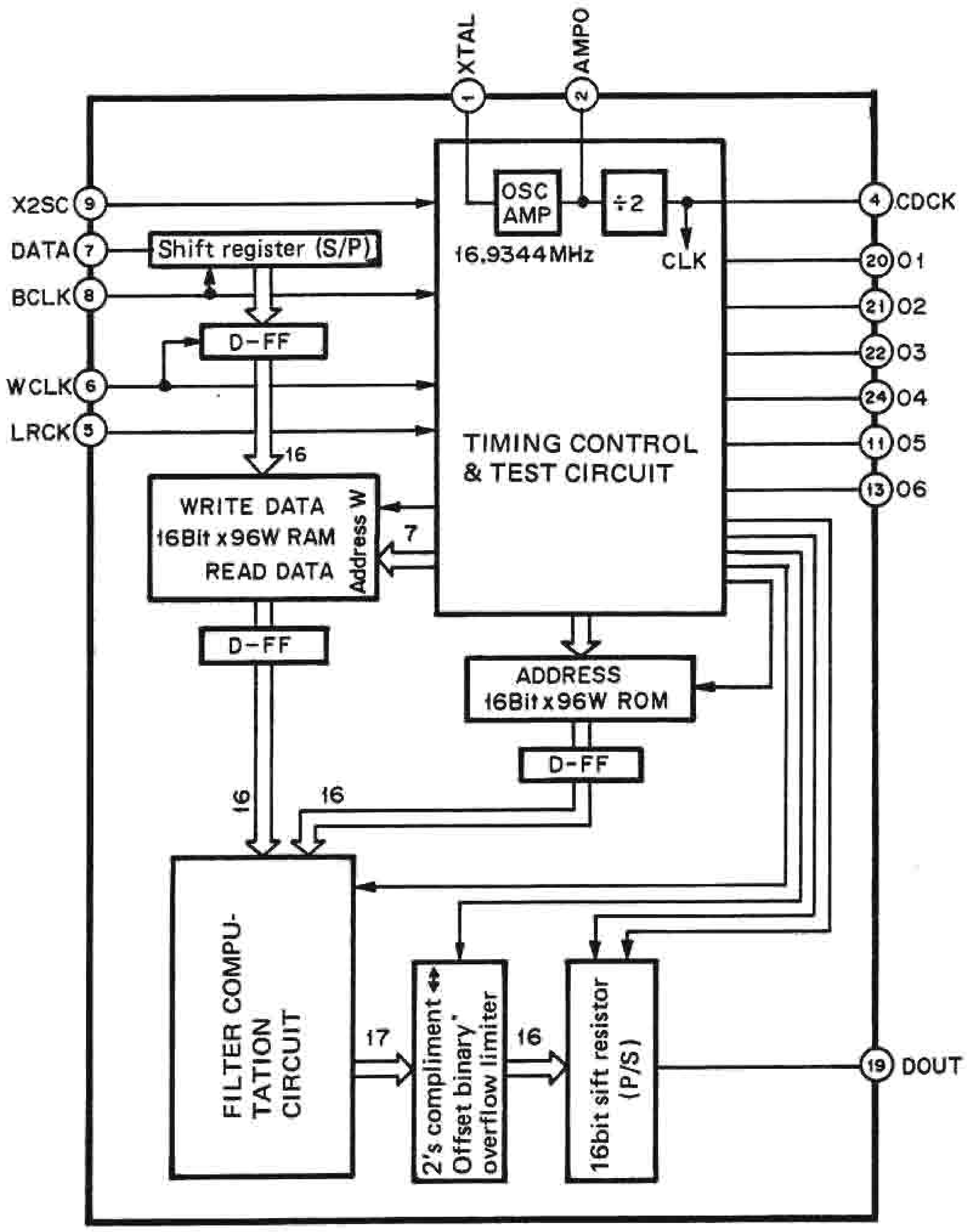


Fig. 10–2

10–5. CX23034 Terminals and their functions

Terminal No.	Terminal name	I/O	Function
1	XTAL	I	Crystal oscillator (16.9344MHz) input.
2	AMPO	O	Crystal oscillator (16.9344MHz) output.
3	TEST 1	I	Test input (normally connected to Vss).
4	CDCK	O	Clock output (8.4672MHz).
5	LRCK	I	44.1kHz strobe input.
6	WCLK	I	88.2kHz strobe input.
7	DATA	I	Serial data input (2's complement, MSB first).
8	BCLK	I	Bit clock input (for serial data input).
9	X2SC	I	Output mode selection input ("H" : offset binary, "L" : 2's complement).
10	TEST 2	I	Test input (normally connected to Vss).
11	O5	O	Timing signal.
12	Vss	–	GND terminal (0V).
13	O6	O	Timing signal.
14	TEST 3	O	Test data output (normally open).
15	TEST 4	O	Test data output (normally open).
16	TEST 5	O	Test data output (normally open).
17	TEST 6	O	Test data output (normally oepn).
18	TEST 7	O	Test data output (normally open).
19	DOUT	O	Serial data output (MSB first).
20	O1	O	Timing signal.
21	O2	O	Timing signal.
22	O3	O	Timing signal.
23	O4	O	Timing signal.
24	VDD	–	Power supply terminal (+ 5V).

Note : The frequencies are specifically for use in the DP-2000 CD player.

Table 10–1

10–6. DATA,SCLK,WCLK, and LRCK signal timing

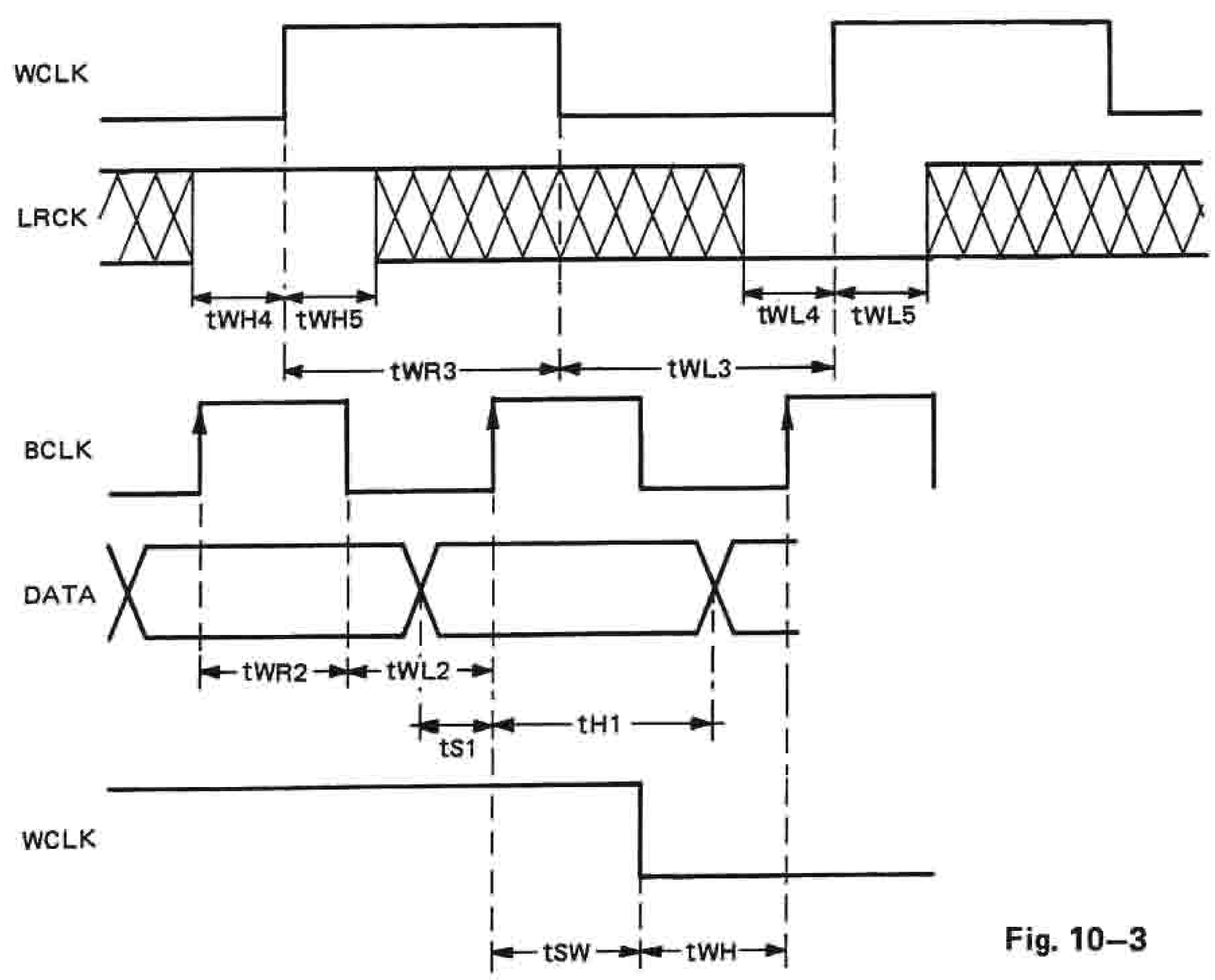


Fig. 10–3

CIRCUIT DESCRIPTION

10–7. Timing chart

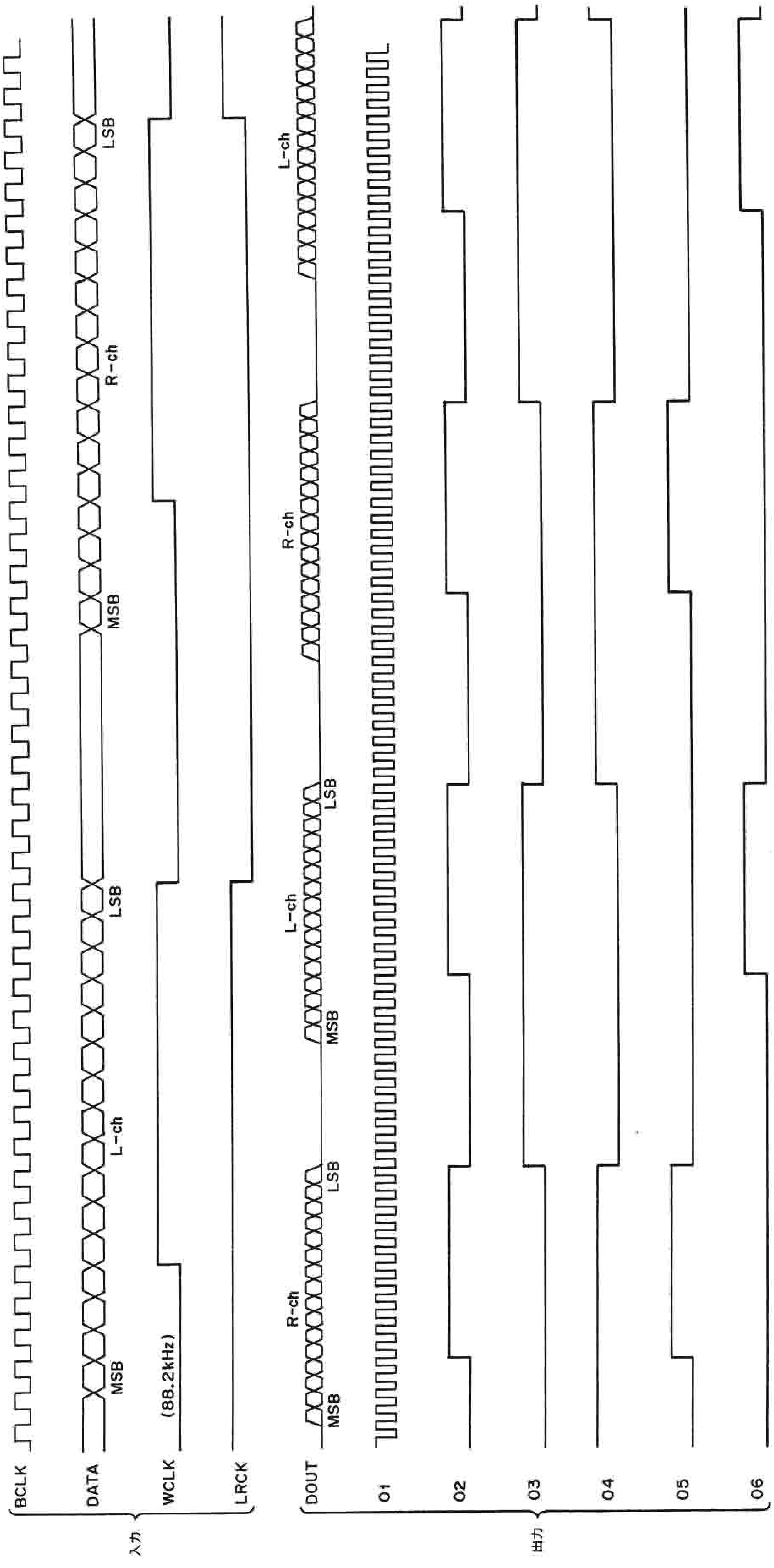


Fig. 10–4

CIRCUIT DESCRIPTION

11. D/A converter (CX20152)

11–1. Internal block diagram

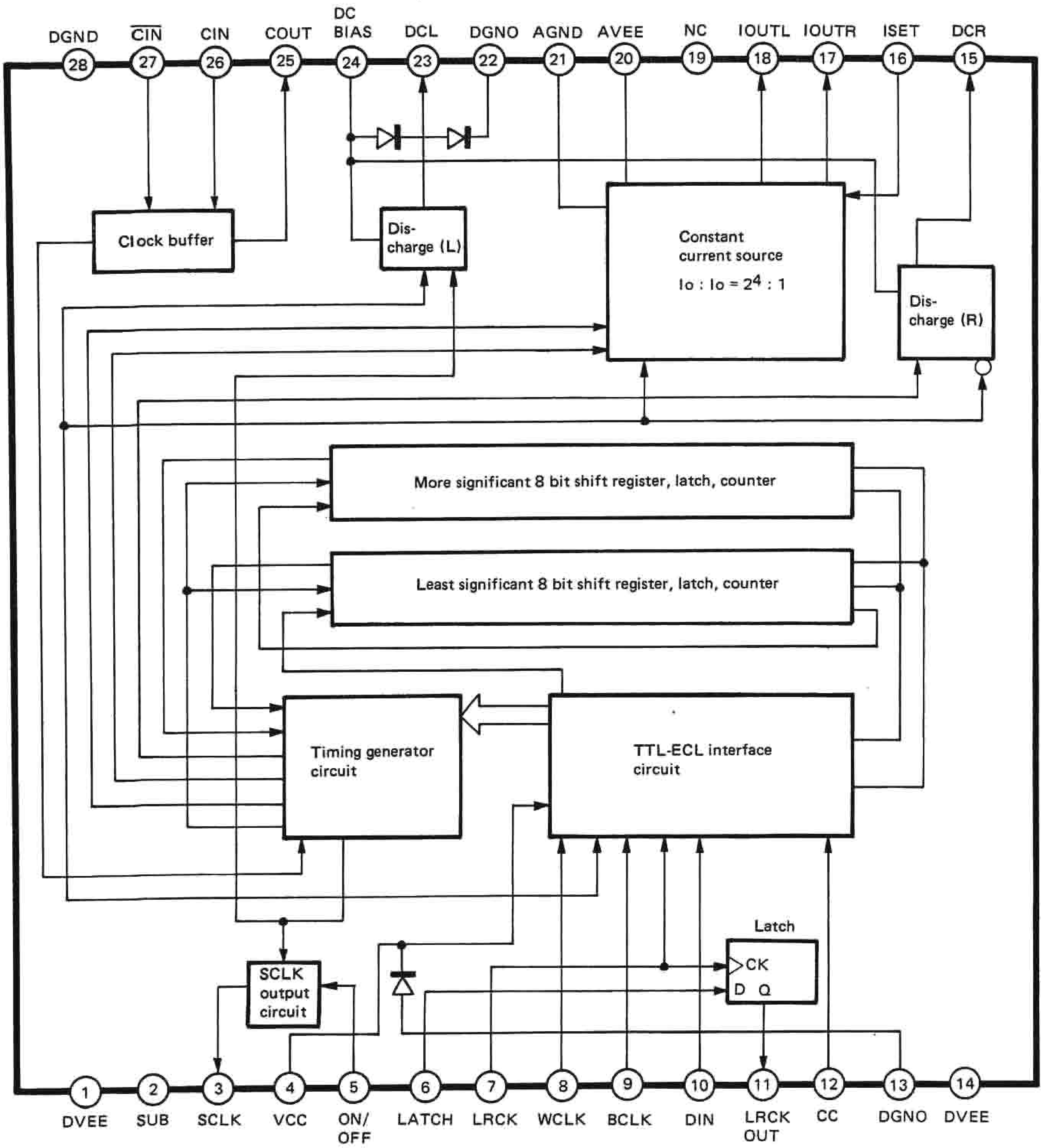


Fig. 11–1

CIRCUIT DESCRIPTION

11–2. Explanation of converting operation

- **Data calling (BCLK, DIN, WCLK, LRCK)**

Each data is a 16 bit serial signal and is of 2's complement form. Data are sequentially fed into the IC beginning with MSB in synchronization with rising edge of a bit clock (BCLK). (Data change occurs at falling edge of BCLK.)

When word clock (WCLK) is changed from high level to low level at 17th falling edge of BCLK, the 16 bit data is transmitted from the shift register to the latch by this falling edge signal. In the case where CX20017 is used in the stereo mode, data of another channel is fed in beginning at the 17th BCLK.

Allocation of data in the stereo mode is such that R-ch data is called in while LRCK is of low level and L–ch data is called in while LRCK is of high level. Further, IOUTL, DCL operate when LRCK is of low level, and IOUTR, DCR operate only when LRCK is of high level.

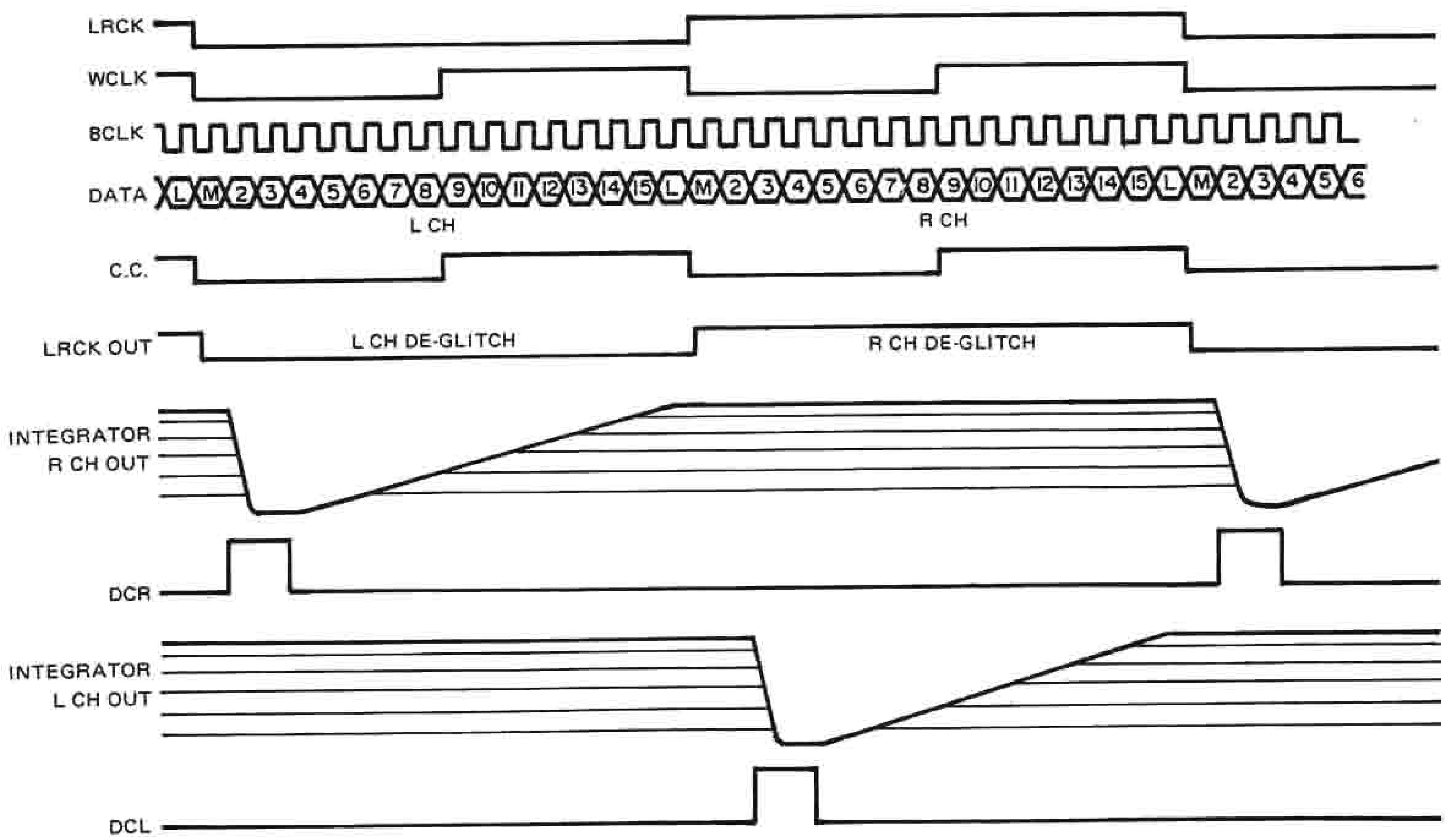


Fig. 11–2

- **Converting operation (CC, LRCK, CIN, IOUTL, IOUTR, DCL, DCR)**

All of the internal timing circuits are reset when the conversion command (CC) is set at high level and three or more clocks are fed through the clock input (CIN).

The internal timing circuits start operation CC is set at low level and a clock is fed through CIN after reset. The signals generated by operation of internal timing circuits are discharge signal, counter set signal and integration current start signal. The times of these signals are determined as follows from the clock period and number of clocks.

$t_1 = 34 \times \tau_0$

$t_2 = 67 \times \tau_0$

$t_3 = 31 \times \tau_0$

$t_4 = 65 \times \tau_0$

$t_5 \min = 47 \times \tau_0$ (when input data is 01~1)

$t_5 \max = 302 \times \tau_0$ (when input data is 10~1)

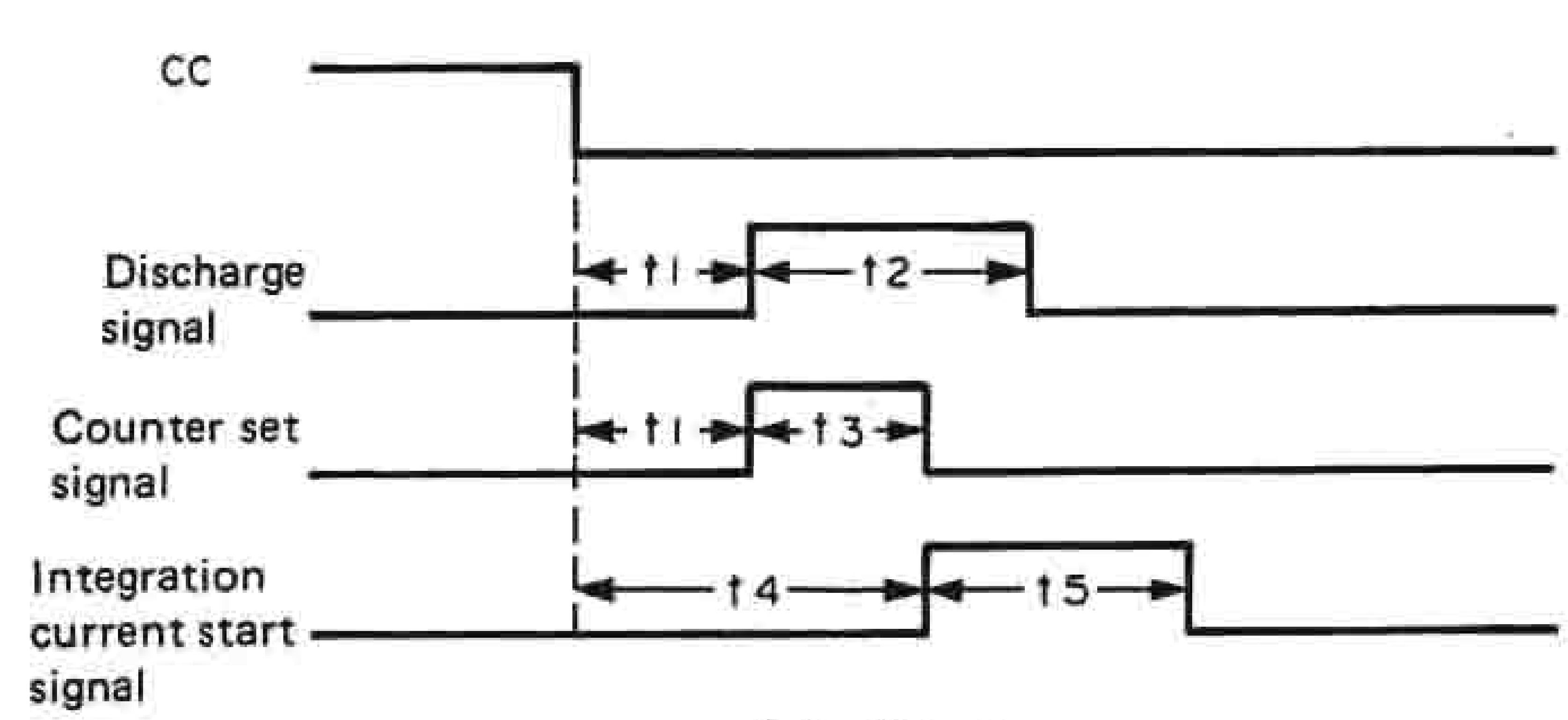


Fig. 11–3

CIRCUIT DESCRIPTION

The counter set signal is used for setting in counter the data that entered the latch, and it is not directed to the exterior. The discharge signal is directed out of DCL DCR. That is, it is directed out of DCL while LRCK is of low level or out of DCR while LRCK is of high level.

Most significant current Io and least significant currant io flow out with an integration current start signal. The counter starts counting simultaneously with OFF of the discharge signal, and after finishing counting, it counts 11 offsets and issues a signal to stop the integration current. The value of t5 varies between 0 and 255 depending on the input data value preset in the counter.

Therefore, the length of time required since CC level was changed to low level until end of integration, that is, conversion, is (t4 + t5 max.) seconds at maximum. Further, as for this integration current, IOUTL is output while LRCK is of low level and IOUTR is output while LRCK is of high level, like the discharge signal.

- **Setting of integration current (SET, IOUTL, IOUTR)**

The integration current is determined by the constant current value fed from the ISET terminal. The relation is as follows.

$$\mathrm{IOUTL(R)} = \mathrm{I_0} + \mathrm{i_0} = (4 + \frac{1}{64})\,\mathrm{1SET}$$

Where; io is the integration current that is equivalent to ILSB, and Io is the integraiton current that is equivalent to $2^8 \cdot$ LSB.

- **Operation of LRCK OUT (LATCH, LRCK, LRCK OUT)**

The output of LRCK OUT is the output for driving the analog switch IC12 (NJM4558D) to cut the output which was converted by CX20017 and the integrator as a PAM wave.

A conversion error occurs if jitter is present in the PAM wave. In order to absorb this jitter, therefore, D type flip-flop is incorporated, and LATCH input is used as its clock. This D type flip-flop causes a change in the output status in synchronization with raising edge a clock.

This LRCK OUT operates only when + 5V is impressed to VCC. Its output level is –3V~+ 3V.

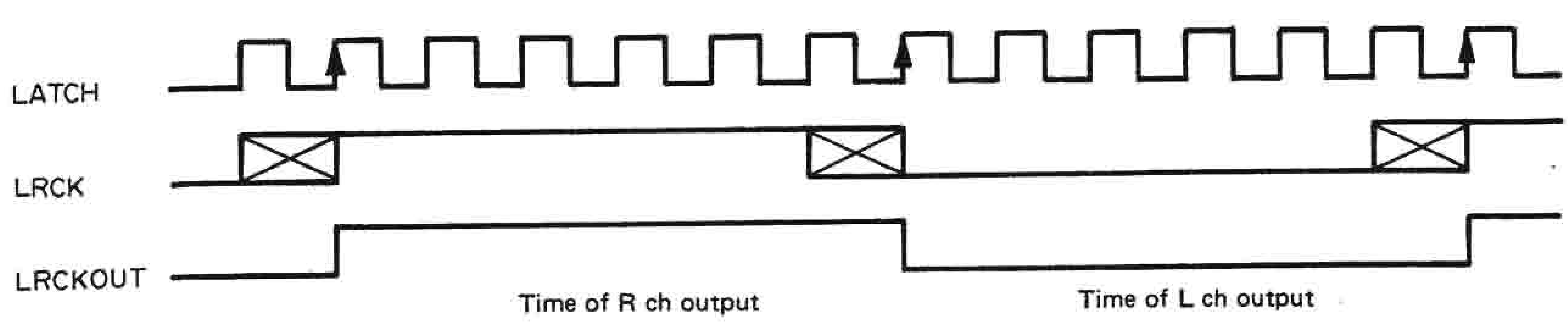


Fig. 11–4 Timing chart of LATCH, LRCK, LRCKOUT

- **Clock input/output terminals (COUT, CIN, $\overline{\mathrm{CIN}}$)**

The clock buffer is composed of a circuit that is equivalent to a general-purpose ECL logic circuit, and the input terminal is biased by an internal circuit. The (≈ –1.3 V) output amplitude level is 0.8V

- **Bias terminals (DVEE, SUB, DGND, VCC, AVEE, AGND, DC BIAS)**

SUB is the substrate for the IC and is used at the potential common with ADVEE. The standard value of DVEE, AVEE is –5.0V. This CX20017 is used with the voltage at VCC terminal raised to + 5V in order to cause the input to operated at 0~+ 5V. Further, LRCK OUT is output in this case as described earlier. BC BIAS is the bias circuit of the discharge signal output circuit.

As a current of about 2.5mA is required at standard value, power is supplied from IC15. The potential of this terminal is biased at 2Vf.

CIRCUIT DESCRIPTION

12. Remote control microprocessor (LM6416E-504)

12–1. Terminal connection

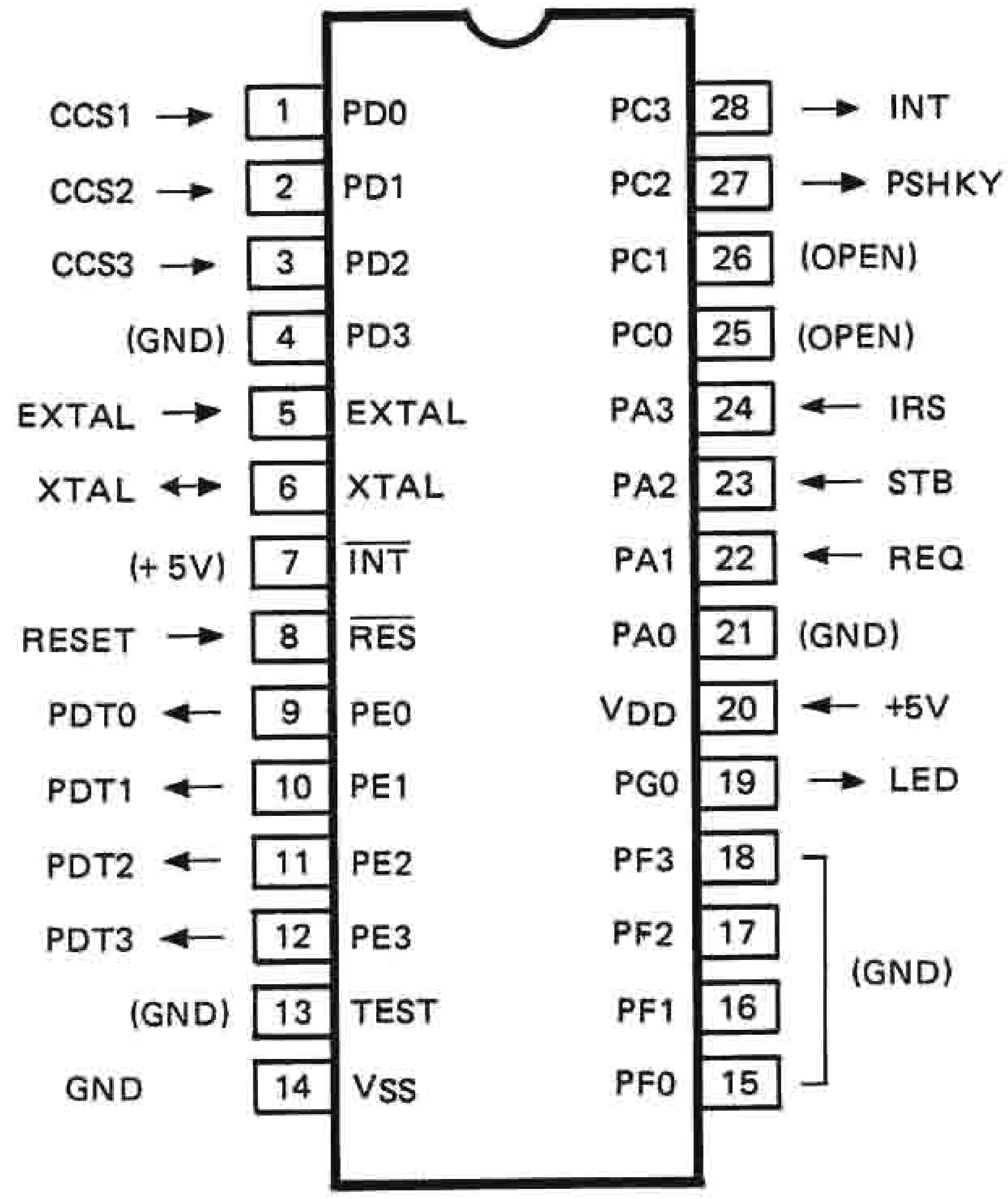
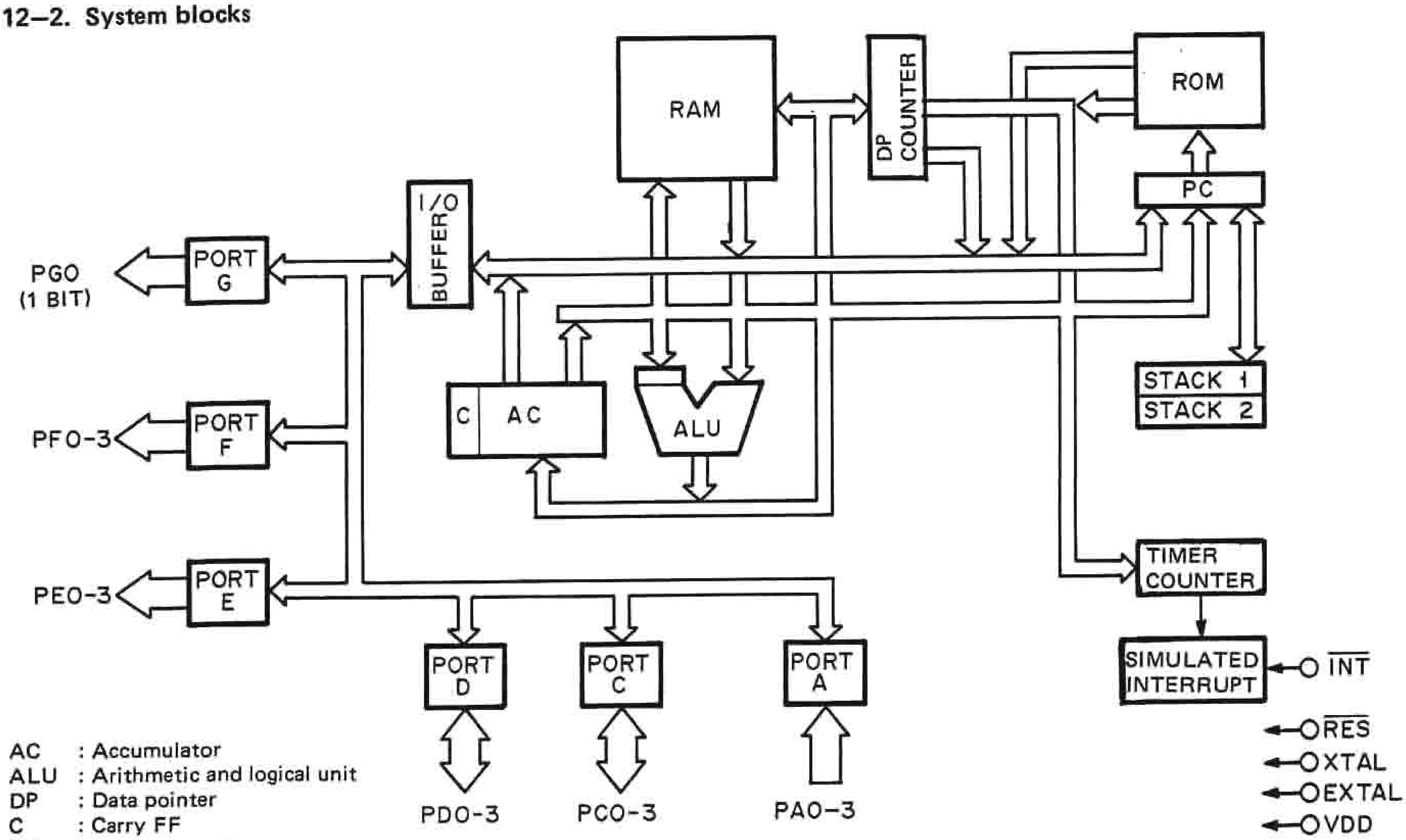


Fig. 12–1

12–2. System blocks



AC : Accumulator
ALU : Arithmetic and logical unit
DP : Data pointer
C : Carry FF
PC : Program counter

Fig. 12–2

12–3. Terminals and their functions

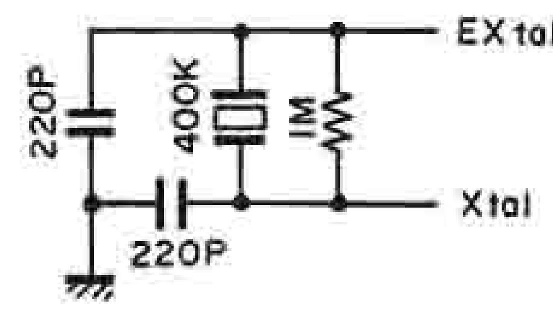
Terminal No.	Port name	Signal name	I/O	Function
1	PD0	CCS1	I	Custom code. Since all CD players use a custom code B6H, CCS1 and CCS3 are fixed at "L" and CCS2 is fixed at "H".
2	PD1	CCS2	I	
3	PD2	CCS3	I	
4	PD3		I	Connect to GND.
5	EXtal	EXTAL	I	Crystal oscillator terminals. 
6	Xtal	XTAL	I/O	
7	$\overline{\text{INT}}$		I	Fix at "H".
8	$\overline{\text{RES}}$	RESET	I	Reset input (open).
9	PE0	PDT0	O	Parallel data code output port (LSB).
10	PE1	PDT1	O	Parallel data code output port.
11	PE2	PDT2	O	Parallel data code output port.
12	PE3	PDT3	O	Parallel data code output port (MSB).
13	TEST		I	LSI test terminal. Connect to GND.
14	Vss	GND	–	Connect to GND.
15	PF0		O	Connect to GND.
16	PF1		O	Connect to GND.
17	PF2		O	Connect to GND.
18	PF3		O	Connect to GND.
19	PGO	LED	O	Activated "H" during remote control code reception.
20	VDD	+5V	I	Power supply terminal (+5V).
21	PA0		I	Connect to GND.
22	PA1	REQ	I	Fixed at "H".
23	PA2	STB	I	Strobe pulse for the μPD7516 to read remote control code.
24	PA3	IRS	I	Input signal from the remote control premaplifier.
25	PC0		O	Leave open.
26	PC1		O	Leave open.
27	PC2	PSHKY	O	"H" while a remote control key is depressed.
28	PC3	INT	O	Leave open.

Table 12–1

12–4. Remote control microprocessor (LM6416E-504) and peripheral circuits

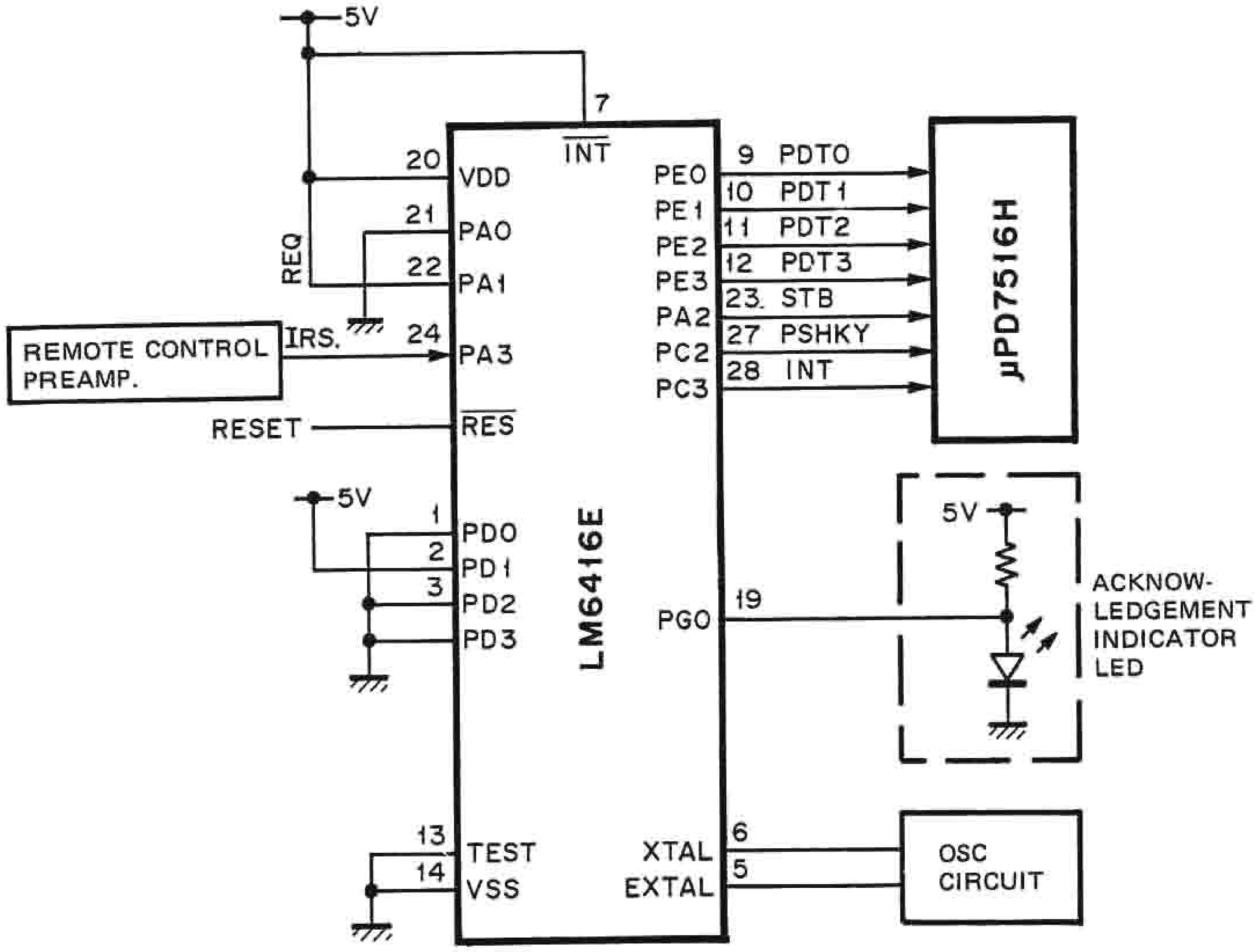


Fig. 12–3

12–5. LM6416E and μPD7516H Communication control signal timing chart

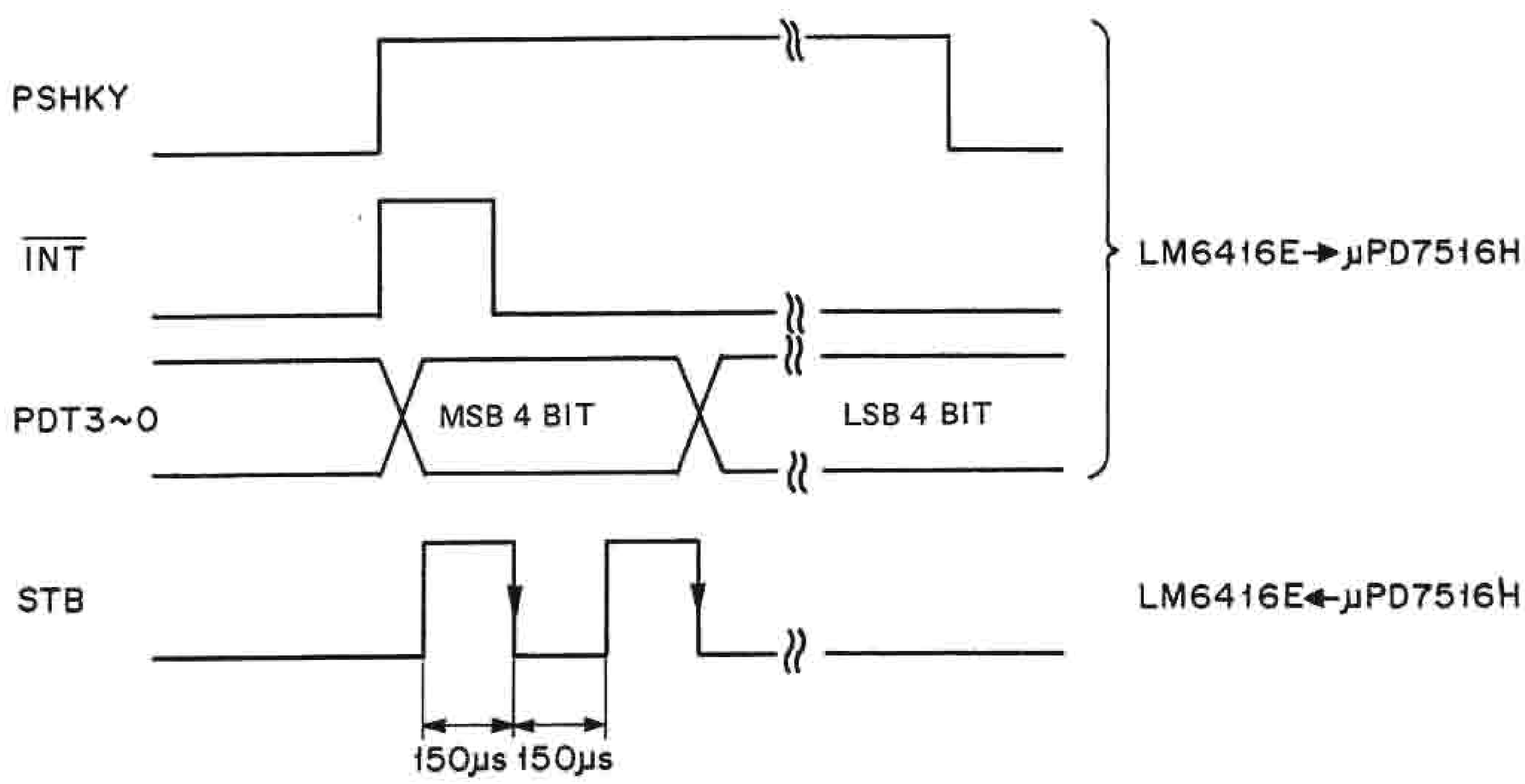


Fig. 12–4

ADJUSTMENT

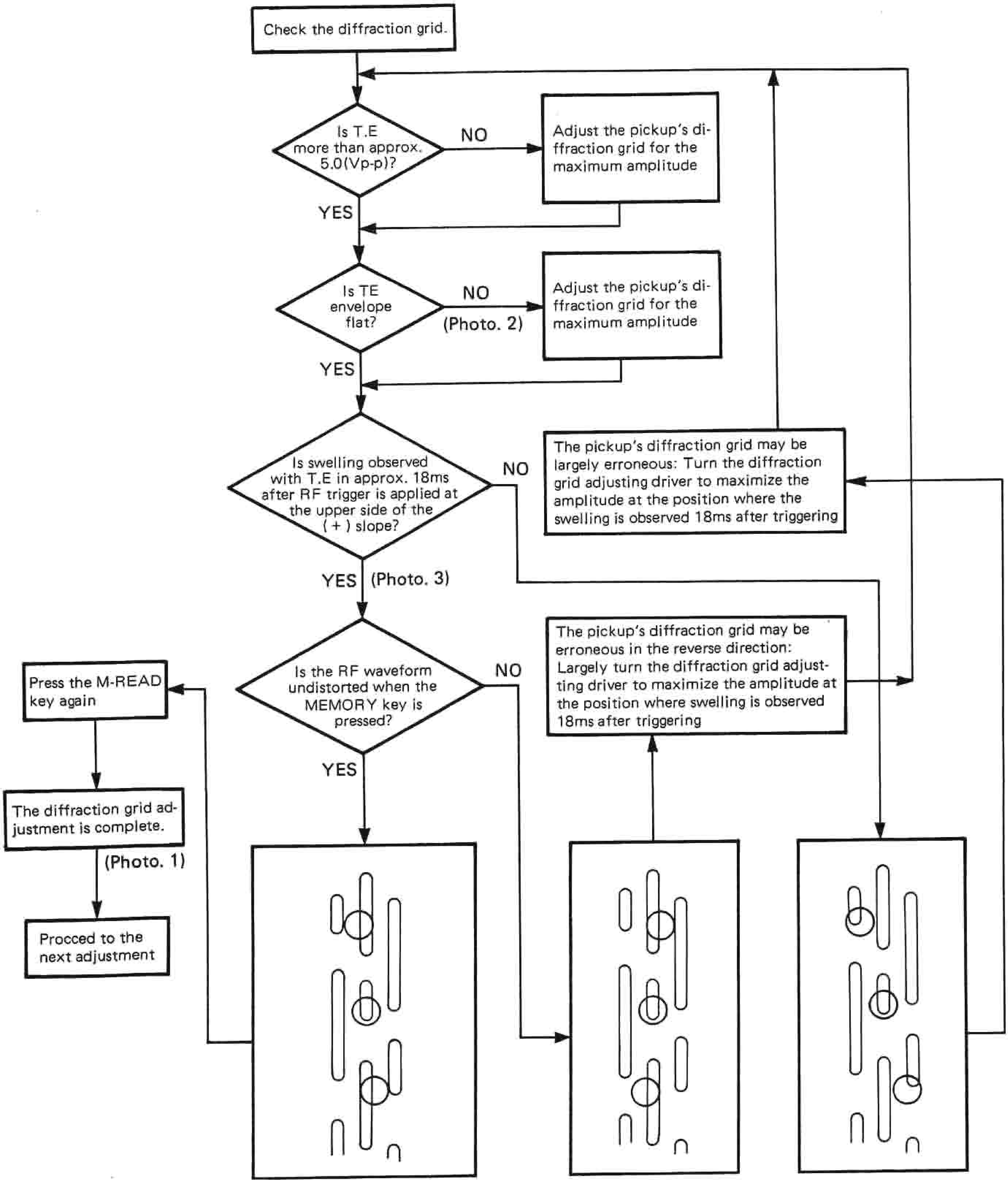
No.	ITEM	INPUT SETTING	OUTPUT SETTING	PlAYER SETTING	ALIGNMENT POINT	ALIGN FOR	FIG
1	VCO ADJUSTMENT	–	Connect an f-counter across CN17 and GND.	Tray open, or stop mode	Turn core of coil of L2 of X32-1040(B/5)	4.23MHz	(a)
2	LASER POWER CHECK (When PU may be defective)	–	Set an optical power meter above the pickup.	Tray - open. Connect the base of Q7 of X32-1040(A/5) to the GND.	–	OK if from 200μW to 300μW.	(b)
3	LASER OPERATING CURRENT CHECK (When PU may be defective)	–	Measure the voltage across two ends of R4 of X32-1040(A/5).	Tray - open. Connect the base of Q7 of X32-1040(A/5) to the GND.	–	Acceptable when larger by 5 to 6mA then the current marked on the pickup.	(c)
4	RF OFFSET ADJUSTMENT	–	Connect an oscilloscope to TP2(RF) of X29-1632(B/6). Connect the scope's GND to TP1(GND).	Tray open, or stop mode.	Turn VR5 of X29-1632(B/6). (RF OFFSET)	Adjust to -0.60(V).	(d)
5	TEST MODE SETUP	Place test disc Type 3 on the tray and set the unit to the loaded condition.	Short-circuit between TP12 and TP13 of X32-1040(A/5).	Turn POWER SW OFF then ON again.	–	Check that the display is "01 oo 00:00"	(e)
6	TANGENTIAL SETTING	Place test disc Type 3 on the tray and set the unit to the loaded condition.	Connect and oscilloscope to TP2(RF) of X29-1632(B/6).	Press M-READ, and laser is focused. (In the test mode.)	Hex socket screw below mechanism	Maximum amplitude	(d)
7	FOCUS OFFSET COARSE ADJUSTMENT	Place test disc Type 3 on the tray and set the unit to the loaded condition.	Connect and oscilloscope to TP2(RF of X29-1632(B/6).	Press M-READ, and laser is focused. (In the test mode.)	Turn VR3 of X29-1632(B/6).	Maximum amplitude	(d)
8	**(When PU may be defective)** DIFFRACTION GRID ADJUSTMENT (PU)	Place test disc Type 3 on the tray and set the unit to the loaded condition.	Connect CH1 of oscilloscope to TP2(RF) of X29-1632(B/6), and CH2 to TP3(TE).	Press M-READ, and laser is focused. (In the test mode.)	Pickup adusting hole- Use the grid driver.	See Fig. 1.	(f)
9	T. ERROR BALANCE COARSE ADJUSTMENT	Place test disc Type 3 on the tray and set the unit to the loaded condition.	Connect CH1 of oscilloscope to TP2(RF) of X29-1632(B/6), and CH2 to TP3(TE).	Press M-READ, and laser is focused. (In the test mode.)	Turn VR4 of X29-1632(B/6).	Adjust so that the T. ERROR amplitude is symmetrical above and below 0(V). (Photo 5)	(f)
10	TANGENTIAL AND FOCUS OFFSET FINE ADJUSTMENTS	Place test disc Type 3 on the tray and set the unit to the loaded condition.	Connect and oscilloscope to TP2(RF of X29-1632(B/6).	Press the PLAY Key. (The unit starts the trace operation.) (In the test mode.)	VR3 of X29-1632(B/6), and hex socket screw above mechanism	Alternately turn VR3 and hex socket screw to obtain optimum waveform.	(d)
11	T. ERROR BALANCE FINE ADJUSTMENT	Place test disc Type 3 on the tray and set the unit to the loaded condition.	Connect CH1 of oscilloscope to TP2(RF) of X29-1632(B/6), and CH2 to TP3(TE).	Press the M-READ Key (with focus servo only). (In the test mode.)	Turn VR4 of X29-1632(B/6).	Adjust so that the T. ERROR amplitude is symmetrical above and below 0(V). (Photo 5)	(f)
12	FOCUS GAIN ADJUSTMENT	Place a test disc which is as flawless as possible, and complete loading.	Connect a servo-adjusting jig to CN4 of X29-1632. (f=1.0kHz, V OUT=40mVrms)	Trun POWER SW OFF then ON again, and press the PLAY key to start normal play.	Trun VR2 of X29-1632(B/6).	Adjust so that the millivoltmeter connected to the jig indicates 40mVrms.	(g)
13	TRACKING GAIN ADJUSTMENT	Place a test disc which is as flawless as possible, and complete loading.	Connect a servo-adjusting jig to CN4 of X29-1632. (f=1.0kHz, V OUT=40mVrms)	Normal play	Trun VR1 of X29-1632(B/6).	Adjust so that the millivoltmeter connected to the jig indicates 40mVrms.	(g)
14	DAC ADJUSTMENT	Test disc YDS-7 Type 3	Connect a millivoltmeter to the output terminal.	Play 1kHz, 0dB signal.	Trun VR2 of X32-1040(A/5).	Adjust to obtain the output level from 1.9 to 2.0Vms.	(h)

ADJUSTMENT

Diffraction grid adjustment

Adjust in the test mode (with focus servo only)

Note : The test mode is the condition in which power is turned on after short-circuiting between TP12 (TEST-12) and TP13 (D.GND-13) in the signal processing unit (X32-1040-00) (A/5).



When diffraction grid adjustment is complete

Diffraction grid adjustment error (reverse direction)

Diffraction grid adjustment error (large error in forward-direction)

Fig. 1

REGLAGE

N°	ITEM	REGLAGE D'ENTREE	REGLAGE DE SORTIE	REGLAGE DE LA LE CTURE	POINT D'ALIGNEMENT	ALIGNEMENT POUR	FIG
1	RÉGLAGE VCO	—	Raccorder un compteur f entre CN17 et GND	Tiroir ouvert ou mode d'arret	Tourner le noyau de bobine de L2 de X32-1040(B/5)	4.23MHz	(a)
2	VÉRIFICATION DE PUISSANCE DE LASER (Quand PU peut être défectueux)	—	Placer un compteur de puissance optique au-dessus du capteur	Tiroir ouvert. Raccorder la base de Q7 de X32-1040(A/5) à GND.	—	Correct si entre 200μW et 300μW.	(b)
3	VERIFICATION DU COURANT DE FONCTIONNEMENT DU LASER(Quand PU peut etre defectueux)	—	Mesurer la tension entre les deux extrémités de R4 de X32-1040(A/5)	Tiroir ouvert. Raccorder la base de Q7 de X32-1040(A/5) à GND.	—	Acceptable si supérieur de 5 à 6mA au courant marqué sur le capteur.	(c)
4	RÉGLAGE DE SUPPRESSION HF	—	Raccorder un oscilloscope à TP2(HF) de X29-1632(B/6). Raccorder GND de l'oscilloscope a TP1(GND).	Tiroir ouvert ou mode d'arret.	Tourner VR5 de X29-1632(B/6). (RF OFFSET)	Ajuster sur -0.60(V)	(d)
5	MONTAGE DU MODE DE TEST	Placer un disque test de type 3 sur le tiroir et régler l'appareil en condition de chargement.	Court-circuiter entre TP12 et TP13 de X32-1040(A/5).	Placer l'interrupteur POWER OFF à nonveau sur ON.	—	Vérifier que l'affichage est "01 oo 00:00".	(e)
6	RÉGLAGE TANGENTIEL	Placer un disque test de type 3 sur le tiroir et régler l'appareil en condition de chargement.	Raccorder un oscilloscope à TP2(RF) de X29-1632(B/6).	Presser M-READ et le laser est mis au point. (En mode de test)	Vis à prise hexagonale sous le mécanisme	Amplitude maximum	(d)
7	RÉGLAGE APPROXIMATIF DE LA SUPPRESSION DE MISE AU POINT	Placer un disque test de type 3 sur le tiroir et régler l'appareil en condition de chargement.	Raccorder un oscilloscope à TP2(RF) de X29-1632(B/6).	Presser M-READ et le laser est mis au point. (En mode de test)	Tourner VR3 de X29-1632(B/6).	Amplitude maximum	(d)
8	**(Quand PU peut etre defectueux)** RÉGLAGÉ DU RESEAU DE DIFFRACTION (PU)	Placer un disque test de type 3 sur le tiroir et régler l'appareil en condition de chargement.	Raccorder le CH1 d'un oscilloscope à TP2(RF) de X29-1632(B/6) et CH2 a TP3(TE).	Presser M-READ et le laser est mis au point. (En mode de test)	Trou de réglage du capteur—Utiliser l'entraineur de réseau.	Voir la figure 1.	(f)
9	RÉGLAGE APPROXIMATIF DE LA BALANCE T.ERROR.	Placer un disque test de type 3 sur le tiroir et régler l'appareil en condition de chargement.	Raccorder le CH1 d'un oscilloscope à TP2(RF) de X29-1632(B/6) et CH2 a TP3(TE).	Presser M-READ et le laser est mis au point. (En mode de test)	Tourner VR4 de X29-1632(B/6).	Régler de manière à ce que l'amplitude T.ERROR soit symétrique en dessus et au dessous de 0(V). (Photo 5)	(f)
10	RÉGLAGES PRÉCIS DE LA SUPPRESSION TANGENTIELLE ET DE MISE AU POINT.	Placer un disque test de type 3 sur le tiroir et régler l'appareil en condition de chargement.	Raccorder un oscilloscope à TP2(RF) de X29-1632(B/6).	Presser la touche PLAY. (L'appareil commence le reperage.) (Dans le mode de test.)	VR3 de X29-1632(B/6) et vis a prise hexagonale au-dessus du mecanisme.	Tourner alternativement VR3 et la vis à prise hexagonale pour obtenir la forme d'onde optimale.	(d)
11	RÉGLAGE PRÉCIS DE LA BALANCE T.ERROR.	Placer un disque test de type 3 sur le tiroir et régler l'appareil en condition de chargement.	Raccorder le CH1 d'un oscilloscope à TP2(RF) de X29-1632(B/6) et CH2 a TP3(TE).	Presser la touche M-READ (avec asservissement de mise au point seulement). (Dans le mode de test.)	Tourner VR4 de X29-1632(B/6).	Ajuster de maniere à ce que l'amplitude T.ERROR soit symétrique en dessus et au dessous de 0(V). (Photo 5)	(f)
12	RÉGLAGE DU GAIN DE MISE AU POINT	Placer un disque test le plus parfait possible et effectuer le chargement.	Raccorder un gabarit de réglage d'asservissement à CN4 de X29-1632. (f=1.0kHz. V OUT=40mVrms)	Placer l'interrupteur POWER OFF à nouveau sur ON et presser la touche PLAY pour commencer la lecture normale.	Tourner VR2 de X29-1632(B/6).	Régler de manière à ce que le millivoltmetre raccordé au gabarit indique 40mVrms.	(g)

REGLAGE

N°	ITEM	REGLAGE D'ENTREE	REGLAGE DE SORTIE	REGLAGE DE LA LE CTURE	POINT D'ALIGNEMENT	ALIGNEMENT POUR	FIG
13	RÉGLAGE DU GAIN D'ALIGNEMENT	Placer un disque test le plus parfait possible et effectuer le chargement.	Raccorder un gabarit de réglage d'asservissement à CN4 de X29-1632. (f=1.0kHz. V OUT=40mVrms)	Lecture normale	Tourner VR2 de X29-1632(B/6)	Régler de maniere à ce que le millivoltmètre raccordé au gabarit indique 40mVrms.	(g)
14	REGLAGE DAC	Disque test YDS-7 Type 3	Raccorder un millivoltmètre à la borne de sortie.	Lire un signal d' 1kHz, 0dB.	Tourner VR2 de X32-1040(A/5)	Régler pour obtenir un niveau de sortie entre 1,9 et 2,0Vrms.	(h)

Réglage du réseau de diffraction

Régler en mode de test (avec l'asservissement de mise au point seulement)

Remarque : Le mode de test est la condition dans laquelle l'alimentation est fournie après avoir court-circuité entre TP12 (TEST-12) et TP13 (D.GND-13) dans l'appareil de traitement du signal (X32-1040-00) (A/5).

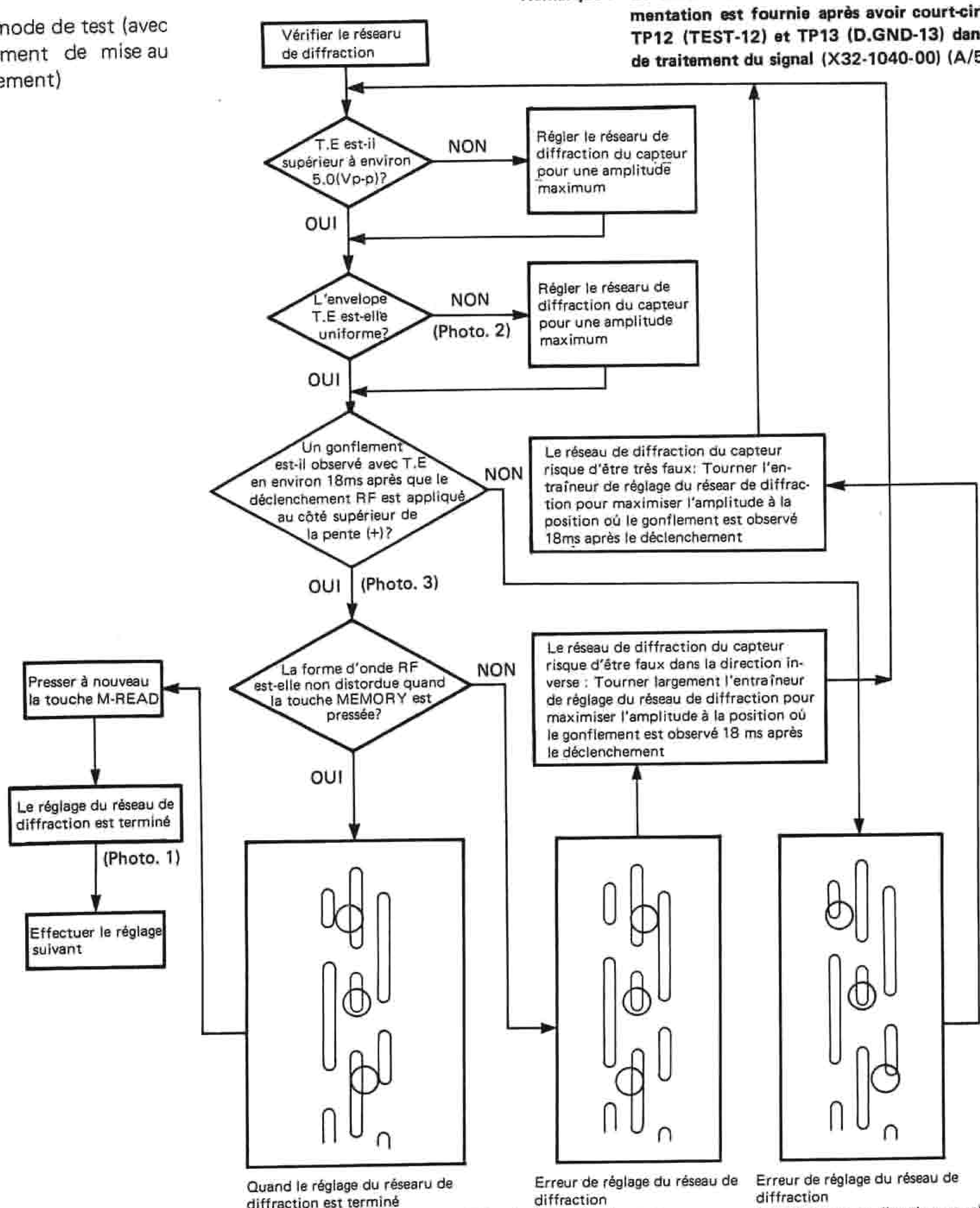


Fig. 1

ABGLEICH

NR.	GEGENSTAND	EINGANGS-EINSTELLUNG	AUSGANGS-EINSTELLUNGE	SPIELER-EINSTELLUNG	ABGLEICH-PUNKT	ABGLEICHUNG	ABB.
1	VCO-EINSTELLUNG	–	Einen Frequenzzähler zwischen CN17 und GND anschlieβen.	Träger geöffnet oder Stop-Betriebsart	Kern der Spule von L2 von X32-1040 (B/5) drehen	4,23MHz	(a)
2	LASERLEISTUNGS PRÜFUNG (wenn PU defekt sein könnte)	–	Einen optischen Leistungsmesser uber den Tonabnehmer setzen	Träger - geöffet. Die Basis von Q7 von X32-1040(A/5) mit GND verbinden.	–	In Ordnung wenn zwischen 200μW und 300μW.	(b)
3	LASERBETRIEBSSTROM PRÜFUNG (wenn PU defekt sein könnte)	–	Die Spannung zwischen den beiden Enden von R4 von X32-1040(A/5) messen.	Träger - geöffet. Die Basis von Q7 von X32-1040(A/5) mit GND verbinden.	–	Akzeptierbar, wenn um 5 bis 6mA groβer als der auf dem Tonabnehmer angegebene Strom.	(c)
4	HF VERSATZ EINSTELLUNG	–	Ein Oszilloskop an TP2(HF) von X29-1632(B/6) anschlieβen. Die Masse des Oszilloskops an TP1(GND) anschlieβen.	Träer geöffnet oder Stop-Betriebsart.	VR5 von X29-1632(B/6) drehen. (HF-VERSATZ)	Auf -0,60(V) einstellen.	(d)
5	ANSCHLÜSSE FÜR TEST BETRIEBSART	Die Test-Disc Typ 3 auf den Träger legen und das Gerät auf den geladenen Zustand einstellen.	TP12 und TP13 von X32-1040(A/5) Kurzschlieβen.	Netzschalter aus und danach einschalten.	–	Überprüfen, daβ auf dem Display "01 oo 00:00" angezeigt wird.	(e)
6	TANGENTIAL EINSTELLUNG	Die Test-Disc Typ 3 auf den Träger legen und das Gerät auf den geladenen Zustand einstellen.	Ein Oszilloskop an TP2(HF) von X29-1632(B/6) anschlieβen.	M-READ drucken, dann wird der Laser fokussiert. (In der Test Betriebsart.)	Innensechskant-schraube unter Mechanismus	Maximale Amplitude	(d)
7	FOKUSVERSATZ GROBEINSTELLUNG	Die Test-Disc Typ 3 auf den Träger legen und das Gerät auf den geladenen Zustand einstellen.	Ein Oszilloskop an TP2(HF) von X29-1632(B/6) anschlieβen.	M-READ drucken, dann wird der Laser fokussiert. (In der Test Betriebsart.)	VR3 von X29-1632(B/6) drehen.	Maximale Amplitude	(d)
8	**(Wenn PU defekt sein könnte)** BEUGUNGS-GITTER EINSTELLUNG (PU)	Die Test-Disc Typ 3 auf den Träger legen und das Gerät auf den geladenen Zustand einstellen.	Kanal 1 eines Oszilloskops an TP2(HF) von X29-1632(B/6) und Kanal 2 an TP3(TE) anschlieβen.	M-READ drucken, dann wird der Laser fokussiert. (In der Test Betriebsart.)	Tonabnehmer Einstellöffnung Den Gitter Schraubenzieher verwenden.	Siehe Abb. 1.	(f)
9	T.ERROR BALANCE GROBEINSTELLUNG	Die Test-Disc Typ 3 auf den Träger legen und das Gerät auf den geladenen Zustand einstellen.	Kanal 1 eines Oszilloskops an TP2(HF) von X29-1632(B/6) und Kanal 2 an TP3(TE) anschlieβen.	M-READ drucken, dann wird der Laser fokussiert. (In der Test Betriebsart.)	VR4 von X29-1632(B/6) drehen.	So einstellen, daβ die T.ERROR Amplitude über und unter 0(V) symmetrisch ist. (Foto 5)	(f)
10	TANGENTIAL UND FOKUSVERSATZ FEINEINSTELLUNGEN	Die Test-Disc Typ 3 auf den Träger legen und das Gerät auf den geladenen Zustand einstellen.	Ein Oszilloskop an TP2(HF) von X29-1632(B/6) anschlieβen.	Die PLAY-Taste drucken.(Das Gerat startet den abtast Betrieb.)(In order Test-Betriebsart.)	VR3 von X29-1632(B/6) und Innensechskant-schraube über Mechanismus	VR3 und die Innensechskant-schraube abwechselnd drehen, um dis optimale Wellenform zu erhalten.	(d)
11	T-ERROR BALANCE FEINEINSTELLUNG	Die Test-Disc Typ 3 auf den Träger legen und das Gerät auf den geladenen Zustand einstellen.	Kanal 1 eines Oszilloskop an TP2(HF) von X29-1632(B/6) und Kanal 2 an TP3(TE) anschlieβen.	Die M-READ-Taste drücken.(nur mit Fokusserbo.) (In der Test Betriebsart.)	VR4 von X29-1632(B/6) drehen.	So einstellen, daβ die T.ERROR-Amplitude über und unter 0(V) symmestrisch ist. (Foto 5)	(d)
12	FOKUSVERSTÄRKUNG EINSTELLUNG	Eine Test-Disc, die so einwandfrei wie moglich sein sollte, auflegen und laden.	Eine Servo Einstellvorrichtung an CN4 von X29-1632 anschlieβen. (f=1,0kHz, V OUT=40mVrms)	Den Netzschalter aus-und wieder einschalten und die PLAY-Taste drucken, um die normale Wiedergabe zu starten.	VR2 von X29-1632(B/6) drehen.	So einstellen, daβ der an die Vorrichtung angeschlossene Millivoltmeter 40mVrms anzeigt.	(g)

ABGLEICH

NR.	GEGENSTAND	EINGANGS-EINSTELLUNG	AUSGANGS-EINSTELLUNGE	SPIELER-EINSTELLUNG	ABGLEICH-PUNKT	ABGLEICHUNG	ABB.
13	SPURHALTEVERSTÄRKUNG EINSTELLUNG	Eine Test-Disc, die so einwandfrei wie moglich sein sollte, suflegen und laden.	Eine Servo Einstellvorrichtung an CN4 von X29-1632(A/4) anschließen. (f=1,0kHz, V OUT=40mVrms)	Normale Wiedergabe	VR1 von X29-1632(B/6) drehen.	So einstellen, daß der an die Vorrichtung angeschlossene Millivoltmeter 40mVrms anzeigt.	(g)
14	DAC EINSTELLUNG	Test-Disc YDS-7 TYPE 3	Einen Millivoltmeter an den Ausgangsanschluß anschließen.	Wiedergabe 1 kHz, 0dB Signal	VR2 X32-1040(A/5) drehen.	So einstellen, dsß ein Ausgangspegel zwischen 1,9 und 2,0Vrms erhalten wird.	(h)

Beugungsgitter-Einstellung

In der Test-Betriebsart einstellen
(nur mit Fokus-Servo)

Hinweis : Die Test-Betriebsart ist der Zustand, in der die Spannungsversorgung nach Kurzschließen von TP12 (TEST-12) und TP13 (D.GND-13) in der Signalverarbeitungseinheit (X32-1040-00) (A/5) eingeschaltet wurde.

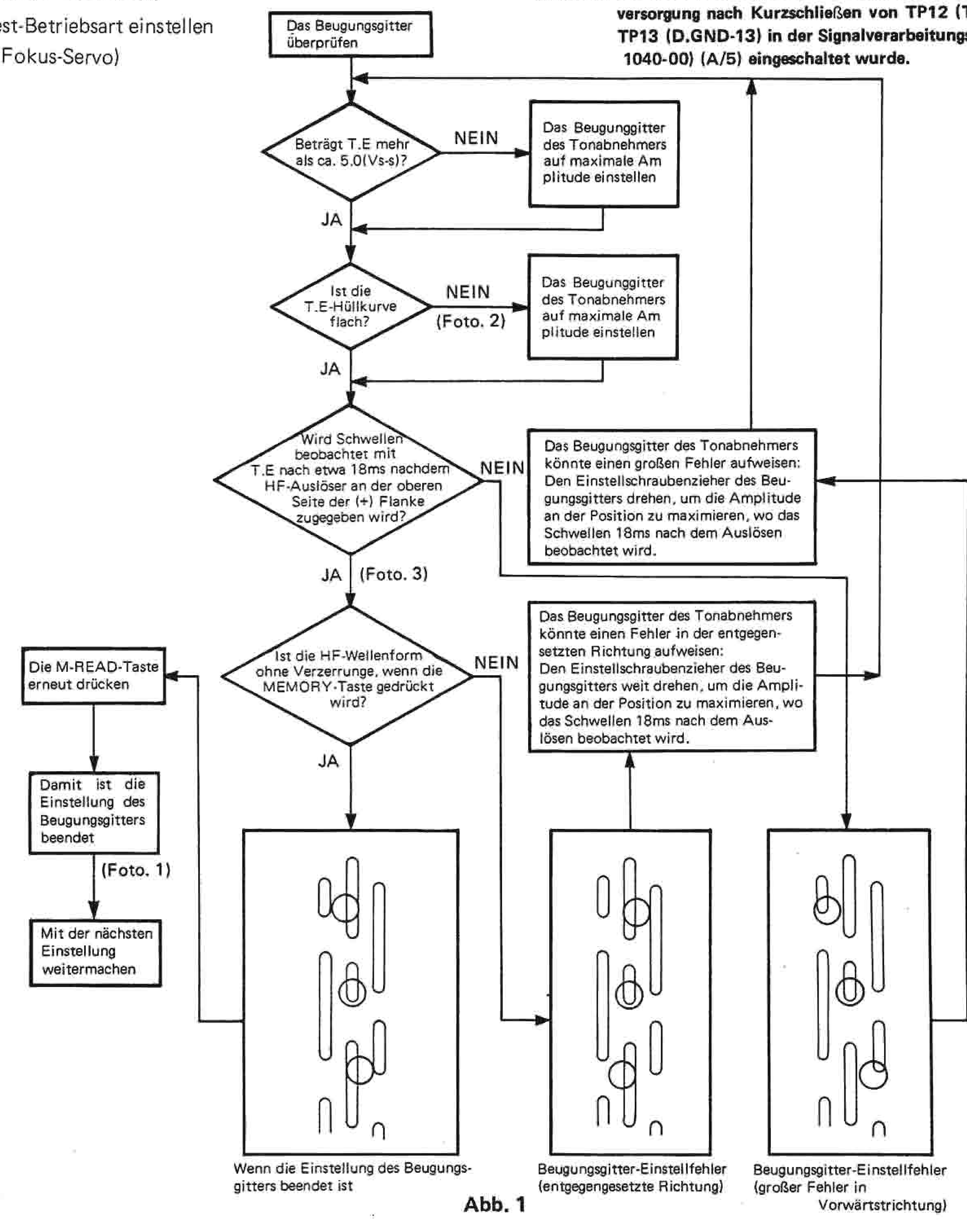
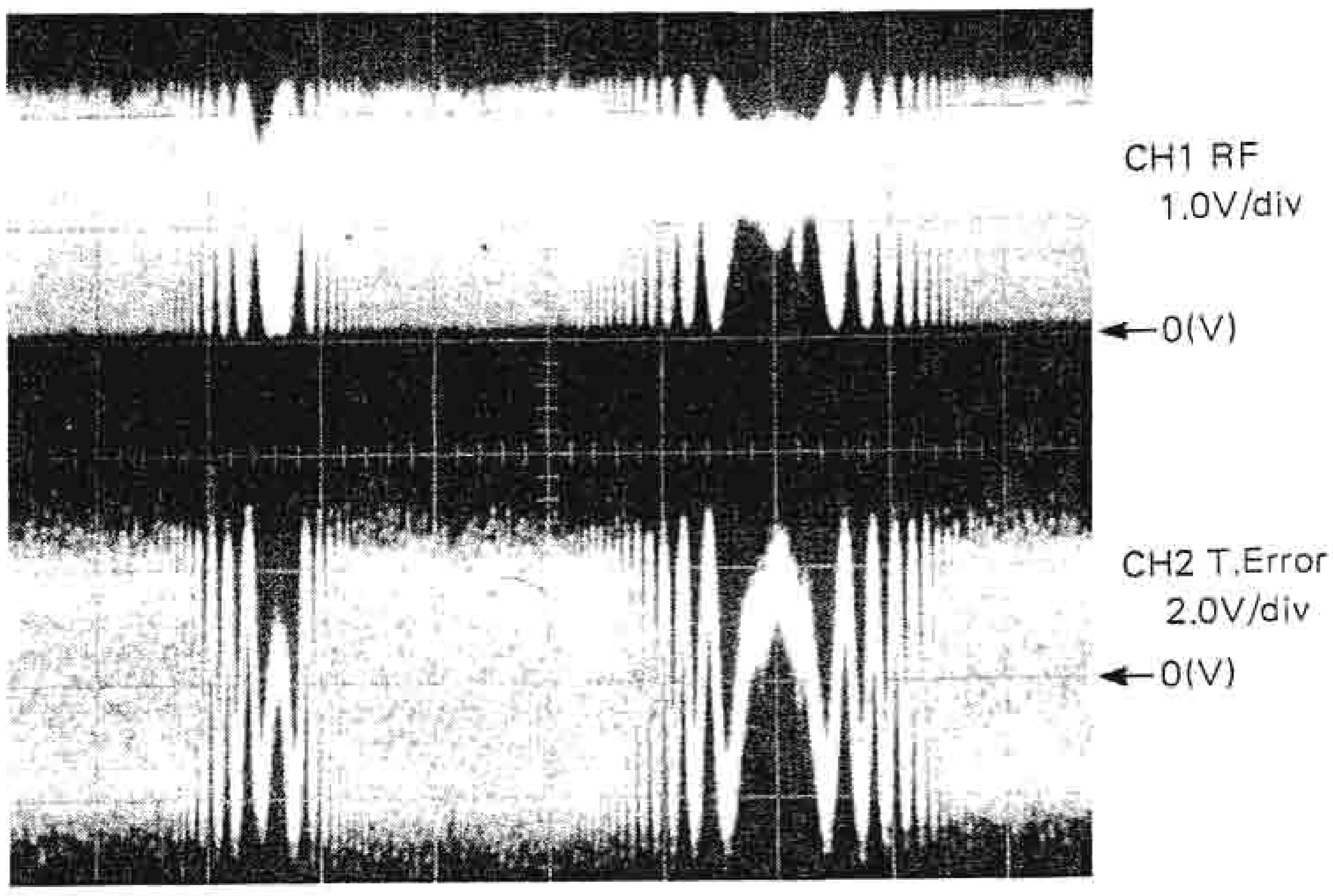


Abb. 1

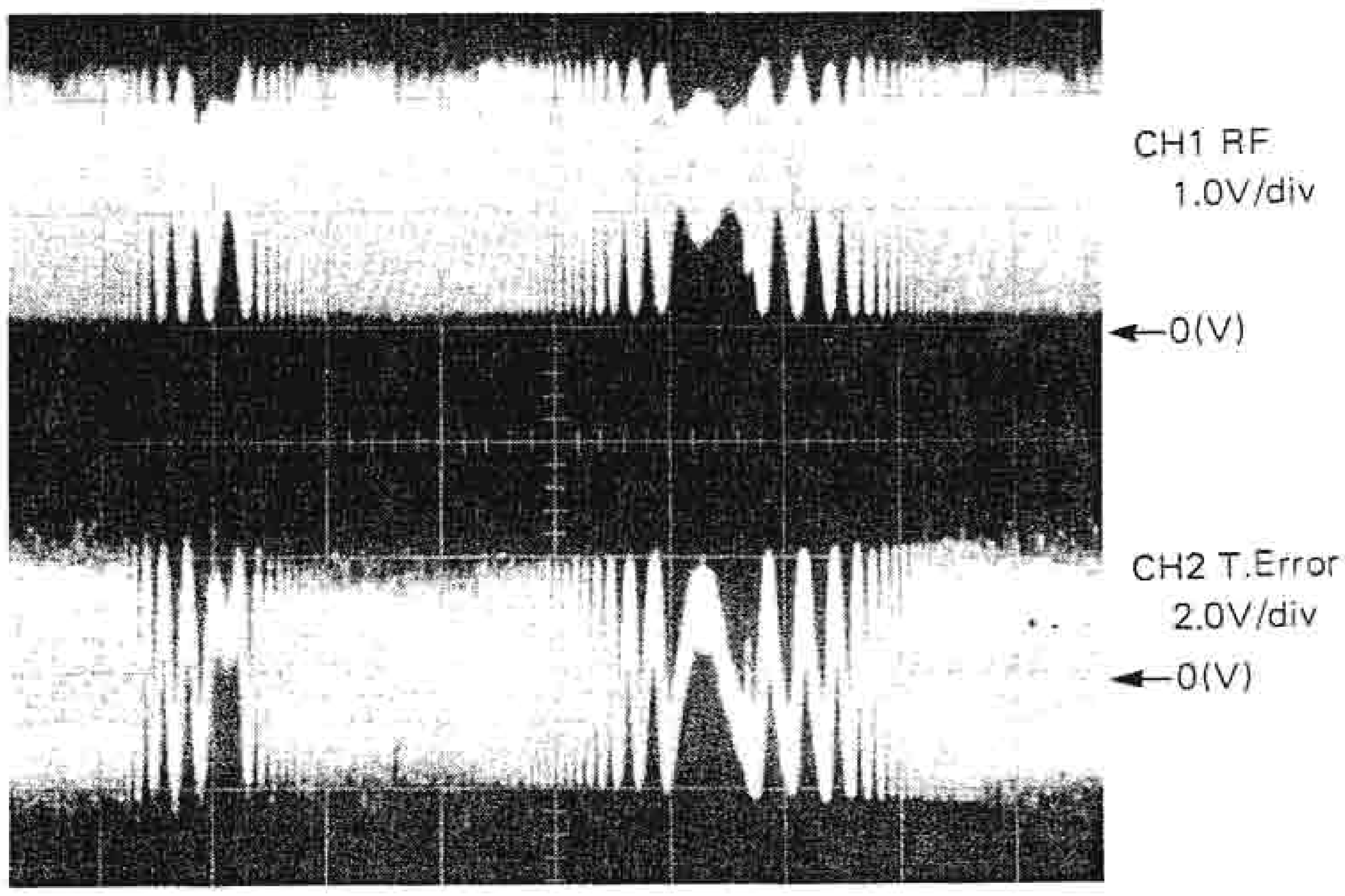
ADJUSTMENT/REGLAGE/ABGLEICH



20msec/div

- RF signal and T.Error signal after completion of diffraction grid adjustment
- Signal RF et signal E.ERROR après avoir terminé le réglage du réseau de diffraction.
- HF-Signal und T.-Fehlersignal nach Beendigung der Beugungsgitter-Einstellung

(Photo. 1)
(Photo. 1)
(Foto. 1)

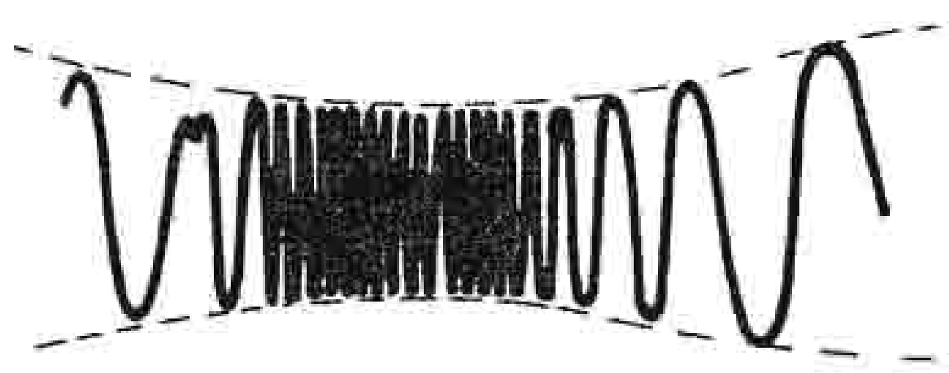


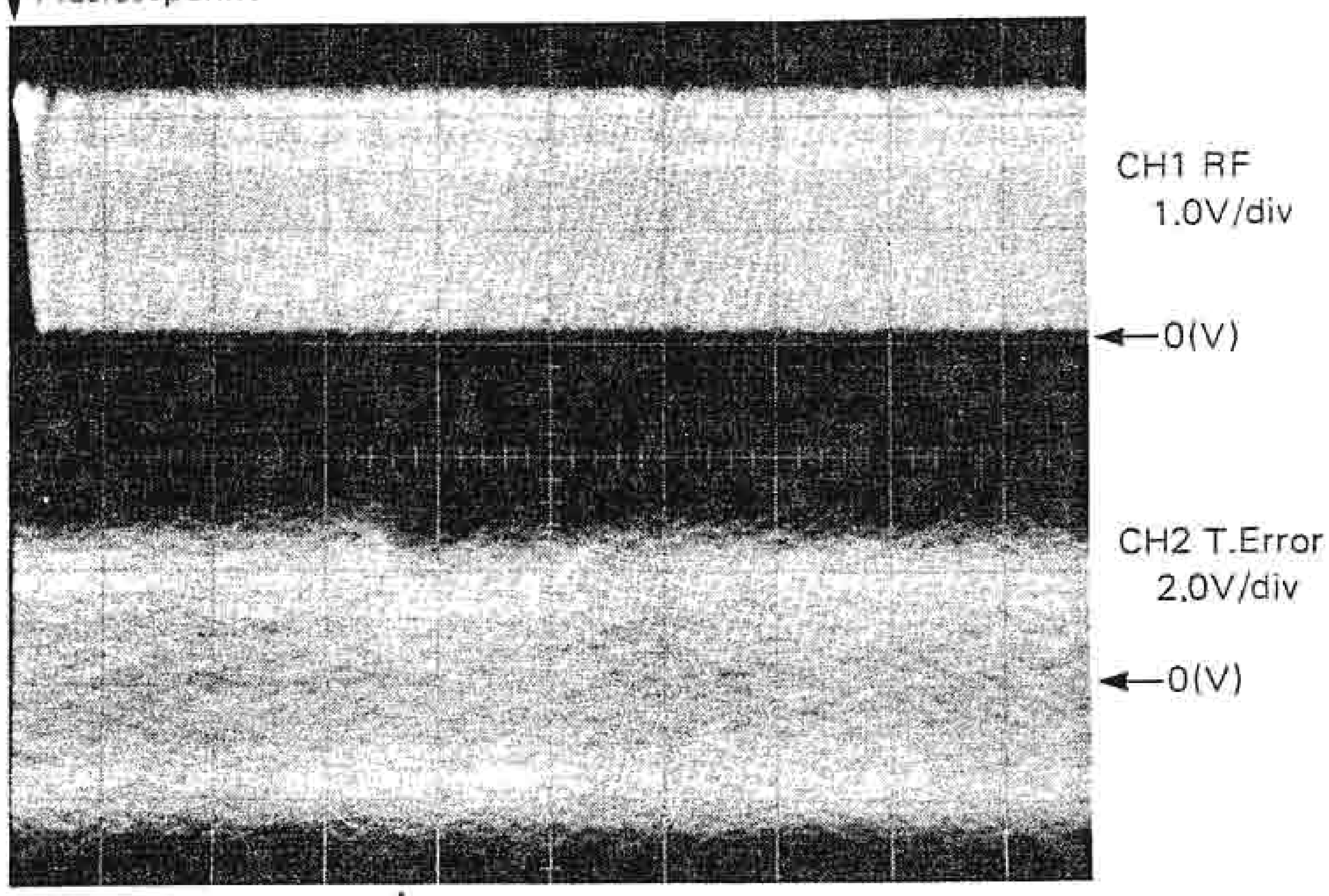
Trigger point
Point de déclenchement
Auslösepunkt

20msec/div

- RF signal and T.Error signal with small diffraction grid error.
- The T.Error level is small, and the envelope is as follows:
- Signal RF et signal T.Error avec une petite erreur de réseau de diffraction
- Le niveau T.ERROR est petit et l'enveloppe est comme suit :
- HF-Signal und T.-Fehlersignal mit kleinem Beugungsgitter-Fehler
- Der T.-Fehlerpegel ist klein und die Hüllkurve ist wie folgt:

(Photo. 2)
(Photo. 2)
(Foto. 2)



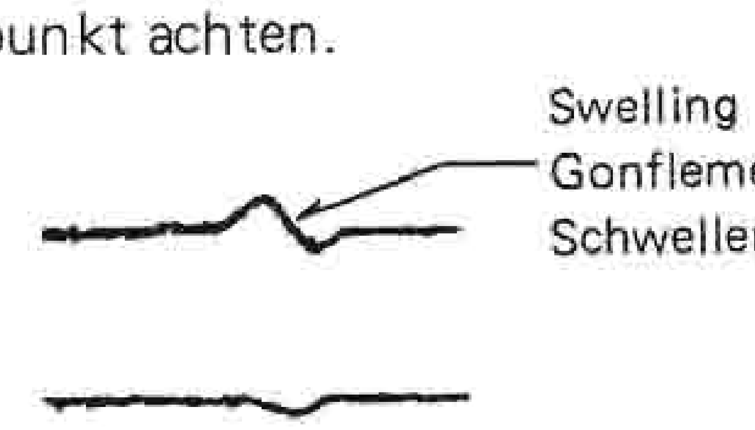


Swelling observed
Gonflement observé
Schwellen beobachtet

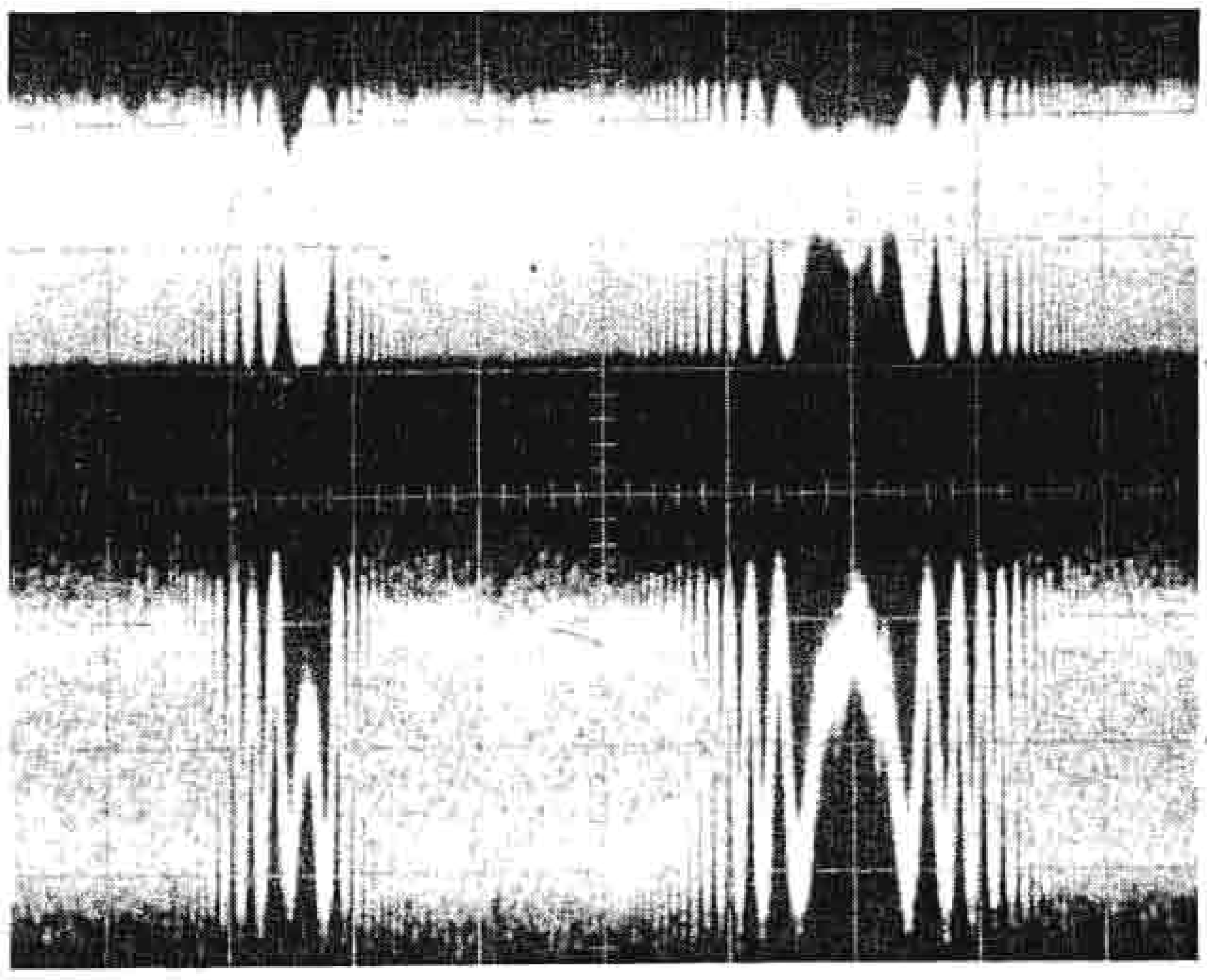
5msec/div

- RF signal and T.Error signal after completion of diffraction grid adjustment.
- Swelling is observed on the T.Error signal of approx. 18ms after the RF trigger point.
- Pay attention to the RF trigger point.
- Signal RF et signal T.ERROR après avoir terminé le réglage du réaeau de diffraction.
- Le gonflement est observé sur le signal T.ERROR d'environ 18ms après le point de déclenchement RF.
- Attention au point de déclenchement RF.
- HF-Signal und T.-Fehlersignal nach Beendigung der Beugungsgitter-Einstellung.
- Am T.-Fehlersignal wird etwa 18ms nach dem HF-Auslösepunkt Schwellen beobachtet.
- Auf den HF-Auslösepunkt achten.

(Photo. 3)
(Photo. 3)
(Foto. 3)



ADJUSTMENT/REGLAGE/ABGLEICH



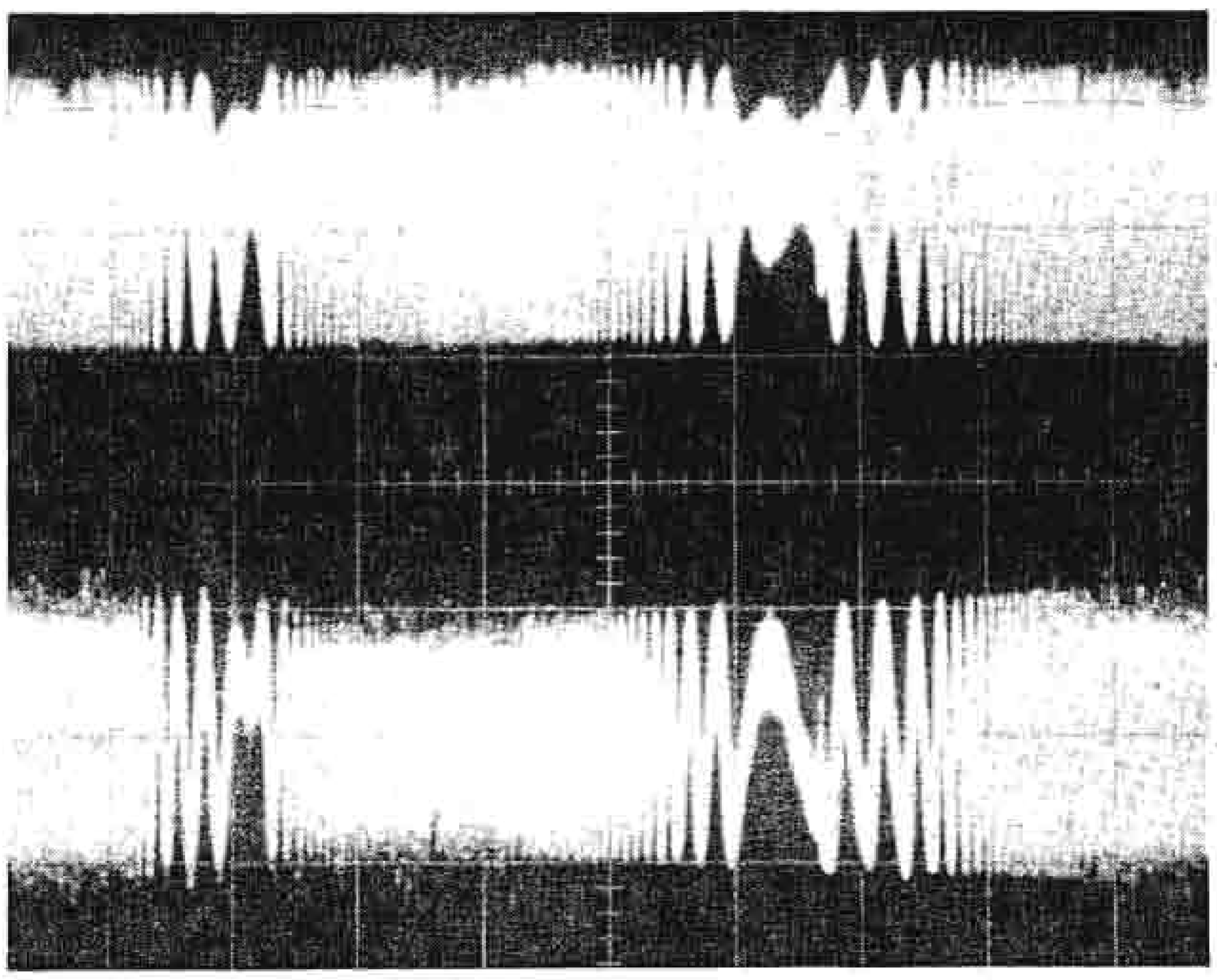
CH1 RF
1.0V/div
←0(V)

CH2 T.Error
2.0V/div
←0(V)

20msec/div

- RF signal and T.Error signal after completion of diffraction grid adjustment
- Signal RF et signal E.ERROR après avoir terminé le réglage du réseau de diffraction.
- HF-Signal und T.-Fehlersignal nach Beendigung der Beugungsgitter-Einstellung

(Photo. 1)
(Photo. 1)
(Foto. 1)



CH1 RF
1.0V/div
←0(V)

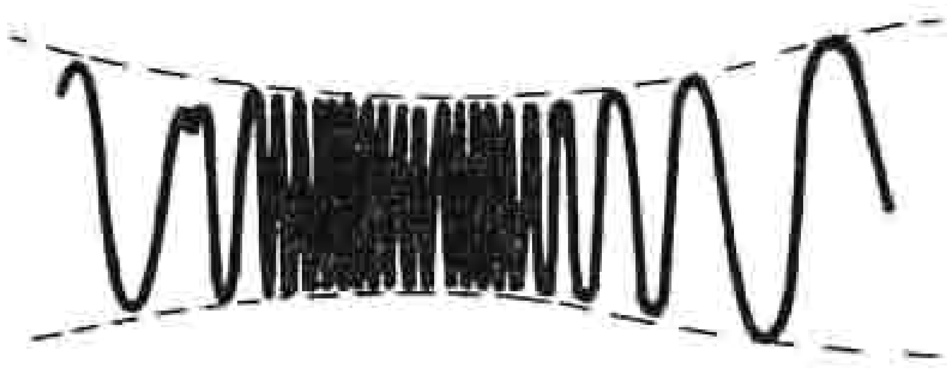
CH2 T.Error
2.0V/div
←0(V)

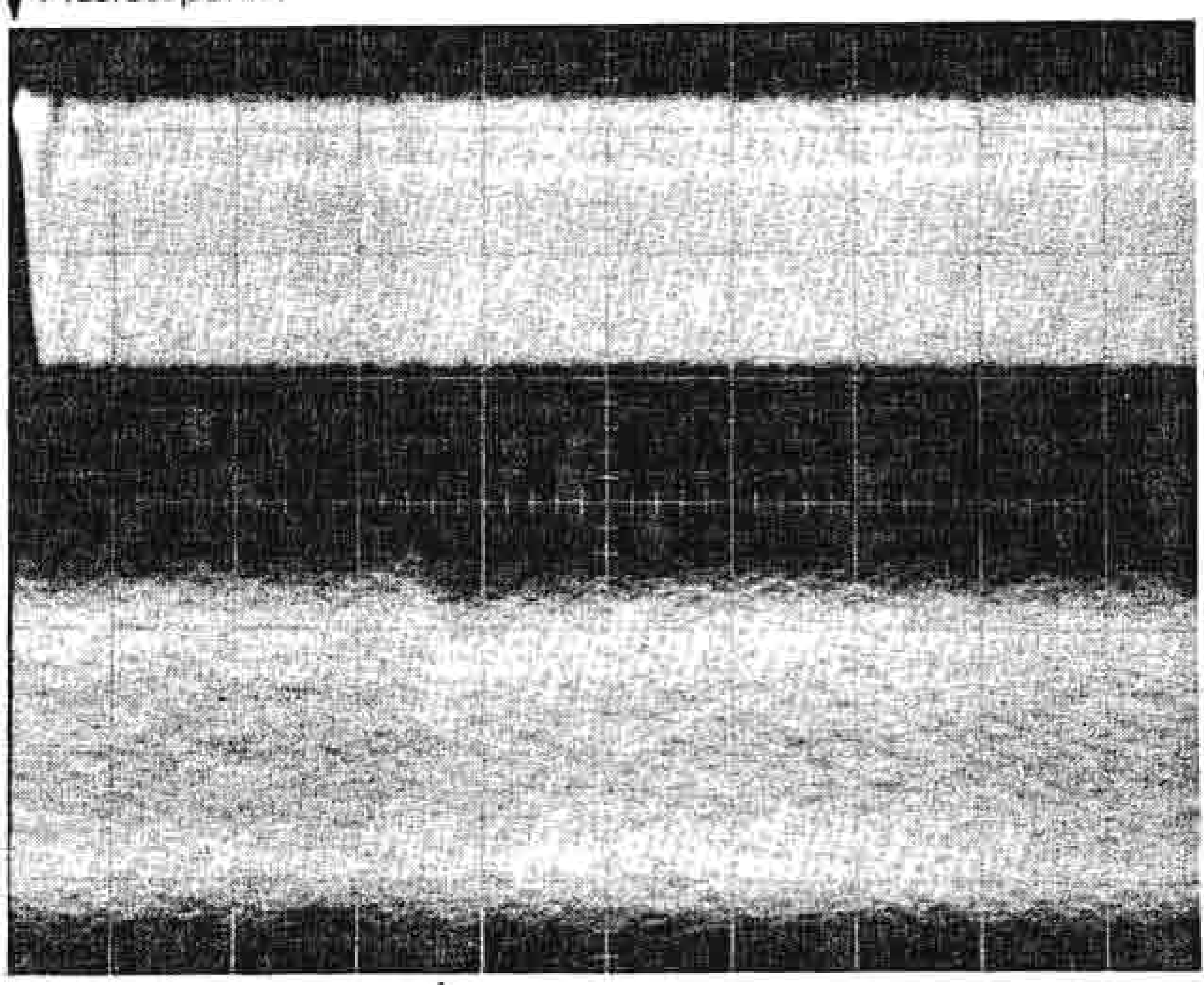
Trigger point
Point de déclenchement
Auslösepunkt

20msec/div

- RF signal and T.Error signal with small diffraction grid error.
- The T.Error level is small, and the envelope is as follows:
- Signal RF et signal T.Error avec une petite erreur de réseau de diffraction
- Le niveau T.ERROR est petit et l'enveloppe est comme suit :
- HF-Signal und T.-Fehlersignal mit kleinem Beugungsgitter-Fehler
- Der T.-Fehlerpegel ist klein und die Hüllkurve ist wie folgt:

(Photo. 2)
(Photo. 2)
(Foto. 2)





CH1 RF
1.0V/div
←0(V)

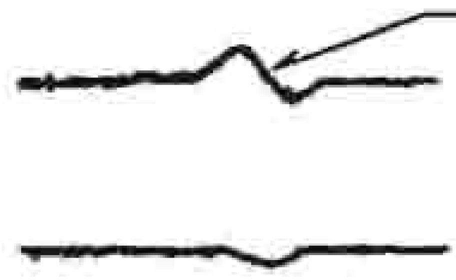
CH2 T.Error
2.0V/div
←0(V)

Swelling observed
Gonflement observé
Schwellen beobachtet

5msec/div

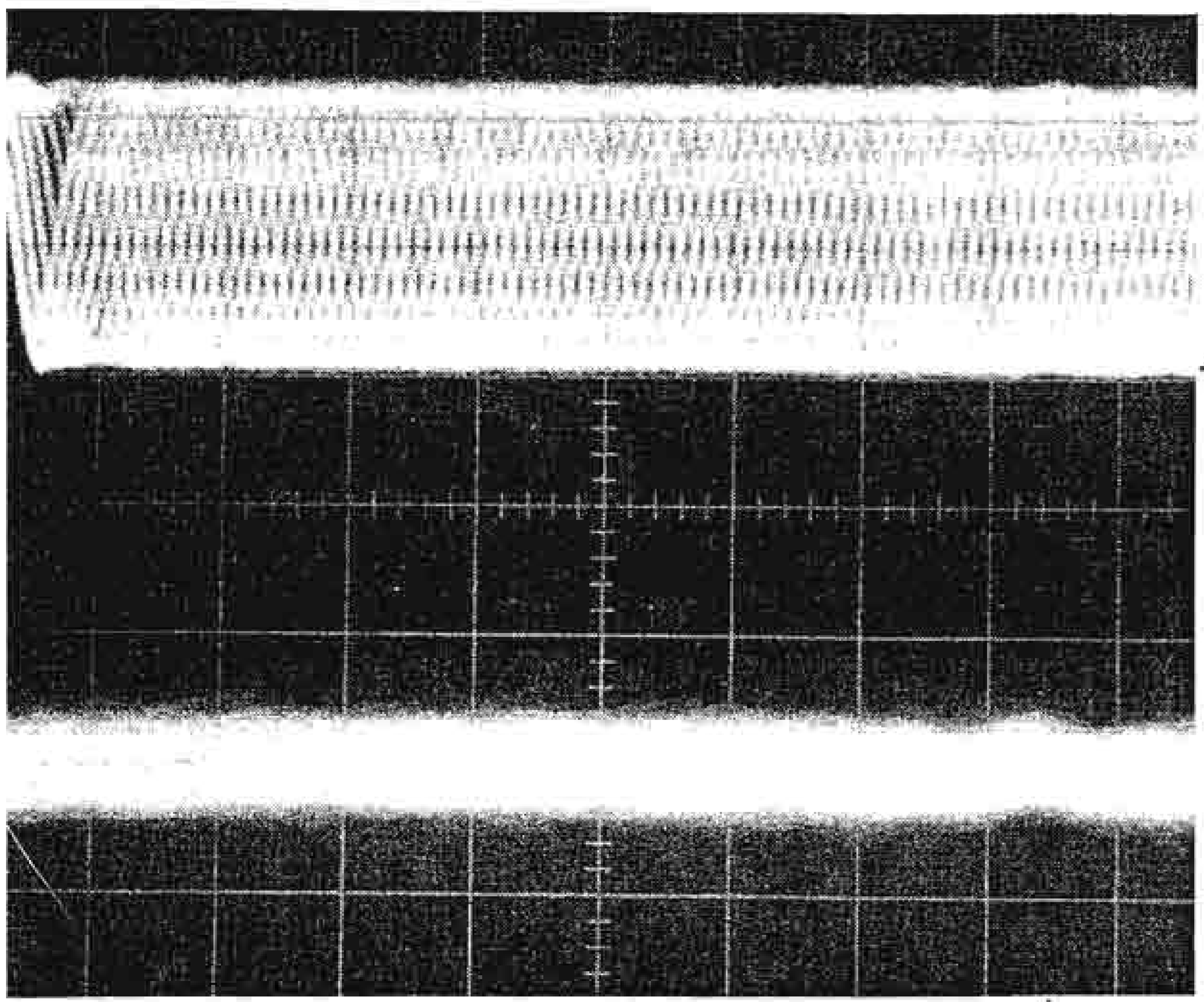
- RF signal and T.Error signal after completion of diffraction grid adjustment.
- Swelling is observed on the T.Error signal of approx. 18ms after the RF trigger point.
- Pay attention to the RF trigger point.
- Signal RF et signal T.ERROR après avoir terminé le réglage du réaeau de diffraction.
- Le gonflement est observé sur le signal T.ERROR d'environ 18ms après le point de déclenchement RF.
- Attention au point de déclenchement RF.
- HF-Signal und T.-Fehlersignal nach Beendigung der Beugungsgitter-Einstellung.
- Am T.-Fehlersignal wird etwa 18ms nach dem HF-Auslösepunkt Schwellen beobachtet.
- Auf den HF-Auslösepunkt achten.

(Photo. 3)
(Photo. 3)
(Foto. 3)



Swelling
Gonflement
Schwellen

ADJUSTMENT/REGLAGE/ABGLEICH



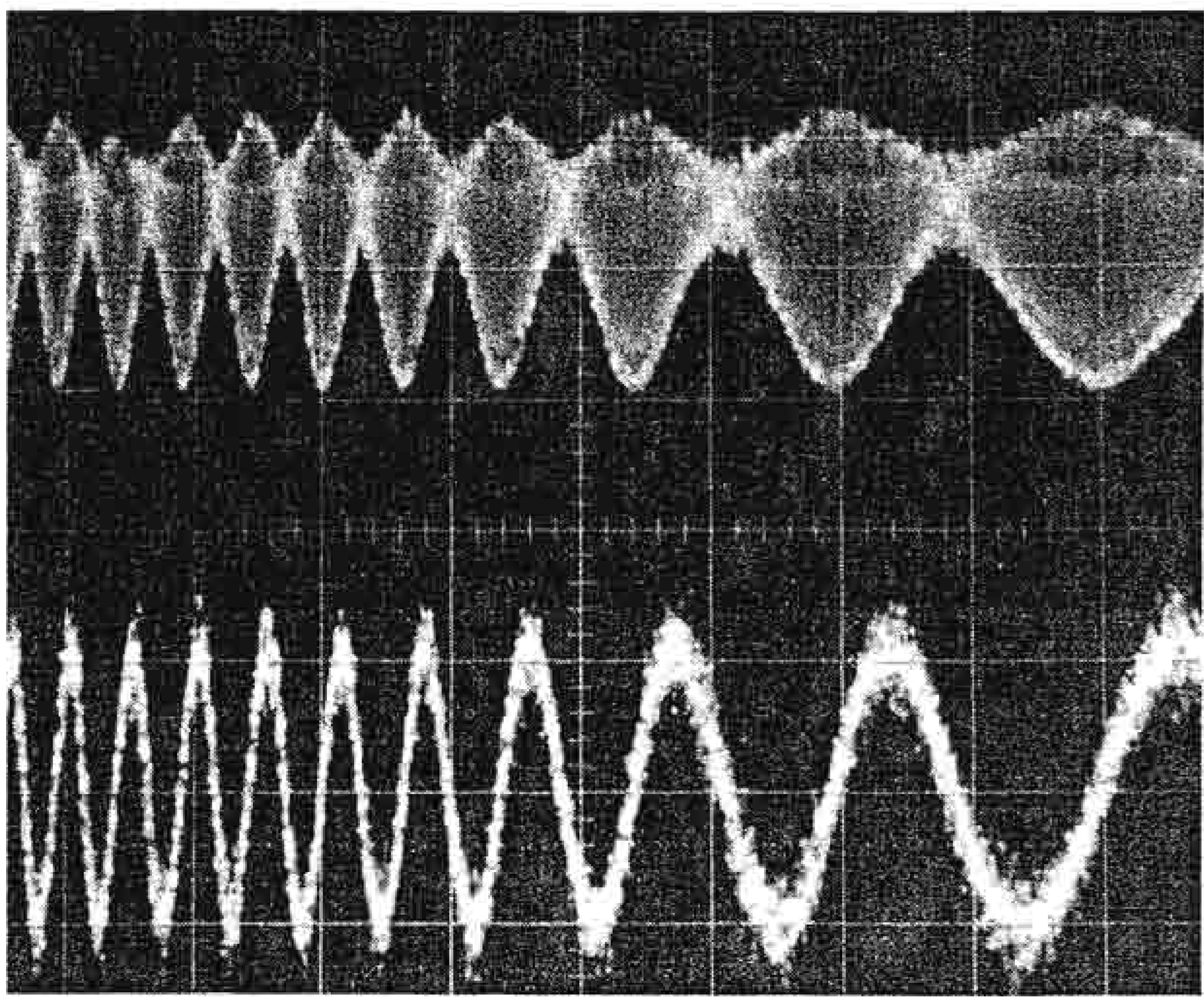
CH1 RF
1.0V/div

←0(V)

CH2
F-SPOT
200mV/div
(AC input)
(AC input)
(NETZ-
EINGANG)

2msec/div

↑Swelling observed
Gonflement observé
Schwellen beobachtet



CH1 RF
1.0V/div

←0(V)

CH2 T.Error
2.0V/div

←0(V)

5msec/div

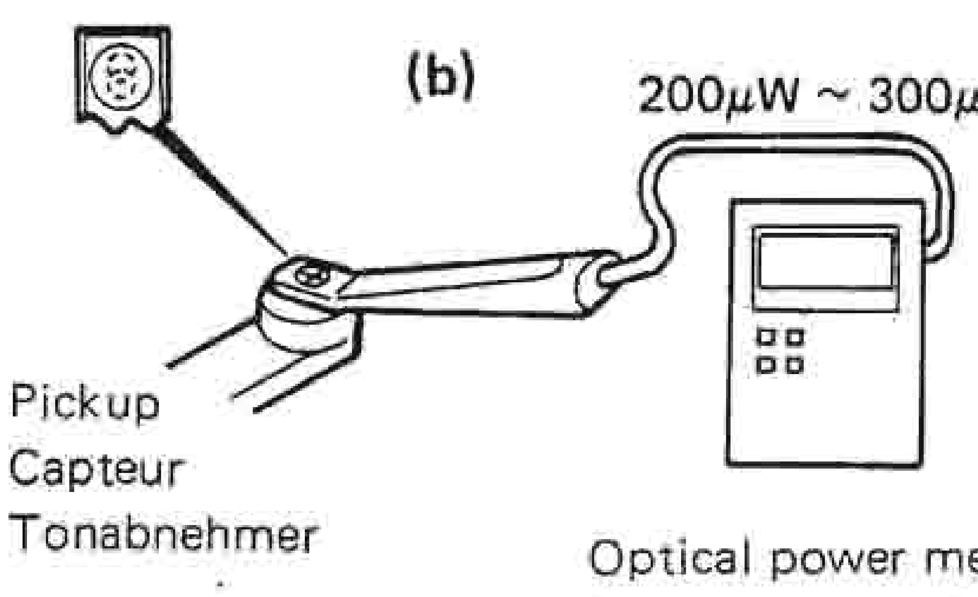
- When the diffraction grid position is correct, tracking servo is applied and RF signal is output.
- In the F spot, swelling is observed approx. 18ms after 18ms.
- Quand la position du réseau de diffraction est correcte, l'asservissement de mise au point est appliquée et le signal RF est mis en sortie.
- Dans le point F, le gonflement est observé environ 18ms après 18ms.
- Wenn die Position des Beugungsgitters korrekt ist, word der Spurhalte-Serve zugegeben und das HF-Signal ausgegeben.
- An der F-Stelle wird nach etwa 18ms Schwellen beobachtet.

(Photo. 4)
(Photo. 4)
(Foto. 4)

- T. Error balance adjustment : Adjust so that the T.Error amplitude is symmetrical above and below 0(V).
- Réglage de la balance T.ERROR : Régler de manière à ce que l'amplitude T.ERROR soit symétrique au dessus et en dessous de 0(V).
- T.-Fehler balance-Einstellung: So einstellen, daß die T.-Fehleramplitude über und unter 0(V) symmetrisch ist.

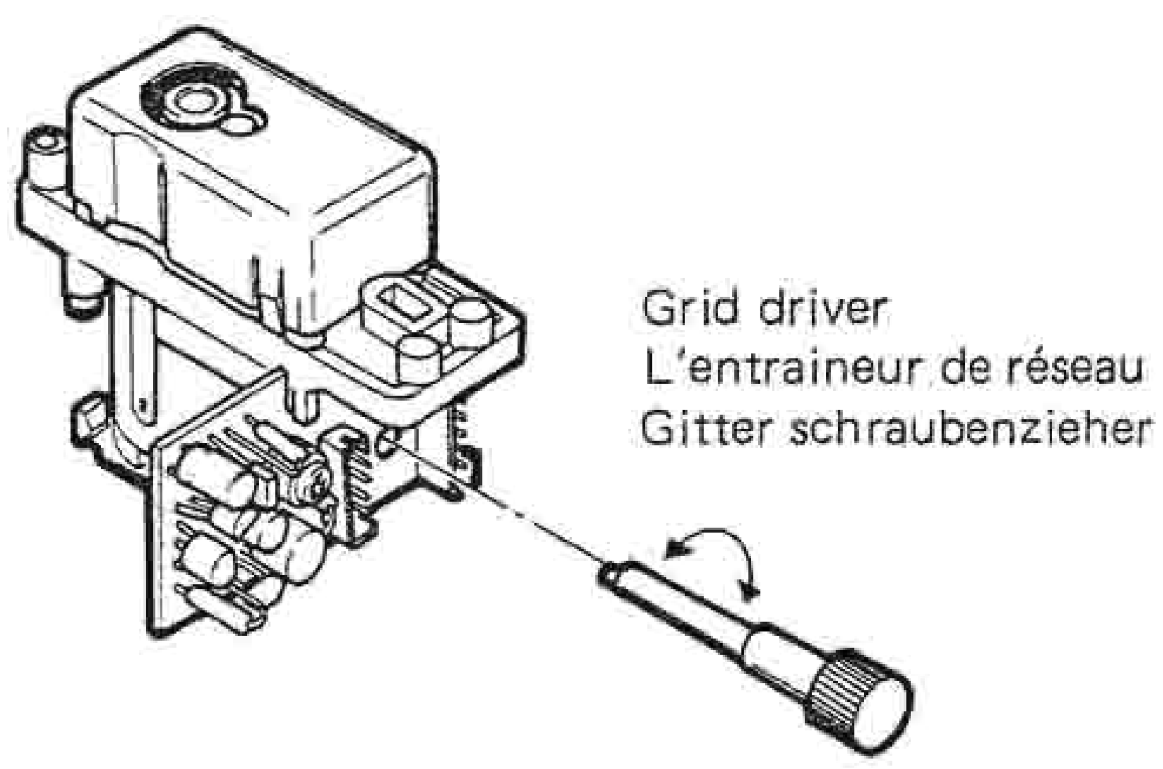
(Photo. 5)
(Photo. 5)
(Foto. 5)

(b)



Optical power meter (b)
Compteur de puissance optique (b)
Optischer Leistungsmesser (b)

(f)



Diffraction grid adjustment (PU)
Réglage du réseau de diffraction (PU)
Beugungsgitter einstellung (PU)

PC BOARD

X29-1632-71

	B	C	E
Q1	–	4.9V	4.2V
Q2	–	4.9V	–
Q5	–	4.9V	–

IC1

7,12	0V
13	–4.9V
21,23,24	4.9V

IC2

2	2.5V
3,4,5	STOP : 2.4V
7	0V
14	4.9V

IC3

1	2.5V
2	–
3	1.6V
4	0V
5	11.4V
6	–
7	–
8	4.8V

X32-1040-00

	B	C	E
Q1	–	PLAY : –14.1V STOP : –16.3V	PLAY : –9V
Q12	–	–	12.1V
Q13	–	PLAY : –12.3V STOP : 4.9V	–12.6V

	G	S	D
Q14	7.8V	7.8V	–
Q15	2.8V	2.8V	7.8V
Q16	–	–	2.8V
Q17,Q18	–	STOP : –3.8V	STOP : 2.2V

	OUT	IN	G
IC1	–5.0V	–12.6V	0V
IC2	4.9V	12.1V	
IC3	18.1V	11.9V	
IC4	–12.1V	–17.1V	
IC5	4.9V	11.9V	
IC6	–5.0V	–12.1V	
IC35	4.9V	4.9V	

IC7

7	4.9V
15	4.9V
17	–5.0V
21	–5.0V
30	0V

IC8

5	–12.6V
10	12.1V

IC10

8	0V
16	4.9V

IC12

29	0V
32	0V
58	–5.0V
64	4.9V

IC13

10	0V
13	4.9V
14	4.9V

IC16

1	Standard clock (2.5V–0.8V Peak, about 0.6V)
3,9,10	0V
24	4.9V

IC17

1,2	–5.0V
4,5,6	4.9V
14	–5.0V
15	STOP : –3.8V
18	STOP : –3.8V
20	–5V
21,22	0V
24	1.4V
28	0V

IC18

1	STOP : 2.2V
3	0V
4	–12.1V
5	0V
6	STOP : –3.8V
7	STOP : 2.2V
8	11.9V

IC19,IC20

6,7,8	–5.0V
10,11,16	4.9V
12,13,14,15	0V

IC21~IC27

4	–11.9V
8	12.1V

IC28

1	STOP : –0.31V
2	STOP : –0.9V
3	–
4	–12.1V
5	STOP : –0.31V
6	STOP : –0.39V
7	STOP : –3.9V
8	11.9V

IC29

1	STOP : –3.9V
2	STOP : –0.39V
3	STOP : –0.39V
4	–12.1V
5	–
6	STOP : –0.9V
7	STOP : –0.39V
8	11.9V

IC30

5	–12.6V
7	2.5V
10	12.1V

IC31

2	PLAY : 2.6V STOP : 0.6V
4	–12.6V
5	2.5V
6	2.5V
7	PLAY : About 0.6V
8	12.1V

IC32

10	0V
12	0V
16	4.9V
33	4.9V
52	0V
58	0V
59	0V
73	4.9V

IC33

12	0V
24	4.9V

Refer to the schematic diagram for the values of resistors and capacitors.

CAUTION: For continue safety, replace safety critical components only with manu cturer's recommended parts (refer to parts list). ⚠ Indicat safety critical components. To reduce the risk of electric hock, leakage-current or resistance measurements shall be ca ied out (exposed parts are acceptably insulated from the su ply circuit) before the appliance is returned to the customer

DP−2000 (K)

- DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

DP-2000

KENWOOD

PARTS LIST

* New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Desti-nation 仕向	Re-marks 備考
				DP-2000		
201	1C	*	A52-0087-03	TOP PLATE ASSY		
202	2D	*	A20-4591-03	PANEL ASSY	UMUEXE	
202	2D	*	A20-4592-03	PANEL ASSY	T	
203	1C	*	A29-0057-03	PANEL ASSY (TRAY)		
204	1C		A70-0129-05	REMOTE CONTROLLER ASSY	UMUEXE	
204	1C		A70-0130-05	REMOTE CONTROLLER ASSY	T	
206	1C	*	A50-0137-03	SIDE PLATE ASSY(L)		
207	1C	*	A50-0138-03	SIDE PLATE ASSY(R)		
208	1C		B07-1415-02	ESCUTCHEON (TRAY)		
209	2D	*	B11-0124-04	SMOKED FILTER		
-			B46-0094-03	WARRANTY CARD	UUE	
-			B46-0095-03	WARRANTY CARD	UUE	
-			B46-0096-13	WARRANTY CARD	X	
-			B46-0122-13	WARRANTY CARD	E	
-			B46-0123-03	WARRANTY CARD	T	
-		*	B50-5886-00	INSTRUCTION MANUAL(ENGLISH)	UMUEXE	
-		*	B50-5887-00	INSTRUCTION MANUAL(FLENCH)	MXE	
-		*	B50-5888-00	INSTRUCTION MANUAL(SPANISH)	M	
-		*	B50-5889-00	INSTRUCTION MANUAL(ENGLISH)	T	
-		*	B50-5890-00	INSTRUCTION MANUAL(G,D,I)	E	
-			B58-0223-04	CAUTION CARD (PRE-SET 120V)	U	
-			B58-0326-04	CAUTION CARD		
-			B58-0327-04	CAUTION CARD		
-			B58-0513-04	CAUTION CARD (PRESET220-240)	UE	
-			B59-0092-00	SERVICE DIRECTORY	UUE	
D1	1D		B30-0431-05	LED(LN21CPH) DISC INDICATOR		
⚠ C1			C91-0023-05	CERAMIC 0.01UF AC250V	UMUE	
⚠ C1			C91-0647-05	CERAMIC 0.01UF P	XTE	
214	1C		E30-0505-05	AUDIO CORD		
⚠ 215	1E		E30-0459-05	AC POWER CORD	E	
⚠ 215	1E		E30-0812-05	AC POWER CORD	UMUE	
⚠ 215	1E		E30-1341-05	AC POWER CORD	X	
⚠ 215	1E		E30-1416-05	AC POWER CORD	T	
-		*	H01-5661-04	ITEM CARTON CASE	UMUEXE	
-		*	H01-5662-04	ITEM CARTON CASE	T	
-		*	H10-1854-02	POLYSTYRENE FOAMED FIXTURE		
-		*	H10-1855-12	POLYSTYRENE FOAMED FIXTURE		
-			H20-0417-04	PROTECTION COVER(460X370X360)	M	
-			H25-0224-04	PROTECTION BAG (800X400)	UUEXTE	
-			H25-0232-04	PROTECTION BAG (235X350)		
223	2D,2E	*	J02-0168-15	INSULATOR ASSY		
224	1E		J42-0083-05	POWER CORD BUSHING		
225	3B		J91-0295-05	PICKUP		
-			J61-0307-05	WIRE BAND		
226	2C	*	K27-1531-04	KNOB (BUTTON) INVERT		
229	1C		K27-1082-04	KNOB (BUTTON) POWER		
230	2C		K29-2201-04	KNOB LEVEL		
231	2D	*	K29-2220-03	KNOB ASSY		
235	1E	*	L01-6814-05	POWER TRANSFORMER (L)		
236	1E	*	L01-6824-05	POWER TRANSFORMER (R)		

E: Scandinavia & Europe H:Audio Club K: USA P: Canada W:Europe
T: England U: PX(Far East, Hawaii)
UE : AAFES(Europe) X: Australia M: Other Areas

⚠ indicates safety critical components.

PARTS LIST

∗ New Parts

Parts without **Parts No.** are not supplied.

Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.

Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Desti-nation 仕向	Re-marks 備考
E	1D		N09-1306-05	TAPPING SCREW (Ø3X6)		
J	1D,1E		N09-1561-05	TAPTITE SCREW (Ø3X6)		
N	1C	∗	N09-1582-05	HEXAGON SOCKET HEAD BOLT(M4X10		
U	1D,2D	∗	N09-1627-05	TAPTITE SCREW (M3X8)		
Z	1D		N29-0035-05	PUSH RIVET (3.5X5.5)		
S1	1D		S40-1066-05	PUSH SWITCH (POWER TYPE)		
S2	1D		S31-2083-05	SLIDE SWITCH (POWER TYPE)		
238	1D		W09-0022-05	BATTERY		
CONTROL UNIT (X29-1632-71)						
D1	1C		B30-0431-05	LED(LN21CPH) RENOTE INDICATOR		
C1			CC45FSL1H100D	CERAMIC 10PF D		
C2			CE04KW1V100M	ELECTRO 10UF 35WV		
C3 ,4			CC45FSL1H150J	CERAMIC 15PF J		
C5			CE04KW1A470M	ELECTRO 47UF 10WV		
C6			C91-0769-05	CERAMIC 0.01UF M		
C7			CK45FF1H103Z	CERAMIC 0.010UF Z		
C8			CE04KW1H2R2M	ELECTRO 2.2UF 50WV		
C9 ,10			CK45FF1H103Z	CERAMIC 0.010UF Z		
C11			CF92FV1H333J	MF 0.033UF J		
C12			C90-1331-05	ALMINIUM ELECTROLYTIC C.		
C13			CK45FB1H471K	CERAMIC 470PF K		
C14			CF92FV1H472J	MF 4700PF J		
C15			CC45FSL1H470J	CERAMIC 47PF J		
C16			CC45FSL1H151J	CERAMIC 150PF J		
C17 ,18			CE04KW1A470M	ELECTRO 47UF 10WV		
C19			CK45FF1H103Z	CERAMIC 0.010UF Z		
C20			C90-1332-05	ELECTRO 10UF 25WV		
C21			CK45FB1H102K	CERAMIC 1000PF K		
C22			C90-1332-05	ELECTRO 10UF 25WV		
C23			CK45FB1H102K	CERAMIC 1000PF K		
⚠ C25 ,26			C91-0647-05	CERAMIC 0.01UF P		
C30		∗	CE04JW0J470M	ELECTRO 47UF 6.3WV		
C31			C91-0751-05	CERAMIC 330PF K		
C32		∗	CE04JW1E3R3M	ELECTRO 3.3UF 25WV		
C33			CE04JW1H010M	ELECTRO 1.0UF 50WV		
C34			CE04DW1HR47M	ELECTRO 0.47UF 50WV		
L1			L79-0702-05	LINE FILTER		
VR1 ,2			R12-3100-05	TRIMMING POT(10K)F.GAIN,T.GAIN		
VR3			R12-3103-05	TRIMMING POT.(47K)FOCUS OFFSET		
VR4		∗	R12-5048-05	TRIMMING POT.(100K)T.ERROR BAL		
VR5			R12-3103-05	TRIMMING POT.(47K)RF OFFSET		
S1 -26	1C,2E		S40-1064-05	PUSH SWITCH		
D2	2D	∗	PH302C	PHOTO DIODE		
FL1	1C	∗	CP2162GR	FLUORESCENT INDICATOR TUBE		
IC1			CX-20109	IC(RF AMP FOR 3-BEAM PICK-UP)		
IC2			TC40H004P	IC(INV BUFFER/CONVERTER X6)		
IC3		∗	CX20106A	IC(REMOTE CONTROLLER PREAMP)		
Q1			2SC1685(R,S)	TRANSISTOR		
Q1			2SC1815(Y,GR)	TRANSISTOR		
Q1			2SC2320(E,F)	TRANSISTOR		
Q1			2SC945(A)(Q,P)	TRANSISTOR		

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Q2 ,3			2SD1302(S)	TRANSISTOR		
Q4 ,5			2SC1685(R,S)	TRANSISTOR		
Q4 ,5			2SC1815(Y,GR)	TRANSISTOR		
Q4 ,5			2SC2320(E,F)	TRANSISTOR		
Q4 ,5			2SC945(A)(Q,P)	TRANSISTOR		
PROCESSOR UNIT (X32-1040-00)						
D36	1C		B30-0371-05	LED(SLP-540A) INVERT		
C1 ,2			CK45FF1H103Z	CERAMIC 0.010UF Z		
C3 ,4			CE04KW1C332M	ELECTRO 3300UF 16WV		
C5 ,6			CE04KW0J102M	ELECTRO 1000UF 6.3WV		
C7		*	C90-1397-05	ELECTRO 3.3UF 50WV		
C8			CK45FF1H103Z	CERAMIC 0.010UF Z		
C9			CE04KW1V471M	ELECTRO 470UF 35WV		
C10			CK45FF1H223Z	CERAMIC 0.022UF Z		
C11			CE04KW1C470M	ELECTRO 47UF 16WV		
C12			CE04KW1E102M	ELECTRO 1000UF 25WV		
C13 ,14		*	CE04KW1E332M	ELECTRO 3300UF 25WV		
C15 ,16			CE04KW1C472M	ELECTRO 4700UF 16WV		
C17 ,18			CE04KW0J102M	ELECTRO 1000UF 6.3WV		
C19			CE04KW1C330M	ELECTRO 33UF 16WV		
C20			CF92FV1H222J	MF 2200PF J		
C21			C90-1349-05	ALMINIUM ELECTROLYTIC C.		
C22			C91-0769-05	CERAMIC 0.01UF M		
C23			CF92FV1H394J	MF 0.39UF J		
C24			CF92FV1H273J	MF 0.027UF J		
C25			CF92FV1H222J	MF 2200PF J		
C26			CF92FV1H104J	MF 0.10UF J		
C27			CF92FV1H333J	MF 0.033UF J		
C28			C90-1349-05	ALMINIUM ELECTROLYTIC C.		
C29			CF92FV1H563J	MF 0.056UF J		
C30			CF92FV1H222J	MF 2200PF J		
C31			CF92FV1H184J	MF 0.18UF J		
C32			CF92FV1H104J	MF 0.10UF J		
C33			CF92FV1H823J	MF 0.082UF J		
C34			CF92FV1H153J	MF 0.015UF J		
C35			C90-1353-05	ALMINIUM ELECTROLYTIC C.		
C36			CK45FF1H223Z	CERAMIC 0.022UF Z		
C37			C90-1353-05	ALMINIUM ELECTROLYTIC C.		
C38			CC45FSL1H101J	CERAMIC 100PF J		
C39 -41			CK45FF1H223Z	CERAMIC 0.022UF Z		
C42			C91-0757-05	CERAMIC 0.001UF K		
C43		*	CC45FUJ1H330J	CERAMIC 33PF J		
C44		*	CC45FUJ1H050C	CERAMIC 5.0PF C		
C45 ,46			CK45FB1H222K	CERAMIC 2200PF K		
C47		*	CC45FUJ1H221J	CERAMIC 220PF J		
C48			CC45FSL1H101J	CERAMIC 100PF J		
C49			CF92FV1H563J	MF 0.056UF J		
C50			CE04KW1H0R1M	ELECTRO 0.1UF 50WV		
C51			CF92FV1H103J	MF 0.010UF J		
C52			CK45FB1H471K	CERAMIC 470PF K		
C53			CK45FF1H223Z	CERAMIC 0.022UF Z		
C54			CK45FB1H102K	CERAMIC 1000PF K		
C55			CK45FF1H223Z	CERAMIC 0.022UF Z		
C56 ,57			CE04KW1C330M	ELECTRO 33UF 16WV		

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C58			C91-0085-05	CERAMIC	0.022UF	N		
C59			C91-0769-05	CERAMIC	0.01UF	M		
C60			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C61			C91-0757-05	CERAMIC	0.001UF	K		
C62 ,63			CE04KW1C330M	ELECTRO	33UF	16WV		
C64 ,65			C91-0749-05	CERAMIC	220PF	K		
C66			CE04KW1H010M	ELECTRO	1.0UF	50WV		
C67			CK45FF1H223Z	CERAMIC	0.022UF	Z		
C68			CF92FV1H473J	MF	0.047UF	J		
C69			CE04KW1H2R2M	ELECTRO	2.2UF	50WV		
C70			C91-0757-05	CERAMIC	0.001UF	K		
C101			C91-0757-05	CERAMIC	0.001UF	K		
C102-105			CE04KW1H2R2M	ELECTRO	2.2UF	50WV		
C106			CE04KW1A471M	ELECTRO	470UF	10WV		
C107			CE04KW1C331M	ELECTRO	330UF	16WV		
C108			CC45FSL1H050C	CERAMIC	5.0PF	C		
C109			C91-0721-05	CERAMIC	10PF	J		
C110			C91-0757-05	CERAMIC	0.001UF	K		
C111			CC45FSL1H030C	CERAMIC	3.0PF	C		
C112-119			CE04KW1H010M	ELECTRO	1.0UF	50WV		
C120,121			CE04KW1V100M	ELECTRO	10UF	35WV		
C122			CE04DW0J471M	ELECTRO	470UF	6.3WV		
C123,124			CQ09FS1H182JZS	POLYSTY	1800PF	J		
C125,126			CQ09FS1H181JZS	POLYSTY	180PF	J		
C127,128		*	CQ93HP2A332J	MYLAR	3300PF	J		
C129-132			CQ93HP2A122J	MYLAR	1200PF	J		
C133,134			C91-0168-05	POLYSTY	68PF	K		
C135-138		*	CQ93HP2A472J	MYLAR	4700PF	J		
C139,140			C91-0168-05	POLYSTY	68PF	K		
C141-144		*	CQ93HP2A562J	MYLAR	5600PF	J		
C145,146			C91-0175-05	POLYSTY	56PF	K		
C147,148		*	CQ93HP2A332J	MYLAR	3300PF	J		
C149,150			CQ09FS1H101JZS	POLYSTY	100PF	J		
C151,152			C91-0168-05	POLYSTY	68PF	K		
C153,154			C91-0175-05	POLYSTY	56PF	K		
C155,156		*	CQ93HP2A472J	MYLAR	4700PF	J		
C157-160			C90-1332-05	ELECTRO	10UF	25WV		
C161,162			CQ93HP2A102J	MYLAR	1000PF	J		
C163,164			C91-0757-05	CERAMIC	0.001UF	K		
J1	1C		E11-0104-15	PHONE JACK	(3P)			
J2	1E		E06-0806-05	CYLINDRICAL RECEPTACLE				
J3	1E		E13-0226-05	PHONO JACK	(2P) OUTPUT			
247	2C		J21-3326-05	JACK MOUNTING HARDWARE				
L1			L40-1092-14	SMALL FIXED INDUCTOR(1.0UH,M)				
L2			L32-0328-05	OSCILATING COIL				
X1			L78-0202-05	RESONATOR	(400KHZ)			
X2			L78-0212-05	RESONATOR	(6.1447MHZ)			
X3		*	L77-0598-05	CRYSTAL RESONATOR(67.7376MHZ)				
A	1E		N09-0295-05	HEXAGON HEAD BOLT(M3X8,+)				
Z	2C		N29-0035-05	PUSH RIVET	(3.5X5.5)			
CP1			R90-0281-05	MULTI-COMP	10KX6	J 1/6W		
CP2			R90-0290-05	MULTI-COMP	10KX3	J 1/6W		
CP3			R90-0228-05	MULTI-COMP	10KX5	J 1/6W		

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CP4			R90-0233-05	MULTI-COMP 10KX4 J 1/6W		
CP5			R90-0291-05	MULTI-COMP 100KX4 J 1/6W		
CP6			R90-0466-05	COMPOSITE ELEMENTS		
CP7			R90-0233-05	MULTI-COMP 10KX4 J 1/6W		
R1			RS14DB3A222J	FL-PROOF RS 2.2K J 1W		
R27			RS14DB3D180J	FL-PROOF RS 18 J 2W		
R34			RS14DB3D220J	FL-PROOF RS 22 J 2W		
R59			RS14DB3D180J	FL-PROOF RS 18 J 2W		
R68		*	RN14BK2C6191F	RN 6.19K F 1/6W		
R69			RN14BK2C6811F	RN 6.81K F 1/6W		
R70		*	RS14DB3D2R2J	FL-PROOF RS 2.2 J 2W		
R205			RN14BK2C6811F	RN 6.81K F 1/6W		
R206			RN14BK2C6811F	RN 6.81K F 1/6W		
R207,208			RN14BK2C4641F	RN 4.64K F 1/6W		
R209,210			RN14BK2C1621F	RN 1.62K F 1/6W		
R211,212			RN14BK2C1003F	RN 100K F 1/6W		
R213,214		*	RN14BK2C4991F	RN 4.99K F 1/6W		
R215,216			RN14BK2C1001F	RN 1.00K F 1/6W		
R217,218			RN14BK2C3831F	RN 3.83K F 1/6W		
R219,220		*	RN14BK2C3481F	RN 3.48K F 1/6W		
R221,222			RN14BK2C1621F	RN 1.62K F 1/6W		
R223,224			RN14BK2C1001F	RN 1.00K F 1/6W		
R225,226		*	RN14BK2C9090F	RN 909.0 F 1/6W		
R227,228			RN14BK2C3161F	RN 3.16K F 1/6W		
R229,230		*	RN14BK2C9090F	RN 909.0 F 1/6W		
R231,232			RN14BK2C1001F	RN 1.00K F 1/6W		
R233,234			RN14BK2C5620F	RN 562.0 F 1/6W		
R235,236			RN14BK2C1003F	RN 100K F 1/6W		
R237,238			RN14BK2C1621F	RN 1.62K F 1/6W		
R239,240			RN14BK2C3161F	RN 3.16K F 1/6W		
R241,242		*	RN14BK2C9090F	RN 909.0 F 1/6W		
R243,244			RN14BK2C1002F	RN 10.0K F 1/6W		
R247,248		*	RN14BK2C9092F	RN 90.9K F 1/6W		
R249,250			RN14BK2C1002F	RN 10.0K F 1/6W		
R251,252			RN14BK2C1003F	RN 100K F 1/6W		
R253			RN14BK2C2150F	RN 215.0 F 1/6W		
R254		*	RN14BK2C2150F	RN 215.0 F 1/6W		
R265			RN14BK2C1000F	RN 100.0 F 1/6W		
R266		*	RN14BK2C1000F	RN 100.0 F 1/6W		
VR1			R12-3096-05	TRIMMING POT. (10K) ODA		
VR2	1C		R10-4022-05	POTENTIOMETER(50K) LEVEL		
K1 ,2			S51-2074-05	MAGNETIC RELAY		
S1	1C		S40-2152-05	PUSH SWITCH (REVERSE,NORMAL)		
D1 ,2			1B4B41	DIODE		
D1 ,2			1D4B41	DIODE		
D1 ,2			1G4B41	DIODE		
D3			DSM1A1	DIODE		
D4			RD8.2E(B2)	ZENER DIODE		
D5			DSM1A1	DIODE		
D6			RD11E(B2)	ZENER DIODE		
D7			RD3.6F(B)	ZENER DIODE		
D8			1SS133	DIODE		
D8			1SS176	DIODE		

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D9 ,10			RD3.6F(B)	ZENER DIODE		
D11 ,12			1SS133	DIODE		
D11 ,12			1SS176	DIODE		
D13 -15			1S2076A	DIODE		
D17 -20			1SS133	DIODE		
D17 -20			1SS176	DIODE		
D21 -23			1SS133	DIODE		
D21 -23			1SS176	DIODE		
D25			1SV147	VARISTOR		
D26 -29			1SS133	DIODE		
D26 -29			1SS176	DIODE		
D30 ,31		*	RD7.5JS(B)	ZENER DIODE		
D32			1SS133	DIODE		
D32			1SS176	DIODE		
D33			1SS133	DIODE		
D33			1SS176	DIODE		
D34			1SS133	DIODE		
D34			1SS176	DIODE		
D35			1SS133	DIODE		
D35			1SS176	DIODE		
IC1			AN7905F	IC(VOLTAGE REGULATOR/ -5V)		
IC2			AN7805F	IC(VOLTAGE REGULATOR/ +15V)		
IC3		*	AN7812F	IC(VOLTAGE REGULATOR/ +12V)		
IC4			AN7912F	IC(VOLTAGE REGULATOR/ -12V)		
IC5			AN7805F	IC(VOLTAGE REGULATOR/ +15V)		
IC6			AN7905F	IC(VOLTAGE REGULATOR/ -5V)		
IC7			CX20108	IC(CD SERVO)		
IC8			TA7256P	IC(OP AMP X2)		
IC9			LM6416E-504	IC(MICROPROCESSOR)		
IC10		*	TC40H157F	IC(QUAD 2-TO-1 LINE DATA SEL		
IC11			TC40H000P	IC(NAND X4)		
IC12		*	UPD7516HCW-230	IC(MICROPROCESSOR)		
IC13		*	HD44700SA39	IC(DROPOUT CONTROL)		
IC14		*	TC40H002P	IC(16KRAM)		
IC15		*	TC74HC00P	IC(QUAD 2-INPUT NAND GATE)		
IC16		*	CX23034	IC(CD DIGITAL FILTER)		
IC17			CX20152	IC(16-BIT D/A CONVERTER)		
IC18			TL072CP-T	IC(OP AMP X2)		
IC19,20			UPD4053BC	IC(3-INPUT 2CH MPX/DE-MPX)		
IC21			TL072CP-T	IC(OP AMP X2)		
IC22-29			NE5532P	IC(OP AMP X2)		
IC30			TA7256P	IC(OP AMP X2)		
IC31			AN6556	IC(OP AMP X2)		
IC31			NJM4558D	IC(OP AMP X2)		
IC32			CX23035	IC(DIGITAL SIGNAL PROCESSOR)		
IC33			CXK5816M	IC(2K BYTE X8 RAM (CMOS))		
IC33			HM6116FP-4	IC(16K RAM)		
IC33			MB8416-20LPF	IC(16K RAM(CMOS))		
IC33		*	TC5517AF-2	IC(16K RAM)		
IC34			NJM4560D	IC(OP AMP X2)		
IC34			NJM4560D-N	IC(OP AMP X2)		
IC35			PST518B	IC(SYSTEM RESET)		
Q1			2SB941(P)	TRANSISTOR		
Q2			2SA1015(Y,GR)	TRANSISTOR		
Q2			2SA1127NC(R,S)	TRANSISTOR		

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Q2			2SA733(A)(Q,P)	TRANSISTOR		
Q3			2SC1685(R,S)	TRANSISTOR		
Q3			2SC1815(Y,GR)	TRANSISTOR		
Q3			2SC945(A)(Q,P)	TRANSISTOR		
Q4			2SA1286	TRANSISTOR		
Q5		*	2SD1266(P)	TRANSISTOR		
Q6 ,7			2SC2878	TRANSISTOR		
Q8			2SC1685(R,S)	TRANSISTOR		
Q8			2SC1815(Y,GR)	TRANSISTOR		
Q8			2SC945(A)(Q,P)	TRANSISTOR		
Q9			2SA1015(Y,GR)	TRANSISTOR		
Q9			2SA1127NC(R,S)	TRANSISTOR		
Q9			2SA733(A)(Q,P)	TRANSISTOR		
Q10			2SD1302(S)	TRANSISTOR		
Q11			2SC1685(R,S)	TRANSISTOR		
Q11			2SC1815(Y,GR)	TRANSISTOR		
Q11			2SC945(A)(Q,P)	TRANSISTOR		
Q12			2SA1015(Y,GR)	TRANSISTOR		
Q12			2SA1127NC(R,S)	TRANSISTOR		
Q12			2SA733(A)(Q,P)	TRANSISTOR		
Q13			2SK246(Y,GR)	FET		
Q14			2SK363(V)	FET		
Q15		*	2SK363(GR)	FET		
Q16			2SK246(Y)	FET		
Q17 ,18		*	2SK152(3,4)	FET		
Q19			2SD1302(S)	TRANSISTOR		
Q20			2SK246(BL)	FET		
			MECHANISM ASS'Y (X92-1060-01)			
1	3B	*	A10-0844-02	CHASSIS CALKING ASSY		
2	1B	*	A11-0166-03	SUB CHASSIS CALKING ASSY		
3	2B	*	A11-0132-03	SUB CHASSIS (TRAY)		
4	2B	*	A11-0168-03	SUB CHASSIS (MECHANISM)		
8	2B	*	B09-0044-04	CAP		
C1 -3			C91-0085-05	CERAMIC 0.022UF N		
12	1A	*	D10-1266-03	SLIDER (L)		
13	2B	*	D10-1267-03	SLIDER (R)		
14	1A	*	D10-1545-03	SLIDER		
15	2A		D10-1269-08	ARM		
16	2B	*	D10-1270-04	ROD		
17	1B	*	D10-1546-03	ARM		
18	1A	*	D12-0105-15	CAM		
19	3B		D13-0159-08	GEAR		
20	3A		D13-0160-08	GEAR		
21	2A	*	D13-0161-03	GEAR		
22	2A		D13-0162-08	GEAR		
23	2A		D13-0163-08	GEAR		
24	2B	*	D13-0164-04	GEAR		
25	3A,1B	*	D14-0106-04	ROLLER		
26	3A	*	D14-0107-04	ROLLER		
27	3B		D15-0220-08	PULLEY		
28	3B		D16-0104-08	BELT		
29	1B	*	D21-1051-04	SHAFT		
30	1B	*	D21-1052-04	SHAFT		

E: Scandinavia & Europe H:Audio Club K: USA P: Canada W:Europe
T: England U: PX(Far East, Hawaii)
UE : AAFES(Europe) X: Australia M: Other Areas

⚠ indicates safety critical components.

PARTS LIST

⁎ New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Desti-nation 仕向	Re-marks 備考
31	1A	*	D32-0122-04	STOPPER		
32	3B	*	D40-0353-05	DRIVE MECHANISM ASSY(TRAY)		
33	2A	*	D40-0348-05	DRIVE MECHANISM ASSY(P.U)		
37	3A	*	F19-0348-04	BLIND PLATE		
40	2A	*	G01-1710-04	COMPRESSION SPRING		
41	1B,3B		G01-0675-04	TORSION COIL SPRING		
42	1A,1B	*	G01-1523-04	EXTENSION SPRING		
43	2B	*	G01-1524-04	EXTENSION SPRING		
44	2A	*	G01-1525-04	EXTENSION SPRING		
45	2A,2B	*	G13-0182-04	CUSHION		
46	1B	*	G16-0117-04	SHEET (38X38X2)		
47	1A	*	G16-0134-04	SHEET (38X152X1)		
48	2A	*	J31-0254-04	COLLAR		
49	2A,2B	*	J02-0158-05	INSULATOR		
50	2A	*	J21-3841-08	MOUNTING HARDWARE		
51	1A	*	J11-0066-14	CLAMPER		
52	2B	*	J19-2153-04	HOLDER		
53	3A		J21-3507-08	MOUNTING HARDWARE ASSY		
54	2A	*	J21-3713-03	MOUNTING HARDWARE ASSY(RACK)		
55	2A	*	J21-3711-08	MOUNTING HARDWARE		
56	2B	*	J21-3513-04	MOUNTING HARDWARE		
57	2B	*	J21-3672-04	MOUNTING HARDWARE(P.U)		
58	2A	*	J25-4669-03	PRINTED WIRING BOARD(FG)		
59	3B	*	J31-0233-05	COLLAR (Ø4.1X8)		
60	3A	*	J90-0143-03	GUIDE (STOPPER)		
61	1A	*	J90-0157-03	RAIL		
62	3B	*	J25-4660-03	PRINTED WIRING BOARD		
63	1B	*	J99-0029-02	TRAY		
64	2B	*	J99-0030-03	TRAY		
65	2B	*	J99-0031-03	TRAY		
-			J61-0307-05	WIRE BAND		
73	1A	*	N15-1026-45	FLAT WASHER (Ø2.6)		
74	2A		N19-0143-04	FLAT WASHER (Ø3)		
75	2A		N19-0366-04	FLAT WASHER (Ø2.1)		
76	1A	*	N19-0945-04	FLAT WASHER		
77	1A,3A		N19-0891-04	FLAT WASHER		
79	1A,1B		N29-0207-04	RETAINING RING (Ø2.5)		
80	3B		N29-0220-05	RETAINING RING (Ø2.4)		
J	2A,2B		N09-1306-05	TAPPING SCREW (Ø3X6)		
K	2A,2B	*	N09-1379-15	STEPPED SCREW (M2.6X15)		
L	2A,2B	*	N09-1380-05	STEPPED SCREW (M2.6X5)		
M	3B	*	N09-1381-05	STEPPED SCREW (M5X26)		
P	3A		N29-0067-05	PUSH RIVET (3.5X4.5)		
Q		*	N09-1561-05	TAPTITE SCREW (3X6,+)		
S1 ,2	3A,3B	*	S46-1045-05	LEAF SWITCH		
S3	2A	*	S46-1046-05	LEAF SWITCH		
84	3A		T42-0049-25	MOTOR ASSY		
85	2A	*	T42-0078-08	MOTOR ASSY		
86	2A	*	T42-0075-04	MOTOR ASSY		
87	1A	*	T50-1023-04	YOKE		
88	1A	*	T99-0222-05	MAGNET		
PH1	2A		T95-0017-05	OPTO ISOLATOR		

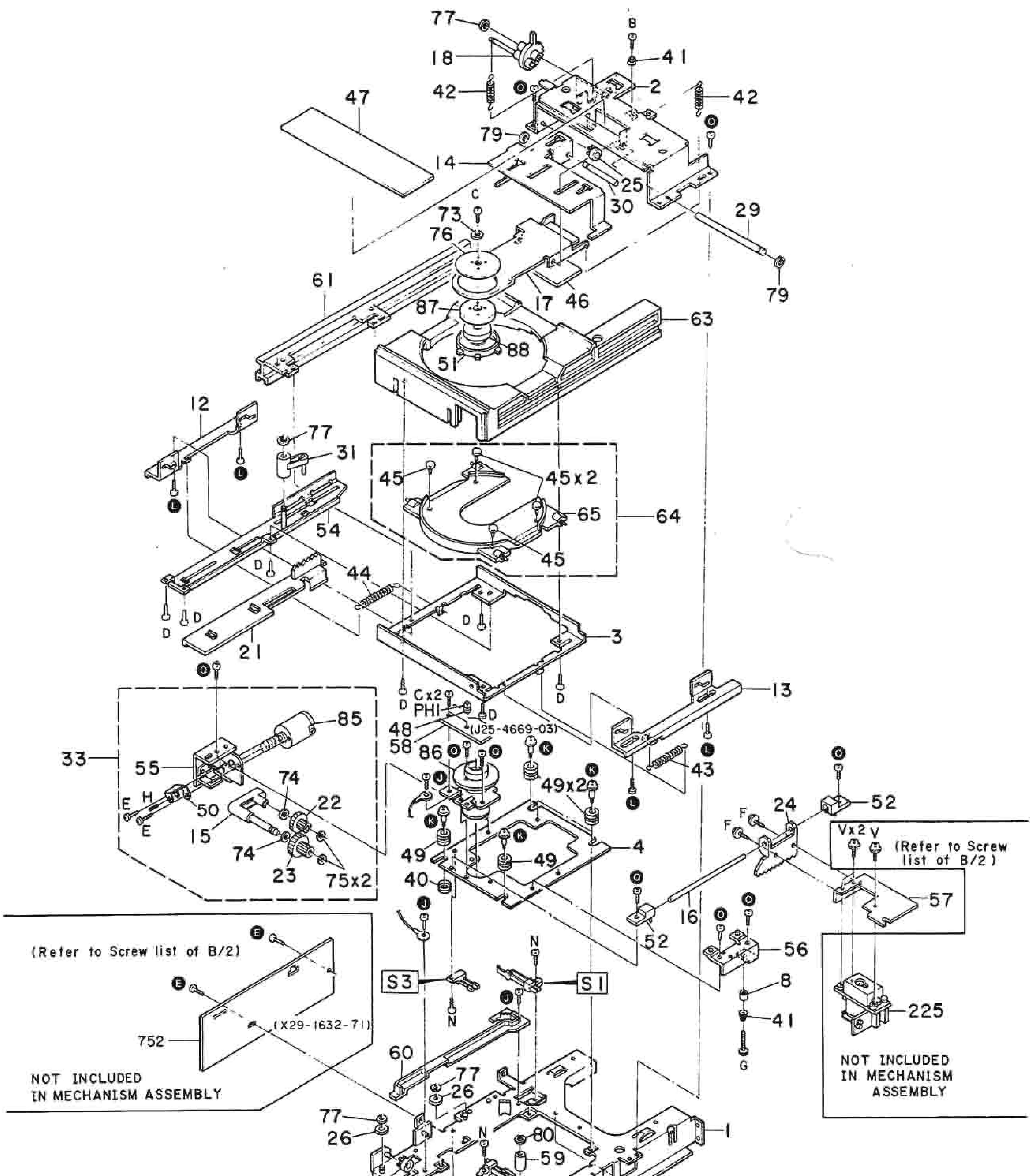
E: Scandinavia & Europe H:Audio Club K:USA P: Canada W:Europe
T: England U: PX(Far East, Hawaii)
UE : AAFES(Europe) X: Australia M: Other Areas

⚠ indicates safety critical components.

EXPLODED VIEW(MECHANISM)

A B

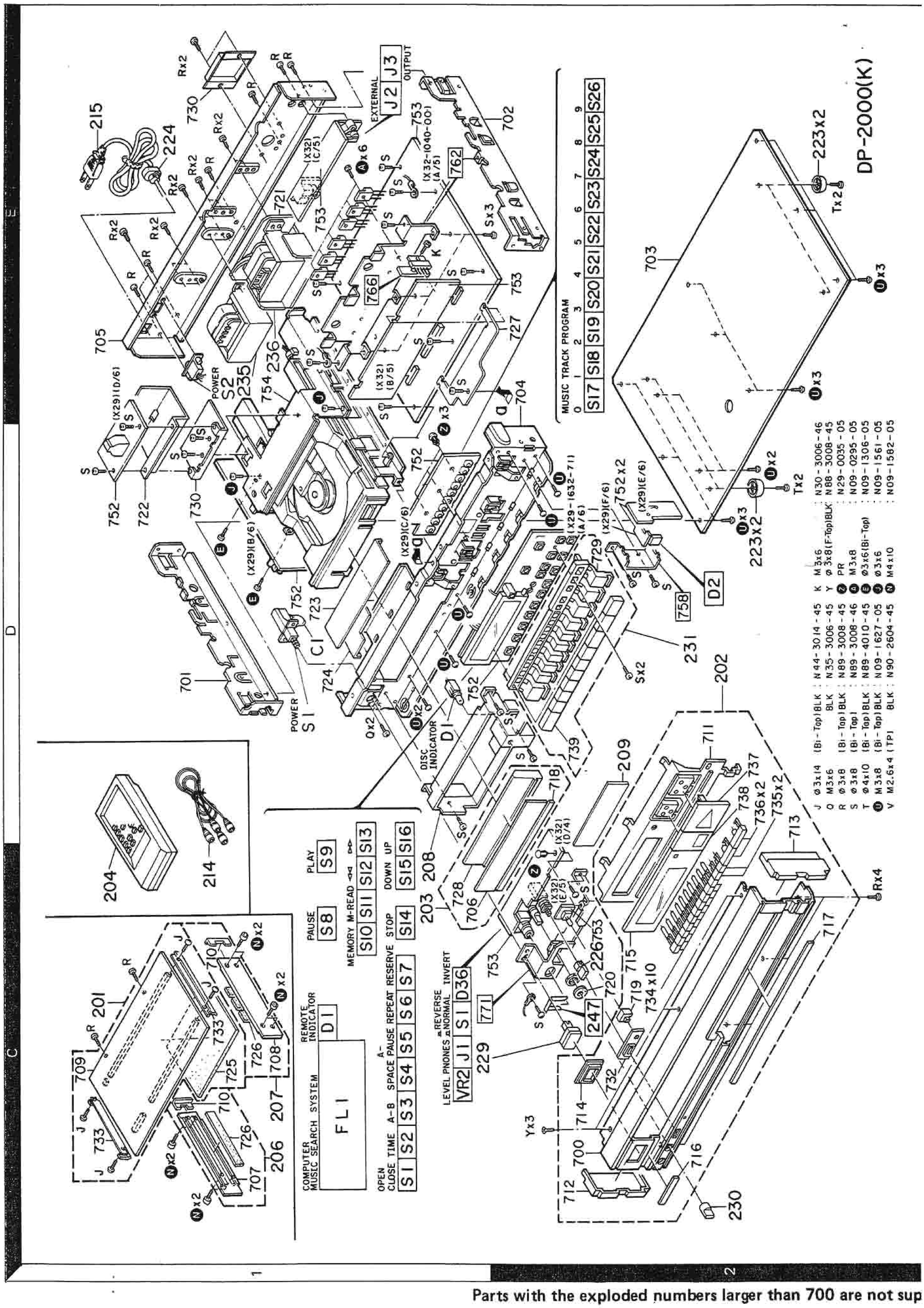
1 2 3



A	M2x3			N30 -2003 -46
B	M3x10	(Bi)	BLK	N35 -3010 -45
C	ø2.6x4	(Bi-Tap)	BLK	N89 -2604 -45
D	ø2.6x10	(Bi-Tap)		N89 -2610 -46
E	M2x5			N30 -2005 -46
F	M3x4	(TP)		N90 -3004 -46
G	M3x14	(Hex Bolt)	NI	N95 -3014 -41
H				N77 -2006 -45
J	M3x6			N09 -1306 -05
K	M2.6x15			N09 -1379 -15
L	M2.6x5			N09 -1380 -05
M	M5x26			N09 -1381 -05
N	M2x6			N09 -1431 -05
P	PR (ø3.5x4.5)			N29 -0067 -05
Q	ø3x6			N09 -1561 -05

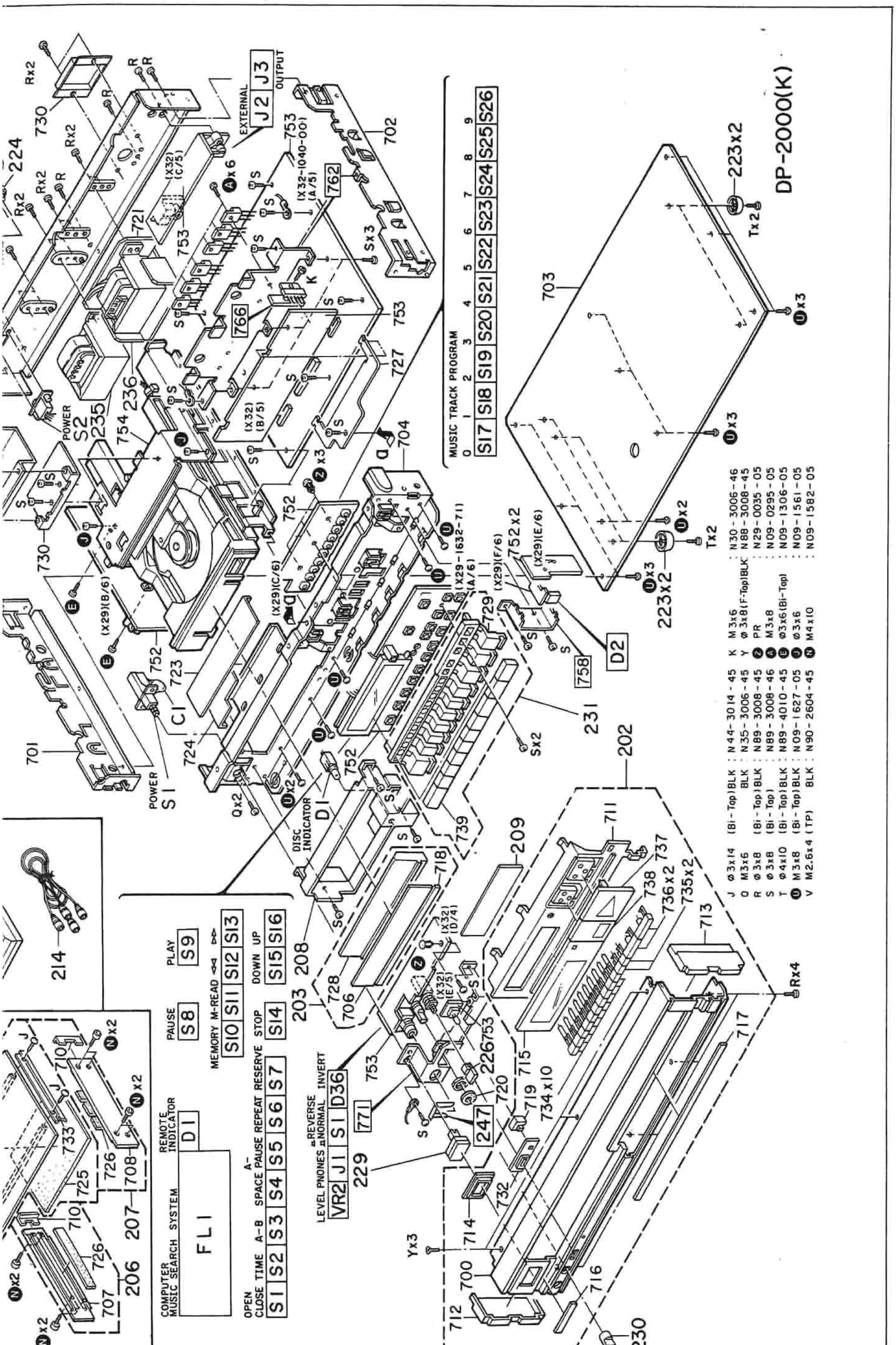
DP-2000(K)

EXPLODED VIEW(UNIT)



Parts with the exploded numbers larger than 700 are not sup

EXPLODED VIEW(UNIT)



Parts with the exploded numbers larger than 700 are not supplied.

LASSIFICATION OF CHIP PARTS

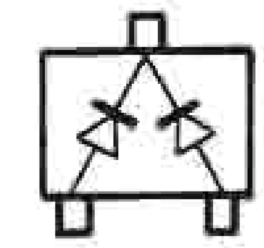
チップ部品の ｱ/Classification of Chip parts

Digital transistor/ﾃ	Symbol/記号	R1	R2
DTA/DTC114E	14/24	10k	10k
DTA/DTC114Y	54/64	10k	47k
DTA/DTC114T	94/04	10k	–
DTA/DTC124E	15/25	22k	22k
DTA/DTC124X	35/45	22k	47k
DTA/DTC143E	13/23	4.7k	4.7k
DTA/DTC143T	93/03	4.7k	–
DTA/DTC144E	16/26	47k	47k
DTA/DTC144W	76/86	47k	22k
DTA/DTC143X	33/43	4.7k	10k

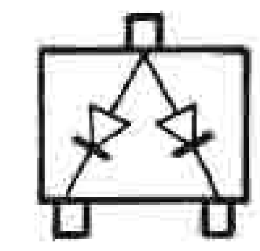
Transistor/トランジスタ	Symbol/記号
2SA1036K	H☐
2SA1037K	F☐
2SC2411K	C☐
2SC2412K	B☐
2SC2413K	A☐
2SC2059K	J☐
2SC3082K	S☐
2SB852K	U☐
2SD1383K	W☐
2SD1757K	AA☐
2SD1328	ID☐
2SC2412LN	L☐

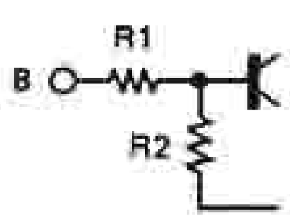
Diode/ダイオード

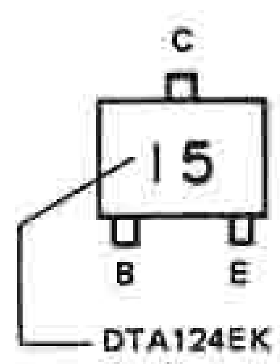
DAN202K Silver/シルバ



DAP202K Green/グリーン

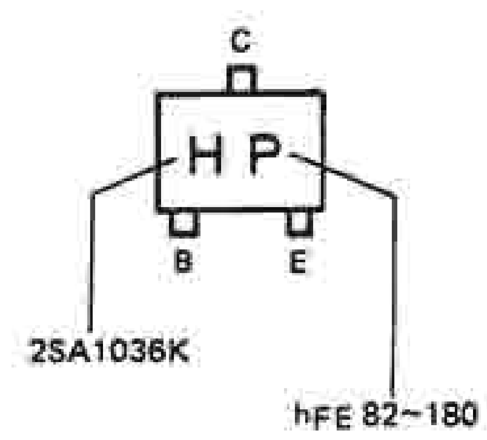






hFE

M	39~ 82
N	56~ 120
P	82~ 180
Q	120~ 270
R	180~ 390
S	270~ 560
E	390~ 820
U	560~1200
A	1000~
B	5000~



⁎ New Parts
Parts without Parts No. are
Les articles non mentionne
Teile ohne Parts No. werden

	Ref. No. 参照番号	Address 位置
	201	1C
	202	2D
	202	2D
	203	1C
	204	1C
	204	1C
	206	1C
	207	1C
	208	1C
	209	2D
	–	
	–	
	–	
	–	
	–	
	–	
	–	
	–	
	–	
	–	
	–	
	–	
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	–	
	–	
	D1	1D
⚠	C1	
⚠	C1	
	214	1C
⚠	215	1E
⚠	215	1E
⚠	215	1E
⚠	215	1E
	–	
	–	
	–	
	–	
	–	
	–	
	–	
	223	2D, 2E
	224	1E
	225	3B
	–	
	226	2C
	229	1C
	230	2C
	231	2D
	235	1E
	236	1E

E: Scandinavia & Europe H
T:
UE : AAFES(Europe) X:

CLASSIFICATION OF CHIP PARTS

チップ部品の見方/Classification of Chip parts

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DTA/DTC143TK	93/03	4.7k	–
DTA/DTC144EK	16/26	47k	47k
DTA/DTC144WK	76/86	47k	22k
DTA/DTC143XK	33/43	4.7k	10k

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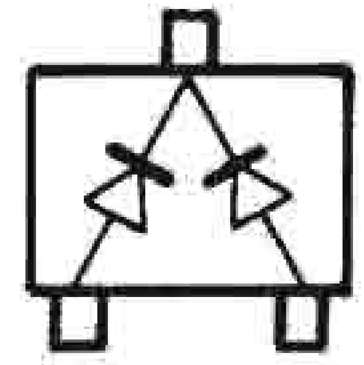
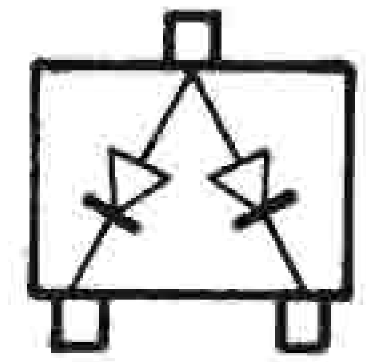
2SC2412K	B□
2SC2413K	A□
2SC2059K	J□
2SC3082K	S□
2SB852K	U□
2SD1383K	W□
2SD1757K	AA□
2SD1328	ID□
2SC2412LN	L□

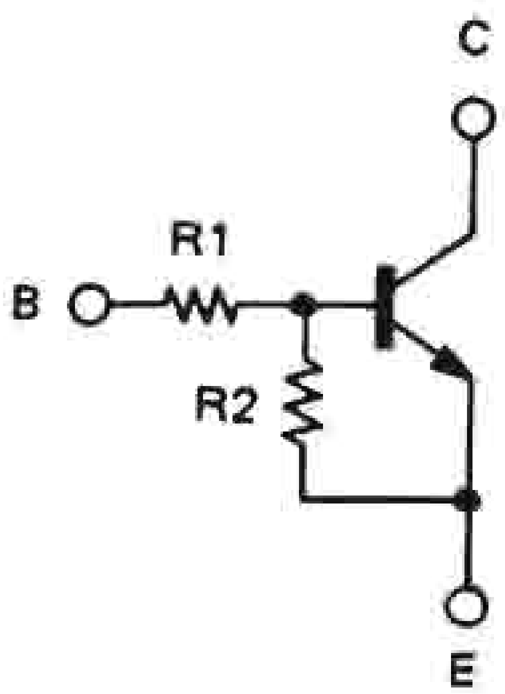
Diode/ダイオード

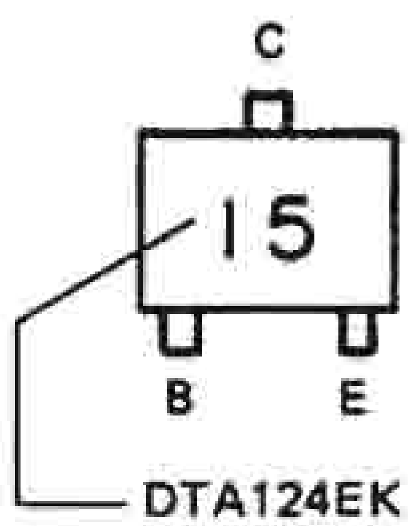
DAN202K Silver/シルバ



DAP202K Green/グリーン







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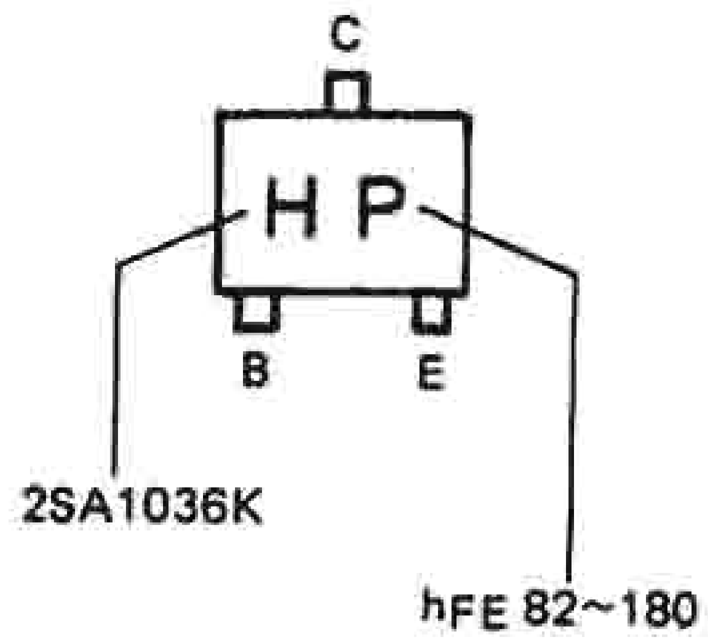

SPECIFICATIONS

Audio

Number of channels .... 2 channels
Frequency response .... 2 Hz ~ 20 kHz, ±0.5 dB
Dynamic range .... 96 dB
Total harmonic distortion .... 0.001% at 1 kHz
Channel separation .... 96 dB at 1 kHz
Wow & flutter .... Unmeasurable limit
Line output level/output impedance .... 2 V/220 ohms
Headphones output level/impedance .... 32 mW/32 ohms

Disc

Playing time .... Approx. 60 min /side
Diameter of the disc .... 120 mm
Constant linear velocity .... 1.2 — 1.4 m/sec.

Signal format

Quantization .... 16 bits linear 1 channel
Sampling frequency .... 44.1 kHz
Channel modulation code .... EFM (eight to fourteen modulation)

Pick up

Type .... Optical pick up
Laser type .... Semiconductor laser

General

Power requirements .... 120 V, 60 Hz (USA and Canada models)
120 V/220 — 240 V, 50/60 Hz (Switchable) (Other Countries)
Power consumptions .... 22 W
Dimentions .... W 440 mm (17-5/16″)
H 95 mm (3-3/4″)
D 313 mm (12-5/16″)
Weight (Net) .... 9.1 kg (20.0 lb)
Supplied accessories .... Remote control unit RC-2000, Connection cables

Note:
We follow a policy of advancements in development. For this reason specifications may be changed without notice.

Note :

Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on, the Europe (E) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

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