9. Circuit Descriptions and List of Abbreviations

1. Introduction
2. Power Supply
3. Loader/Monoboard
4. Data Processing
5. Control and Display
6. Abbreviations

Notes:
- Figures can deviate slightly from the actual situation, due to different set executions.
- For a good understanding of the following circuit descriptions, please use the diagrams in chapter 6 and 7. Where necessary, you will find a separate drawing for clarification.

9.1 Introduction

9.1.1 Features

The SACD 900/DVD962SA range is a new model DVD/SACD player and is equipped with:
- Build in MPEG2, AC-3 and DSD decoder,
- 6 channel audio output,
- RGB video output on SCART (Europe only),
- YUV output,
- Progressive scan (for DVD962SA Non-Europe models),
- CD-RW compatible.

9.1.2 Differences

The SACD 900/DVD962SA is derived from the SACD 1000. It has a new Audio/Video board, Front Display board, Progressive scan board (same as used in Step2001 DVD-player) and another Power Supply module (same as used in Step2001 DVD-players).

9.1.3 Modules

The main modules are:
- Power Supply Unit (PSU).
- Mercury 1 Loader - VAL6011
- ASD1.1 Mono Board.
- Audio Video (A/V) Board.
- Front Display Board.
- Progressive Scan Board.

9.1.4 Service

This ASD1.x has the same ComPair connector as in previous DVD generations.
Flashing of the application-SW is not possible with the ComPair cable, except with a CD-R disc. For sets with Mask-ROM software, replace it with a programmed Flash (available via your Philips Service organisation).

9.2 Power Supply Unit

9.2.1 Introduction

This supply is a Switching Mode Power Supply (SMPS), which uses the control IC UC3842 to produce pulses to drive the power 'switch' (MOSFET). The regulation of the 'duty cycle', controls the supply output, at a fixed switching frequency (approximately 58 kHz, determined by the RC timing components at pin 4).

The UC3842 (item IC1) is a high performance, fixed frequency, current mode controller for DC-to-DC converter applications. This integrated circuit features a:
- trimmed oscillator for precise duty cycle control,
- temperature compensated reference,
- high gain error amplifier,
- current sensing comparator and
- high current totem pole output ideally suited for driving a power MOSFET (item Q1).

Also included are protective features consisting of input and reference under-voltage lockouts each with hysteresis, cycle by cycle current limiting, programmable output dead time and a latch for single pulse metering.

9.2.2 Output Voltages

- +12V_stdby (present during standby).
- +5V_ stdby (present during standby).
- +5V_digital (will switch off via Q3 during Standby).
- +5V_AV (will switch off via Q3 during Standby).
- 3V3 (present during standby).
- -5V (will switch off during standby).

9.2.3 Operation

Power Supply

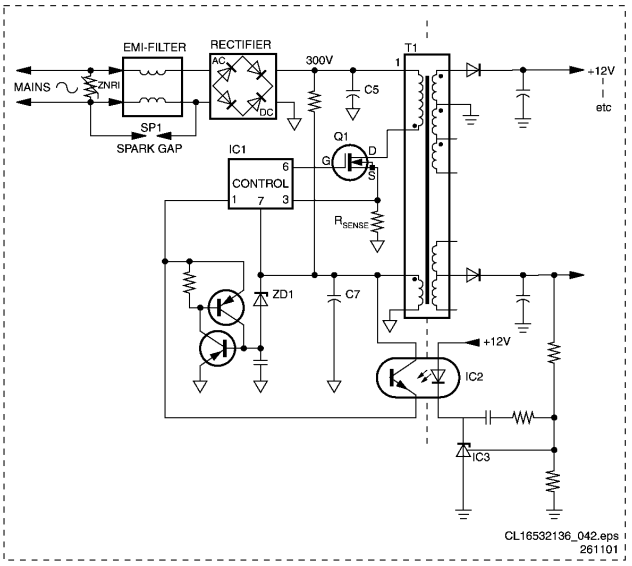


Figure 9-1

Mains Input Circuit
The bridge rectifier (D1-D4) rectifies the mains voltage, after which C5 smoothens this voltage. The DC voltage across this capacitor is the DC input voltage (approximately 300 V), to pin 1 of transformer T1.
The mains input also consists of a (differential mode) lightning protection ZNR1 and a (common mode) lightning protection SP1 (spark gap).

Start-up and Take-over Circuitry

With the mains voltage input, C7 will charge. When this voltage, (at pin 7 of IC1), reaches the start-up threshold of min 14.5 V, the control circuit starts to operate.

After start-up, IC1 requires a maximum sinking current of 17 mA, which the start-up circuitry cannot deliver. Therefore, a take-over circuitry (a coupled winding of transformer T1) is present. The voltage at this point will take over the supply voltage at pin 7 of the IC.

If the take-over circuit does not function, the IC will switch 'off' again at the minimal operating voltage of 8.5 V. The whole operation cycle will repeat itself with audible hiccup sound if take-over is not present.

Secondary Voltage Sensing

The secondary voltage regulating circuit comprises of opto-coupler IC2 (which isolates the error signal from the control IC on the primary side), and a reference component IC3 (TL431). The reference component has two functions:

- a very stable and accurate reference diode
- a high gain amplifier.

TL431

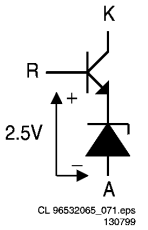


Figure 9-2

When the output voltage increases (due to a reduction in the load), the voltage across R23 increases to above the internal reference voltage of 2.5 V. IC3 will conduct and the current through the opto-coupler will increase. This results in an increase of the voltage at pin 2 of IC1, which will reduce the on time of FET Q1.

In the event of an output voltage decrease (due to an increase in the load), the control circuit will operate in the opposite way.

Primary Current Sensing

The current through FET Q1, will result in a voltage drop across R3A. This line goes to pin 3 of IC1, which is the current sense input. The higher the input voltage, the more the primary current is limited. In this way, the maximum output power of the power supply is limited.

Under-voltage Protection

Two under-voltage lockout comparators are incorporated, to guarantee that IC1 is fully functional
before the output stage is enabled. Separate comparators with built-in hysteresis monitor both the supply voltage at pin 7 and the reference voltage at pin 8.

If the supply voltage at pin 7 drops below 10 V (typical), e.g. due to a shorted secondary voltage or
excessive load, the drive pulse at pin 6 is disabled and the controller will switch 'off'.

Over-voltage Protection

The over-voltage circuitry (ZD1, Q7, and Q8) is used to detect an over-voltage situation on the secondary side of the transformer.

If, after start-up, the voltage at the zenerdiode ZD1 will exceeds its zener voltage, the internal latch circuit is triggered (via pin 1), the output buffer is disabled, and the SMPS goes into over-voltage protection. Now a complete restart sequence is required.

Note: If the event of the over-voltage situation remains present, the SMPS will go in sequence of protection, start-up, protection and the cycle repeats. This effect is highly audible.

9.3 Loader/Monoboard

SD1.1 Loader Assy

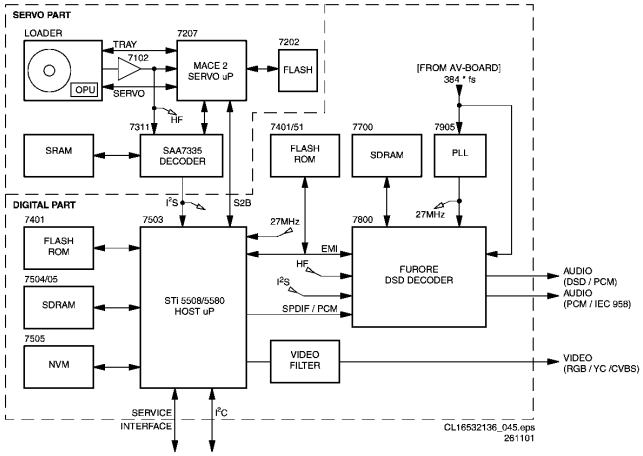


Figure 9-3

9.3.1 The Servo Part

The Optical Unit

The optical unit consists of two lasers, one for CD with a wavelength of 780 nm, and one for DVD with a wavelength of 650 nm. The TZA1033 (item 7102) controls the data from these lasers, and the supply to them.

The Signal Processor TZA1033

The TZA1033 (or DVDALAS2) is an analogue pre-processor and laser supply circuit. It contains data amplifiers and several options for radial tracking and focus control.

It is possible to optimise the dynamic range of this pre-amp/ processor combination for the LF servo and RF data paths. The gain in both channels is separately programmable. This will guarantee an optimal playability for all kind of discs.

Also, a dual laser supply is implemented, with fully automatic laser control including stabilisation and an ON/OFF switch, plus a separate supply pin for power efficiency.

The servo signals go to the MACE2 servo processor, while the HF output signal, goes to the SAA7335 decoder (item 7311).

The Servo Processor MACE2

The servo circuit in the MACE2 IC (item 7207), takes care of the servo controls. In a CD system, there are some 12 control loops active. About six of them are needed to adjust the servo error signals, that is once per disc rotation. It also adjusts offsets, signal amplitudes, and loop gains (AGCs), to enlarge system robustness and to avoid expensive potentiometer adjustments in production.

The other six loops determine the laser spot position on the disc in the radial, axial (focus), and tangential directions.

It also has to take care that the spot accesses a required position as fast as possible. This access system consists of two parts, namely the actuator and the sled, which are (within a certain range) mechanically and electrically independent. Therefore, during an access, the servo has to control as well the actuator as the sled.

The analogue signals from the diode pre-processor are converted into a digital representation using A/D converters. For the communication between the host processor (STi5505) and the servo processor the S2B bus is used, this supports full-duplex asynchronous communication.

Note: For an extensive description of the MACE2 IC, see Service Manual 3122 785 11010.

The Decoder SAA7335

The SAA7335 (item 7311) is a high-end combined Compact Disc (CD) and Digital Versatile Disc (DVD) compatible decoding device. The device operates with an external 32 KB SRAM for DVD error correction and de-interleaving operations.

This IC decodes EFM or EFM+HF signals directly from the laser pre-amplifier, including analogue front-end, PLL data recovery, demodulation, and error correction.

The analogue front-end input converts the HF input to the digital domain via an 8-bit ADC, proceeded by an AGC circuit to obtain the optimum performance from the converter. An external resonator clocks this block. This subsystem recovers the data from the channel stream. It corrects asymmetry, performs noise filtering and equalisation, and finally recovers the bit clock and data from the channel using a digital PLL. The demodulator part detects the frame synchronisation signals and decodes the EFM (14 bit) and EFM+ (16 bit) data and sub-code words into 8-bit symbols. Via the serial output interface, the I^2S data (audio and video) go to the DVD decoder STi5505.

The spindle-motor interface provides both motor control signals from the demodulator and, in addition, contains a tachometer loop that accepts tachometer pulses from the motor unit. They drive the motor IC (item 7304).
The SAA7335 has two independent microcontroller interfaces. The first is a serial I^2C-bus and the second is a standard 8-bit multiplexed parallel interface. Both of these interfaces provide access to 32 8-bit registers for control and status.

9.3.2 The Digital Part

The Host Processor STi5505

The STi5505 host processor works on 3.3 V (VDD_STI). It comprises the following functions:

- video decoder which supports MPEG1 and MPEG2
- audio decoder which supports AC-3, MPEG1, MPEG2, PCM, 6-channel, virtual surround
- PAL/NTSC video encoder with simultaneously Y/C, CVBS and RGB/YUV outputs
- the video encoder supports Closed Captioning (CC) and MacroVision 7.0/6.1
- full screen On Screen Display (OSD) generator
- on-chip PLLs to generate all necessary clocks (as reference the 27 MHz video clock is used).

Input

Input data comes from the I^2S-bus. The front-end interface of this device, accepts DVD, CD and CD-DA information.

Signal Processing

For video, the input data stream is decoded to the appropriate MPEG, Sub Picture, and OSD data streams, after which they are fed to the PAL/NTSC encoder. This cell will convert the digital MPEG/Sub Picture/OSD stream into a standard base band signal and into RGB components. It handles interlaced and non-interlaced data, can perform CC/TXT encoding, and allows MacroVision copy protection.

For audio, the processing cell is a fully compatible Dolby AC-3, MPEG1, MPEG2, PCM decoder, capable of decoding 5.1 and 2 channel streams.

Output

For video, six analogue output pins are available on which CVBS, S-VHS (Y/C), and RGB/YUV signals are present. They go directly to the A/V board.

For audio, the STi5505 has three PCM digital outputs (for 6-channel analogue audio):

- PCM_OUT0: left and right (to pin 60 of FURORE IC7800).
- PCM_OUT1: centre and LFE (to pin 61 of FURORE IC7800).
- PCM_OUT2: left and right surround (to pin 62 of FURORE IC7800).

The FURORE SACD processor

General

The FURORE-IC is a one-chip design, containing all the hardware that is required for SACD processing. It is intended to interface with the STi-family (STi5505/STi5508) DVD video-decoders.
The FURORE-IC contains a memory interface to support an external 16 or 64 Mbit SDRAM.
During SACD application, the STi5505 serves as a host, whereby the FURORE is controlled via the EMI interface. The FURORE processing part is not used during all other play modes. In these modes, the PCM audio signals are fed through the FURORE to the appropriate DAC.

Block Diagram

FURORE

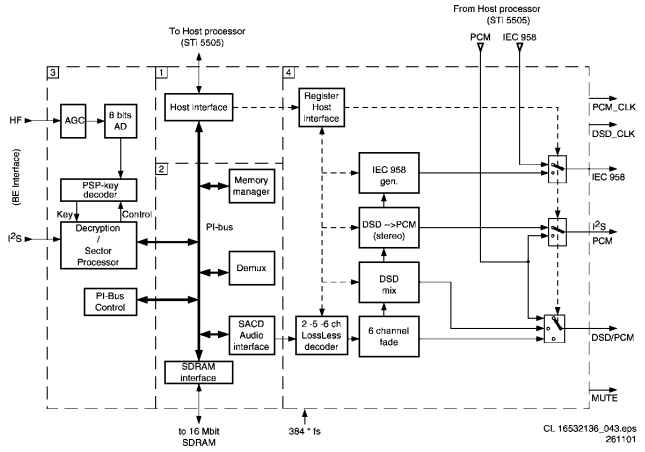


Figure 9-4

We can divide the FURORE-IC in four main parts (see block diagram):

1. **Host interface.** This is the link between the host bus and the internal registers and memory bus. It also supplies the general reset signal (HW and SW) and the interrupt signals.
2. **Data processing.** All modules and peripherals in this part are connected to a so-called PI-bus. It is beyond the scope of this manual to go more in detail on this subject.
3. **Copy protection.** On every SACD disc, a PSP-signal is recorded. The player can only play a disc if a valid PSP-signal is detected. This PSP-key is recorded, via a special mechanism, in the EFM-signal on the disc. To detect this key, the analogue HF-signal from the optical pick-up unit is fed directly to the FURORE-IC. Via an AGC, the signal is fed to an ADC. The digitised HF signal is then fed to a block where key is encrypted. Control of this process is done via the host interface (sector processor).
4. **DSD decoding and post processing.** In this part, all processing is done to generate a DSD and/or an I^2S stream (from the de-multiplexed stream coming from the data processing block), in such a way that it can directly be connected to a DA-converter. All processing is done on $384 * f_S$.

Interfaces

- Basic Engine Interface:
  - **Data input interface.** The Basic Engine Interface (I^2S), is connected to the output of the SAA7335 (HD61) high speed CD decoder.
  - **Analogue HF input.** The analogue HF input, coming from the optical pickup unit (OPU), is also fed to the FURORE-IC, to extract the copy-protection information PSP (Pit Signal Processing = invisible data is stored on to disc, which is required to decrypt the encrypted content).

- SDRAM Interface: The SDRAM interface forms a glue less interface to one 16 Mbit (or one 64 Mbit) SDRAM device. The interface takes care for the power-up sequence, mode programming and refreshing of the SDRAM devices. This is hard coded in the interface and does not have to be controlled by the host.

- Audio data input/output Interface:
  - **DSD/PCM combined data output.** DSD_PCM: Output intended for a combined 6-channel DSD (SACD) and PCM (DVD-CDDA) DAC. Switching between the PCM data coming from the STi5505, and the internal generated DSD signals, is done in the FURORE IC.
  - **Stereo DSD only output.** DSD_stereo: 2-channel DSD output with stereo down mix in the case of 5- and 6-channel, and normal stereo in case of 2-channel DSD mode.
  - **Stereo PCM data output.** Two possible stereo sources can be selected as stereo PCM output:
    1. Stereo PCM coming from the STi5505 via the PCM input on Furore.
    2. Stereo or down-mix-PCM derived via a decimation filter from the SACD-DSD signal.
  - **Digital audio output interface (IEC958).** The IEC958 format is intended to connect the SACD 900 to a digital receiver. No DSD signals are defined for IEC958, therefore the 'DSD-->PCM converted' signal is transmitted. Following two types of signals are possible on the digital interface:
    1. IEC958 data coming from the STi5505.
    2. IEC958 data (stereo or down-mix-PCM) derived via a decimation filter from the SACD-DSD signal.
  - **Clock + reset input.** Two different processing clocks and a reset pulse are needed:
    1. Sys_clk: System clock for data processing part, frequency can be 27 MHz or 768 * f_S.
    2. 384 * f_S: Processing clock for LLD and post processing.
    3. RESETn is an asynchronous reset and should be low for at least 1 period of DSD_CLK.

Memory

SDRAM

The size of the SDRAM is 2 times 16 Mbit or 1 time 64 Mbit (not simultaneously).
The SDRAM (items 7504 and 7505) has the following functions:

- it is used by the MPEG video decoder as a frame buffer,
- it holds the software and the variables used by it.

Flash-ROM

A 2MB Flash-ROM (item 7401) holds the DVD firmware, and is controlled by pin 16 (FLASH_OEN) of the STi5505. It must be able to perform a download (by disk or OS-link) in a Flash-only system.

EEPROM

User settings, player settings, and region code are stored in a 32 Kb I²C EEPROM.

9.4 Data Processing

9.4.1 Audio/Video (A/V) Board

General

This board is the interface panel between the DVD-player and its peripherals. See also block diagram in Chapter 6. This board has some added features compared to the 2nd generation DVD 2B.
The control of the A/V board is done by the I²C-decoder IC7107 (see table below):

Description	Pin	Hi	Lo
CLK_SEL	12	Internal clock	External clock
CLKFREQSEL	11	384 * fs	192 * fs
DAC_RESET	10	Normal	Reset
DSD_PCM	6	DSD stream output	PCM stream output
SACD_ACT	5	SACD	CD
SACD_BASSMGT	4	Configure 0 (LLL1)	Configure 1 (SSS1)
VMUTE	7	Video mute (audio direct)	No video mute
Reserved	9		

Block diagram

A/V Board

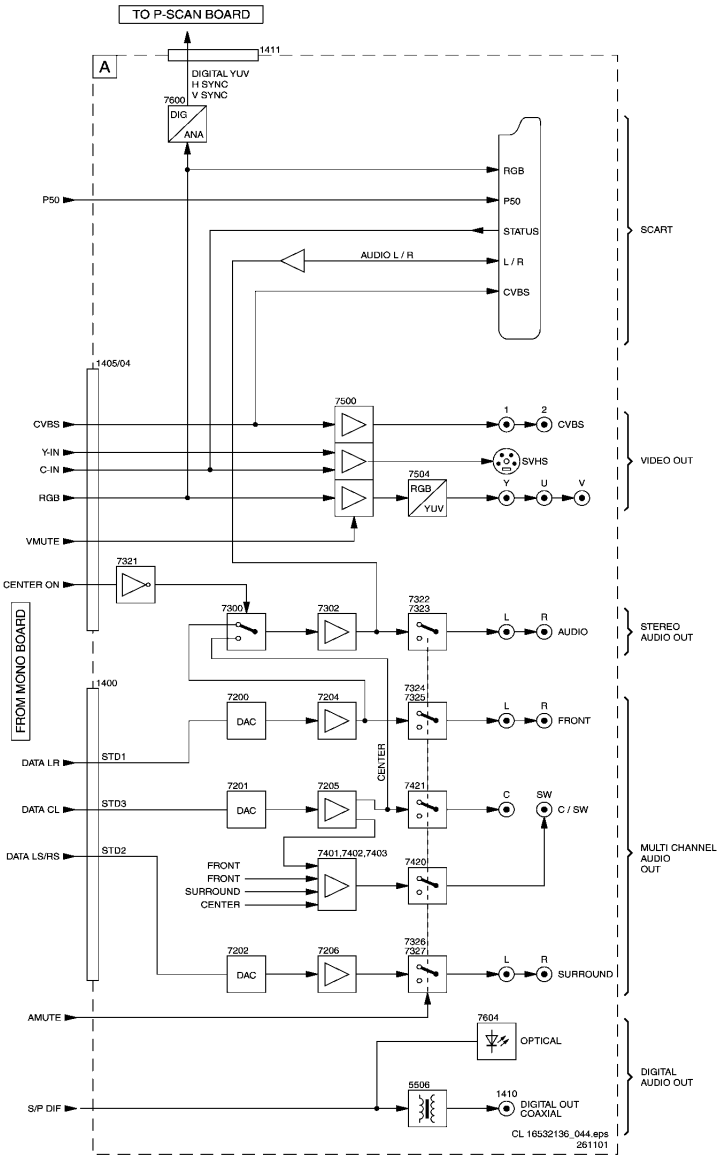


Figure 9-5

Video

The analogue video signals from the SD1.1 Mono Board are fed to video buffer LA7109 (item 7500). Then (for Europe) they

go directly to the SCART plug or the appropriate VIDEO OUT cinch connectors.
The video output from the STi5505 is RGB, YC, and CVBS. To get YUV output, an RGB to YUV conversion matrix (item 7504) is necessary.

It is possible to set the SACD player in 'audio direct' mode. This means that there is no video output from the A/V board. This is indicated by a blue LED on the front panel, and is controlled via the VMUTE control signal from pin 7 of IC7107.

Audio
The digital audio signals are fed to three DACs for the 6-channel audio output:
- 7200 (CS4397) for the front left and right channel,
- 7201 (CS4392) for the centre and subwoofer,
- 7202 (CS4392) for the rear left and right channel.

All these DACs can accept both DSD and PCM data streams from the SD1.1.

Front channels
Due to the gain difference between DSD and PCM in the CS4397, an external circuit (7222, 7221 and 7203) is added to perform hardware attenuation for PCM data. It is controlled via the DSD_PCM control signal (pin 6 of IC7107):
- When this signals is 'low' (= PCM), the voltage at pin 28 is 3.3 V, resulting in 5 dB attenuation.
- When this signal is 'high' (= DSD), the voltage at pin 28 of IC7200 is 5 V, resulting in no attenuation.

After the DAC, the signals are amplified again with 5dB (IC7204) to compensate for the gain loss in the DAC.

Rear channels
All the rear channels have the same gain.

Centre channel
There is a control line from the STi5505, called CENTRE_ON, which is used to switch between the centre channel and front channels for both SACD- and DVD modes (see figure above).

Speaker setting for '6 channel DSD '
The SACD 900 will support two speaker-settings in this mode. This is controlled via the SACD_BASSMGT control signal (pin 4 of IC7107). This will switch a 120 Hz filter 'on' or 'off', for bass enhancement.
This setting is always 'off' when the set is playing PCM-stream.

9.4.2 Progressive Scan Board (if present)

General
The DVD962SA series offer progressive scan YUV outputs (only for non-Europe models).

Block Diagram

Progressive Scan Board

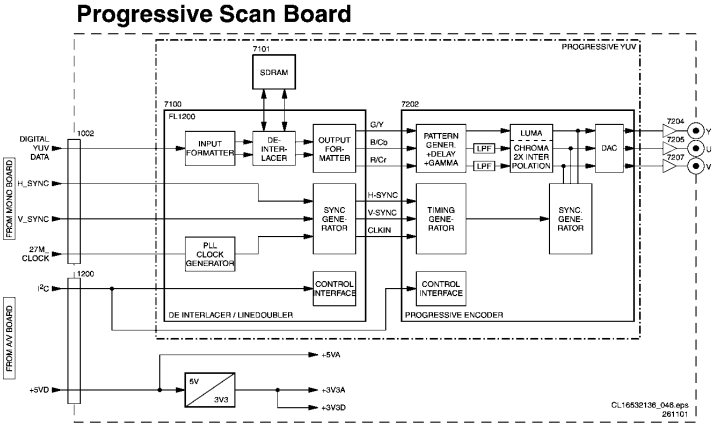


Figure 9-6

Progressive YUV
This creates a picture signal with double the scan lines of a conventional interlaced picture, to create a noticeably sharper and smoother image. It offers higher picture resolution and eliminates virtually all motion artefacts. Even on large screens, the progressive scan lines are barely noticeable and it reduces picture flickering significant.

This board also offers the Digital Crystal Clear feature, which allow you to fine-tune the following parameters:
- Gamma correction,
- Chroma and Luma delay.

9.5 Control and Display Panel

9.5.1 Control

Slave Processor
The most important component on this board is the (slave) microprocessor (item 7401). It works on an 8 MHz resonator (item 1119) and has a RESET circuit (7105), which is triggered by the +5Vstb. After the RESET pulse, the STB_CONT line will release the reset of the host microprocessor (see circuit around TS7452 on the Monoboard, diagram 4)
In addition, when going to Standby, the slave processor will reset the host processor. When the slave processor receives the correct IR (or key) code to leave the Standby mode, it resets the host processor.
Other slave processor functions are:
- generation of a scanning grid for the keys,
- generation of the display grid and segment scanning,
- generation of square signal to generate the filament voltage for FTD display,
- inputs for RC5/6 and P50 (P50 controller is build in).

Standby LED
Transistor 7104 drives the Standby LED. When the STBLED signal from the slave processor is 'high', the LED is 'off'.

Key Matrix
When a key on the local keyboard is pressed, the signal at the scanning pins of the microprocessor goes from +5 V to 0 V.

IR Receiver
The IR controller in the slave processor handles both RC5 and RC6 signals. The logic is +5 V for 'high' and 0 V for 'low'.

P50 Interface
P50 (or Easylink) is a bi-directional serial interface for communication between video equipment. For European sets, this communication goes via pin 10 of the SCART connector, while for other regions (when present), this is a cinch connector. The slave processor controls the P50 bus.

9.5.2 Display

FTD Display
The slave processor has an internal square signal generator (42 kHz), to generate the AC filament voltage. TS7106 and 7109 amplify the square signal before it is applied to the display.
The necessary power supply of -32 V is derived from the -40 V signal via voltage regulator 7400.

DVDALAS2plus Advanced Analogue DVD Signal Processor and Laser Supply

TZA1033

FEATURES

- Operates with DVD-ROM,DVD-RAM, DVD+RW, DVD-RW, CD-ROM and CD-RW media
- Operates up to 64x CD-ROM and 8x DVD-ROM
- Support for Dual Light pen DVD systems (DVD/CDRW)
- DVD-RAM (C) playback capability
- DVD-RAM Land-Groove servo polarity switching
- 3 different tracking servo strategies:
  Conventional 3 beam tracking for CD
  Differential Phase Detection (DPD) for DVD-ROM (including option to emulate traditional drop out detection; drop out concealment)
  Advanced Push Pull with dynamic offset compensation for DVD-RAM (recorded and unrecorded areas)
- Radial error signal for fast track counting (FTC)
- 2 different strategies to read header data:
  - Full bandwidth Push Pull signal
  - Left and Right side signal
- Universal photo diode IC interface using internal conversion resistors and offset cancelation
- Flexible adaption to different light pen configurations
- Input buffer amplifiers with low-pass filtering
- RF data amplifier with wide (programmable) bandwidth equivalent to 64xCD / 8x DVD when using equaliser function
- Built-in equalisers cover CAV inner-outer disc range at highest speed.
- Programmable RF gain for DVD-ROM / DVD-RAM / CD-RW / CDROM applications(approx 50dB range)
- Balanced RF-Data signal transfer (single ended still supported)
- Fully automatic laser control including stabilization and an ON/OFF switch, plus a separate supplypin for power efficiency
- Automatic monitor diode polarity selection.
- 3 and 5 V compatible digital interface
- Enhanced signal conditioning in DPD circuit for optimal tracking performance under noisy conditions.

GENERAL DESCRIPTION

The DVDALAS2 is an analogue preprocessor and laser supply circuit for DVD / CD read only players. The device contains data amplifiers, several options for radial tracking and focus control. The preamplifier forms a versatile, programmable interface between dual, voltage output CD/DVD mechanisms to Philips' digital signal processor family for CD and DVD (Gecko, HDR65, Iguano, etc..)

The device contains serval options for radial tracking:
Conventional 3 beam tracking for CD;
Differential Phase Detector (DPD) for DVD;
Push Pull for DVD-RAM with flexible L/R weighing to compensate dynamic offsets e.g. beamlanding offset.
A radial error signal is generated to allow fast track count (FTC) during track jumps.

The dynamic range of this preamp/processor combination can be optimized for the LF servo and RF data paths. The gain in both channels can be programmed separately. This will guarantee an optimal playability for all kind of discs.

Several functions are included to allow playback of DVD-RAM(C) discs:

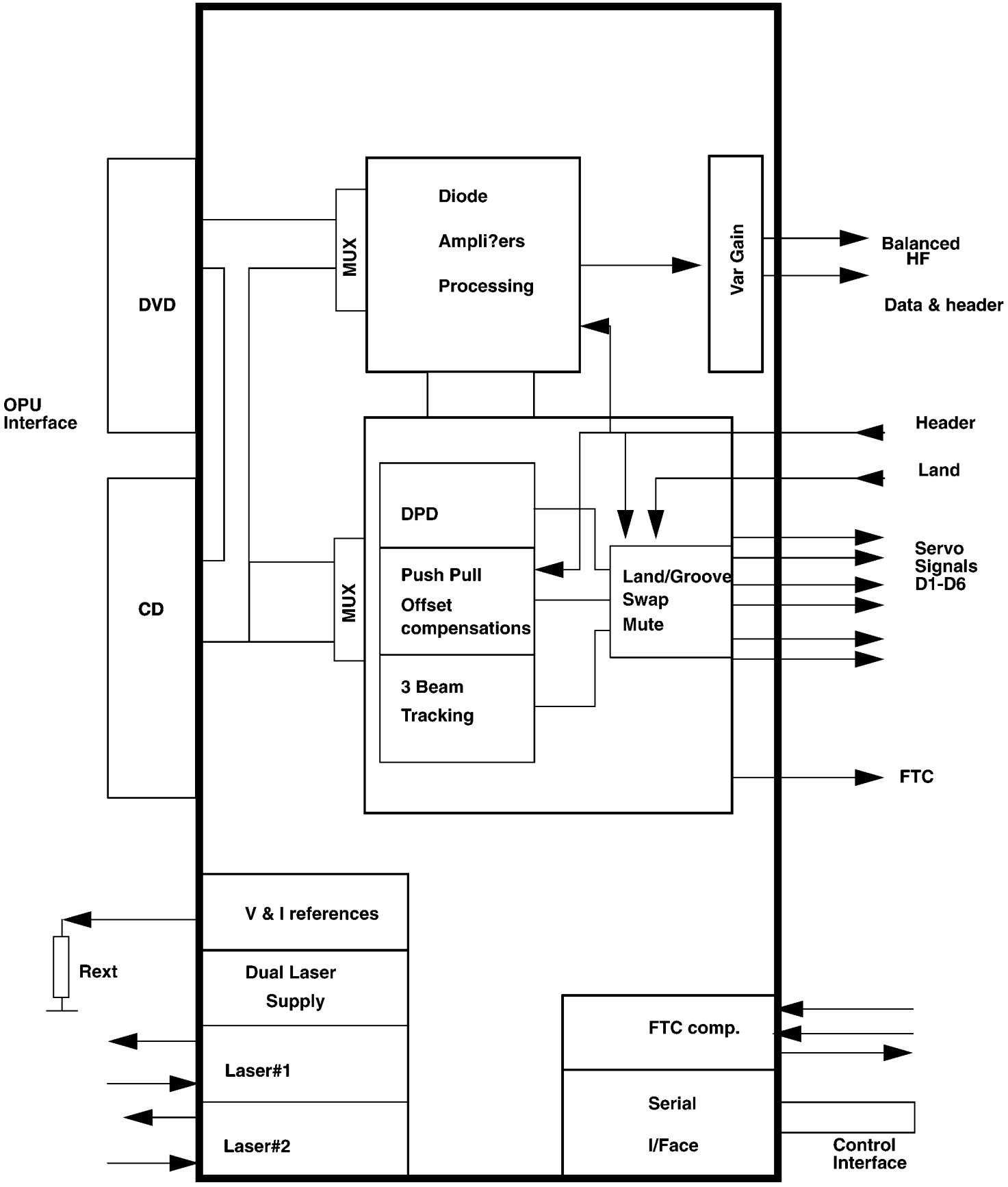
- The header information can be read via the data output path (RF)
- DC offset compensation techniques provide a fast settling after disc errors.
- Radial servo Polarity switch for land/groove
- two settings for focus offset correction for land and groove

The device can accommodate astigmatic, single foucault and double foucault detectors and can be used with P-type lasers with N- or P-sub monitor diodes. After an initial adjustment, the circuit will maintain control over the laser diode current. With an on-chip reference voltage generator, a constant and stabilized output power is ensured independent of ageing. A separate power supply connection allows the internal power dissipation to be reduced by connecting a low voltage supply.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA1023	LQFP64	Plastic low pro?le QFP64; body 10 x 10 x 1.4 mm	SOT314-2

DEVICE BLOCK DIAGRAM



PINNING

Name	Pin	Description
CD-A	1	CD pick up input A
CD-B	2	CD pick up input B
CD-C	3	CD pick up input C
CD-D	4	CD pick up input D
CD-REF	5	CD pick up reference voltage
CD-E	6	CD pick up input E
CD-F	7	CD pick up input F
DVD-A	12	DVD pick up input A
DVD-B	13	DVD pick up input B
DVD-C	14	DVD pick up input C
DVD-D	15	DVD pick up input D
DVD-ref	16	DVD pick up reference voltage
O-A	48	Servo current output for Focus-A
O-B	47	Servo current output for Focus-B
O-C	46	Servo current output for Focus-C
O-D	45	Servo current output for Focus-D
O-central	40	Testpin for offset cancelation
TD2	37	Internally connected
FTC-ref	36	Servo output voltage reference input
S1	42	Servo current output for radial tracking
S2	41	Servo current output for radial tracking
TD1	35	Internally connected
FTC	33	Fast track count voltage output
RFP	55	pos. RF output signal
RFN	56	neg. RF output signal
RF-REF	54	DC Reference signal input RF
LPF-DPD1	38	DPD Low pass bandwidth capacitor, channel pos
LPF-DPD2	39	DPD Low passbandwidth capacitor, channel neg
Land	20	Land/groove toggle input
HEADER	21	Header detector window input
CD-MI	62	CD laser monitor input
DVD-MI	10	DVD laser monitor input
CD-LO	61	CD laser output
DVD-LO	64	DVD laser output
COP	27	Positive inputFTC comparator
COM	28	Inverting inputFTC comparator
COO	29	FTC comparator output

Name	Pin	Description
SIDA	23	Serial host interface data input
SICL	24	Serial host interface clock input
SILD	25	Serial host interface load
VDDA1	8	Analog Supply voltage 1 (RF input)
VDDA2	59	Analog Supply voltage 2 (RF internal)
VDDA3	53	Analog Supply voltage 3 (RF output stage)
VDDA4	44	Analog Supply voltage 4 (Servo)
VDDD5	30	Digital Supply voltage (5V dig core)
VDDD3	22	Digital Supply voltage (3V I/O pads and FTC comp.)
VDDL	63	Supply voltage for laser
VSSA1	9	Analog Ground 1
VSSA2	58	Analog Ground 2
VSSA3	57	Analog Ground 3
VSSA4	43	Analog Ground 4
VSSD	26	Digital ground
Rext	60	Reference current input (Connect 12k1 to VSSA4)
STB	31	Standby input
TM	19	Testmode input
TDO	34	test data out

PINNING

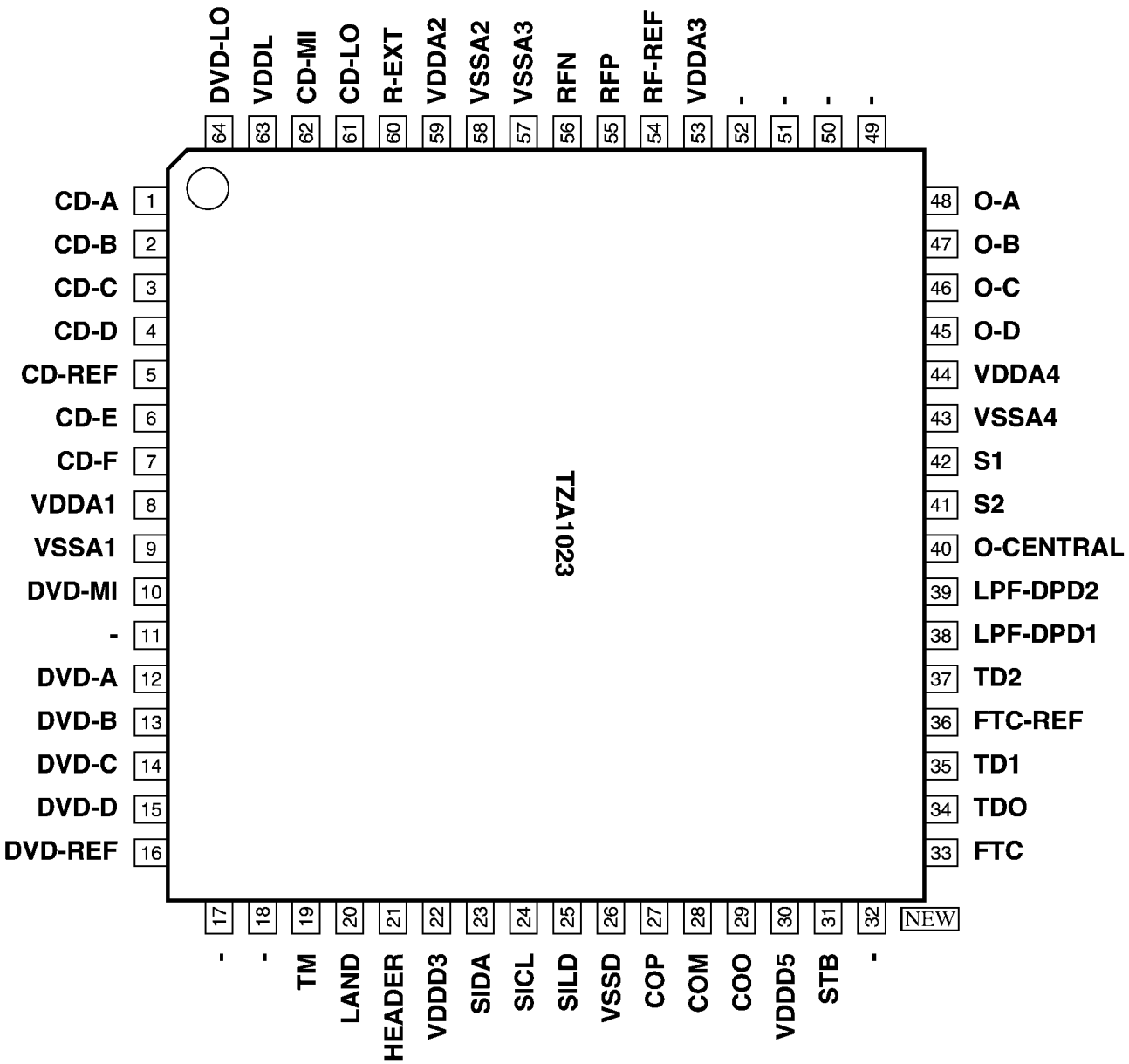


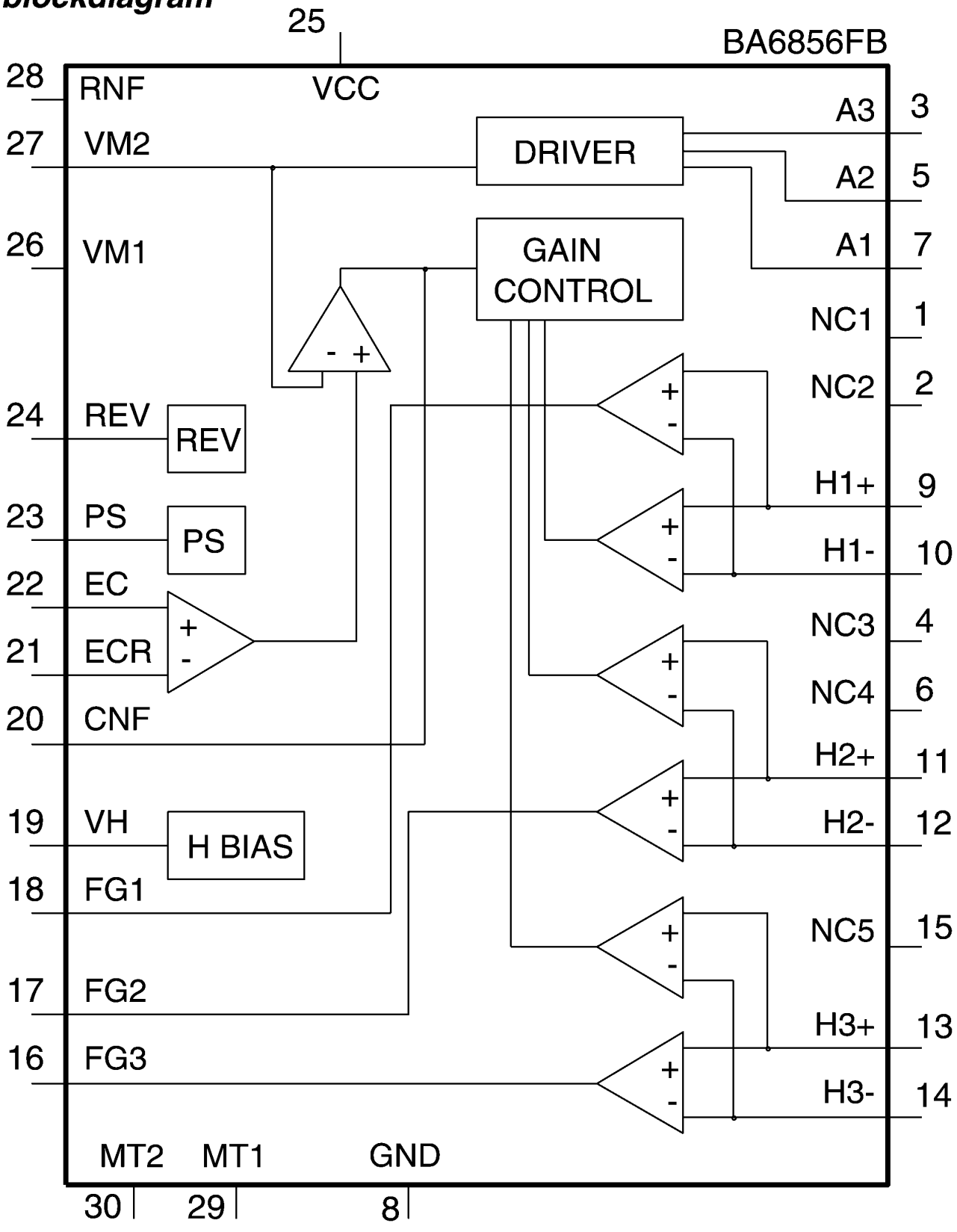
Fig.2 Pin configuration.

BA6856FP: 3 PHASE MOTOR DRIVER FOR DVD PLAYERS

Features

- /3-phase, full-wave pseudo linear driving system
- built-in power save
- built-in therma shut down circuit
- built-in current limit circuit
- built in Hall bias circuit
- built in FG-output (3-phase parallel output)
- with switching function of regular/ reverse rotations

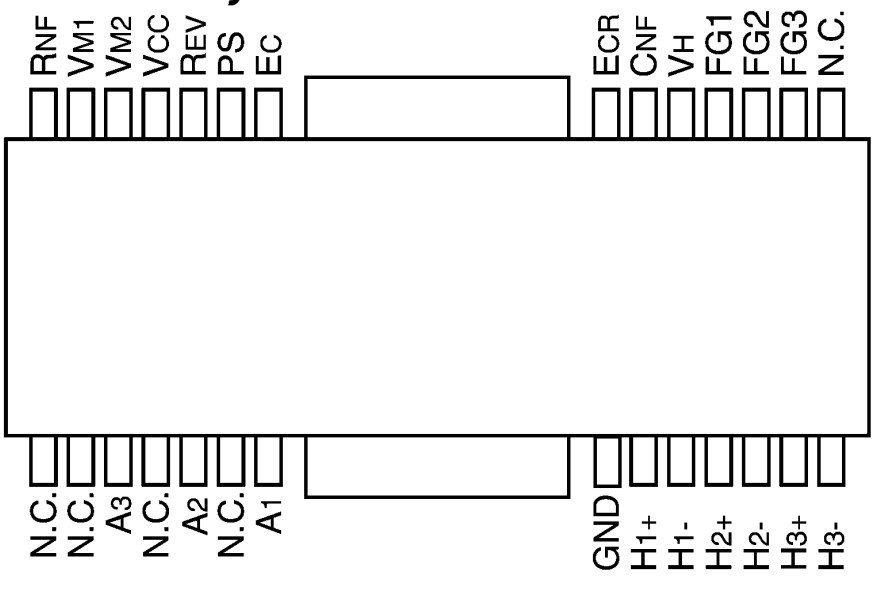
blockdiagram



pin description

PIN No	PIN NAME	DESCRIPTION
1	N.C.	Not connected
2	N.C.	Not connected
3	A_3	Output 3 for motor
4	N.C.	Not connected
5	A_2	Output 2 for motor
6	N.C.	Not connected
7	A_1	Output 1 for motor
8	GND	Ground
9	H_1^+	Hall input Amp1. positive input
10	H_1^-	Hall input Amp1. negative input
11	H_2^+	Hall input Amp2. positive input
12	H_2^-	Hall input Amp2. negative input
13	H_3^+	Hall input Amp3. positive input
14	H_3^-	Hall input Amp3. negative input
15	N.C.	Not connected
16	FG3	FG3 signal output terminal
17	FG2	FG2 signal output terminal
18	FG1	FG1 signal output terminal
19	V_H	Hall Bias
20	C_{NF}	Capacitor connection pin for phase compensation
21	E_{CR}	Torque control standard voltage input terminal
22	E_C	Torque control voltage input terminal
23	PS	POWER SAVE switch
24	R_{EV}	Reverse terminal
25	V_{CC}	Power supply for sinal division
26	V_{M2}	Power supply 2 for driver
27	V_{M1}	Power supply 2 for driver
28	R_{NF}	Power supply for driver division
FIN	FIN	GND

Terminal lay-out



DSP for CD and DVD-ROM systems

SAA7335

FEATURES

- Compatibility with CD-I, CD-ROM, MPEG-video DVD-ROM and DVD-video applications
- Designed for very high playback speeds
- Typical CD-ROM operation up to n = 12, DVD-ROM to n = 1.9, maximum rates (tbf)
- Matched filtering, quad-pass error correction (C1-C2-C1-C2), overspeed audio playback function included (up to 3 kbytes buffer)
- Lock-to-disc playback, Constant Angular Velocity (CAV), pseudo-Constant Linear Velocity (CLV) and CLV motor control loops
- Interface to 32 kbytes SRAM for DVD error correction and de-interleave
- Sub-code/ header processing for DVD and CD formats
- Programmable HF equalizer
- In DVD mode it is still compatible with Philips block decoders
- Sub-CPU interface can be parallel or fast I^{2}C-bus
- On-chip clock multiplier.

GENERAL DESCRIPTION

This device is a high-end combined Compact Disc (CD) and Digital Versatile Disc (DVD) compatible decoding device. The device operates with an external 32 kbytes S-RAM memory for de-interleaving operations. The device provides quad-pass error correction for CD-ROM applications (C1-C2-C1-C2) and operates in lock-to-disk, CAV, pseudo CLV and CLV modes.

In DVD modes double-pass C1-C2 error correction is used which is capable of correcting up to 5 C1 frame errors and 16 C2 frame errors.

The SAA7335 contains all the functions required to decode an EFM or EFM+ HF signal directly from the laser pre-amplifier, including analog front-end, PLL data recovery, demodulation and error correction. The spindle motor interface provides both motor control signals from the demodulator and, in addition, contains a tachometer loop that accepts tachometer pulses from the motor unit.

The SAA7335 has two independent microcontroller interfaces. The first is a serial I^{2}C-bus and the second is a standard 8-bit multiplexed parallel interface. Both of these interfaces provide access to a total of 32 $\times$ 8-bit registers for control and status.

This data sheet contains an descriptive overview of the device together with electrical and timing characteristics. For a detailed description of the device refer to the user guide *"SAU/UM96018"*.

Supply of this CD/DVD IC does not convey an implied license under any patent right to use this IC in any CD or DVD application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
I_{DDD}	digital supply current	–	70	300	mA
V_{DDA}	analog supply voltage	4.5	5.0	5.5	V
I_{DDA}	analog supply current	–	70	300	mA
f_{xtal}	crystal input frequency	4	25	tbf	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C
T_{stg}	storage temperature	–55	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7335GP	LQFP100	plastic low pro?le quad ?at package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

BLOCK DIAGRAM

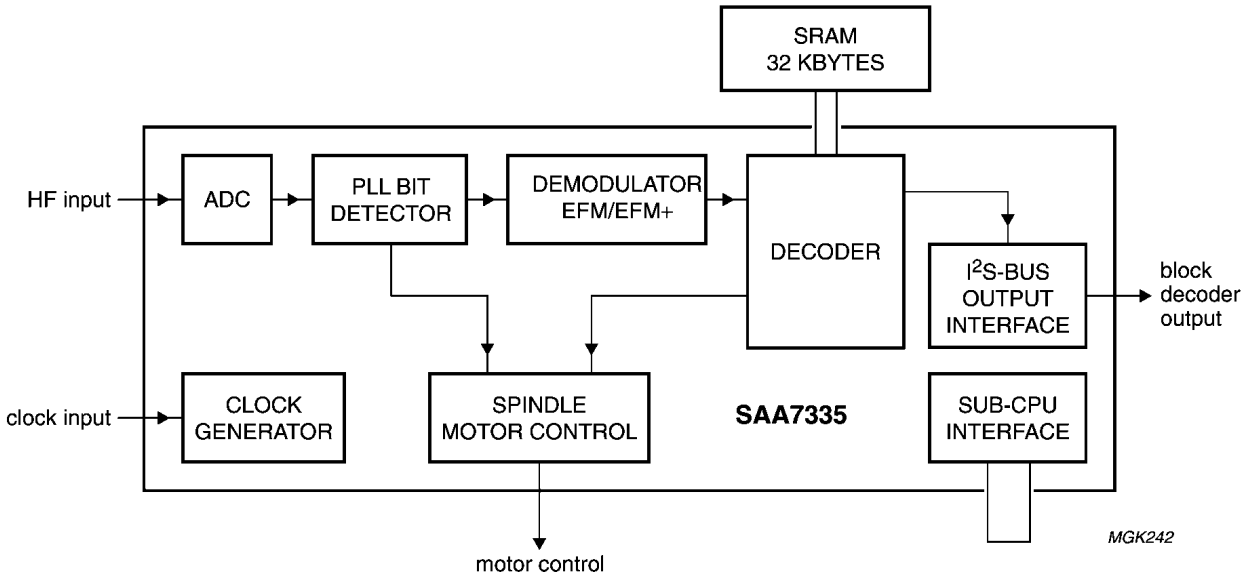


Fig.1 Simplified block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
V_{SSA1}	1	supply	analog ground 1
I_{ref}	2	I	analog current reference input for ADC
REFLo	3	I	analog low reference input for ADC
REFHi	4	I	analog high reference input for ADC
VREF	5	I	analog negative input
HFIN	6	I	analog positive input
V_{SSA2}	7	supply	analog ground 2
AGCOUT	8	O	analog test pin output
V_{DDA2}	9	supply	analog supply voltage 2
V_{DDD1}	10	supply	digital supply voltage 1
V_{SSD1}	11	supply	digital ground 1
OTD	12	I	off track detect input
MOTO1	13	O	3-state motor control output
n.c.	14	–	not connected, reserved
MOTO2/T3	15	I/O	motor control output/tachometer 3 input
n.c.	16	–	not connected, reserved
T1	17	I	tachometer 1 input
T2	18	I	tachometer 2 input
V_{DDD2}	19	supply	digital supply voltage 2
V_{SSD2}	20	supply	digital ground 2
TEST1	21	I	test input 1
TEST2	22	I	test input 2
POR	23	I	power-on reset input
MUXSWICH	24	I	use clock multiplier input
n.c.	25	–	not connected, reserved
CL1	26	O	divided clock output
BCAIN	27	I	BCA input
SDA	28	I/O	sub-CPU I^2C-bus serial data input/output
SCL	29	I	sub-CPU I^2C-bus serial clock input
INT	30	O	sub-CPU interrupt output (open-drain)
V_{DDD3}	31	supply	digital supply voltage 3
V_{SSD3}	32	supply	digital ground 3
da7	33	I/O	sub-CPU data bus bit 7 input/output (parallel)
da6	34	I/O	sub-CPU data bus bit 6 input/output (parallel)
da5	35	I/O	sub-CPU data bus bit 5 input/output (parallel)
n.c.	36	–	not connected, reserved
da4	37	I/O	sub-CPU data bus bit 4 input/output (parallel)
n.c.	38	–	not connected, reserved
da3	39	I/O	sub-CPU data bus bit 3 input/output (parallel)
da2	40	I/O	sub-CPU data bus bit 2 input/output (parallel)

SYMBOL	PIN	TYPE	DESCRIPTION
da1	41	I/O	sub-CPU data bus bit 1 input/output (parallel)
n.c.	42	–	not connected, reserved
da0	43	I/O	sub-CPU data bus bit 0 input/output (parallel)
V_{DDD4}	44	supply	digital supply voltage 4
V_{SSD4}	45	supply	digital ground 4
$\overline{WRi}$	46	I	sub-CPU write enable input (active LOW)
$\overline{RDi}$	47	I	sub-CPU read enable input (active LOW)
ALE	48	I	sub-CPU address latch enable input
CSi	49	I	sub-CPU chip select input (active HIGH)
STOPCLOCK	50	O	stop clock output
n.c.	51	–	not connected, reserved
V4	52	O	serial subcode output (for CD)
EBUOUT	53	O	digital audio output
SYNC	54	O	I^2S-bus sector sync output
FLAG	55	O	I^2S-bus correction ?ag output
DATA	56	O	I^2S-bus serial data output
BCLK	57	I/O	I^2S-bus bit serial clock input/output
WCLK	58	I/O	I^2S-bus word clock input/output
V_{DDD5}	59	supply	digital supply voltage 5
V_{SSD5}	60	supply	digital ground 5
RAMRW	61	O	RAM read/write control output
n.c.	62	–	not connected, reserved
RAMDA7	63	I/O	RAM data bus bit 7 input/output
RAMDA6	64	I/O	RAM data bus bit 6 input/output
RAMDA5	65	I/O	RAM data bus bit 5 input/output
RAMDA4	66	I/O	RAM data bus bit 4 input/output
RAMDA3	67	I/O	RAM data bus bit 3 input/output
RAMDA2	68	I/O	RAM data bus bit 2 input/output
n.c.	69	–	not connected, reserved
RAMDA1	70	I/O	RAM data bus bit 1 input/output
RAMDA0	71	I/O	RAM data bus bit 0 input/output
V_{DDD6}	72	supply	digital supply voltage 6
V_{SSD6}	73	supply	digital ground 6
RAMAD0	74	O	RAM address bit 0 output
RAMAD1	75	O	RAM address bit 1 output
RAMAD2	76	O	RAM address bit 2 output
RAMAD3	77	O	RAM address bit 3 output
RAMAD4	78	O	RAM address bit 4 output
RAMAD5	79	O	RAM address bit 5 output
RAMAD6	80	O	RAM address bit 6 output
V_{DDD7}	81	supply	digital supply voltage 7

SYMBOL	PIN	TYPE	DESCRIPTION
V_{SSD7}	82	supply	digital ground 7
RAMAD7	83	O	RAM address bit 7 output
RAMAD8	84	O	RAM address bit 8 output
RAMAD9	85	O	RAM address bit 9 output
n.c.	86	–	not connected, reserved
RAMAD10	87	O	RAM address bit 10 output
RAMAD11	88	O	RAM address bit 11 output
RAMAD12	89	O	RAM address bit 12 output
RAMAD13	90	O	RAM address bit 13 output
RAMAD14	91	O	RAM address bit 14 output
V_{DDD8}	92	supply	digital supply voltage 8
V_{SSD8}	93	supply	digital ground 8
CRIN	94	I	analog crystal input
CROUT	95	O	analog crystal output
CFLG	96	O	correction statistics output
MEAS1	97	O	front-end telemetry output
V_{DDD9}	98	supply	digital supply voltage 9
V_{SSD9}	99	supply	digital ground 9
V_{DDA1}	100	supply	analog supply voltage 1

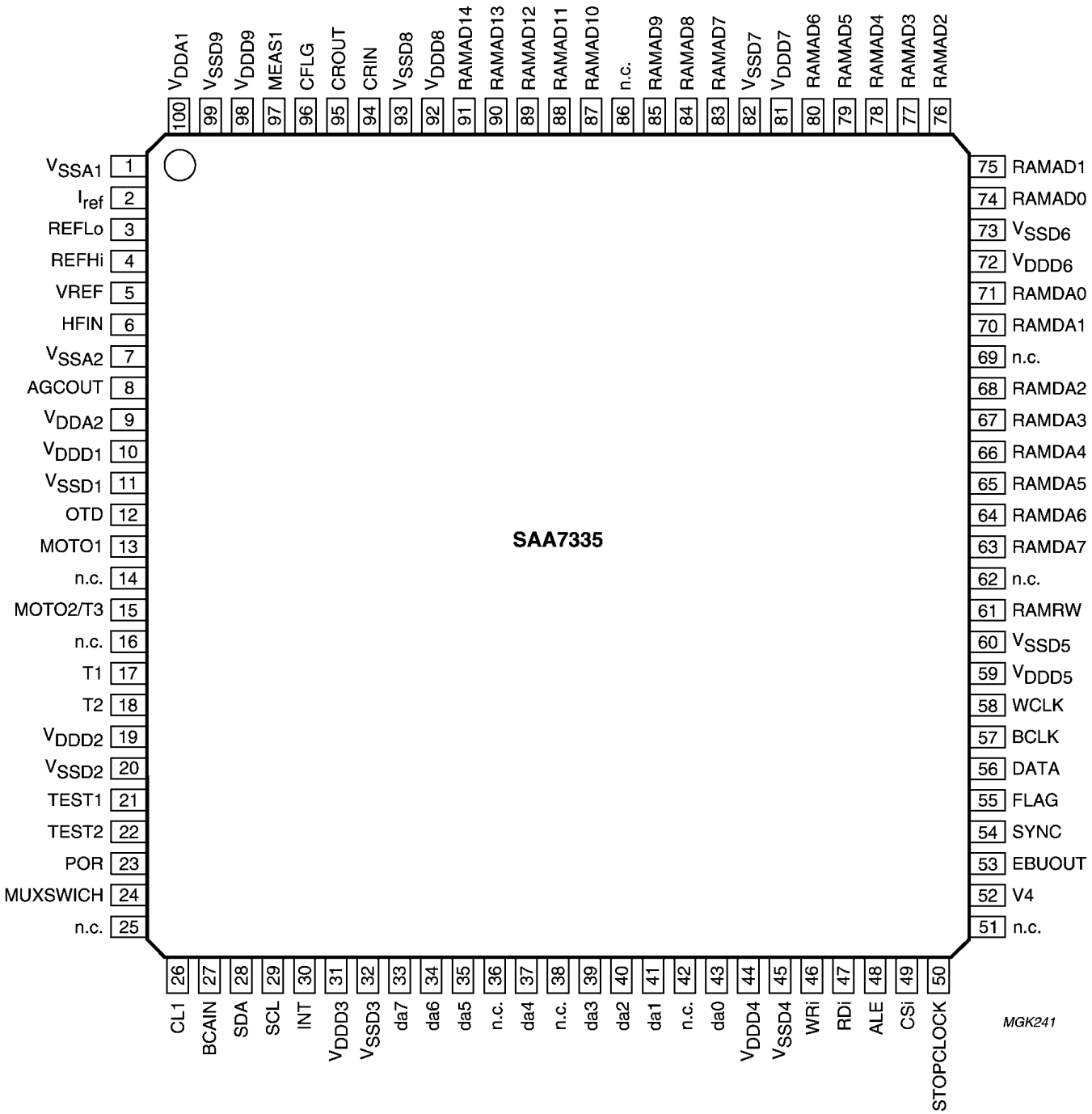


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Analog front-end

This block converts the HF input to the digital domain using an 8-bit ADC proceeded by an AGC circuit to obtain the optimum performance from the convertor. This block is clocked by ADCCLK which is set by the external crystal frequency plus a flexible clock multiplier and divider block.

PLL and bit detector

This subsystem recovers the data from the channel stream. The block corrects asymmetry, performs noise filtering and equalisation and finally recovers the bit clock and data from the channel using a digital PLL.

The equalizer and the data slicer are programmable.

Digital logic

All the digital system logic is clocked from the master ADC clock (ADCCLK) described above.

Advanced bit detector

The advanced bit detector offers improved data recovery for multi-layer discs and contains two extra detection circuits to increase the margins in the bit recovery block:

1. Adaptive slicer: adds a second stage slicer with higher bandwidth
2. Run length 2 push-back: all T2 run lengths are pushed back to T3, thereby automatically determining the erroneous edge and shifting the transitions on that edge.

Demodulator

FRAME SYNC PROTECTION CD MODE

This circuit detects the frame synchronization signals. Two synchronization counters are used in the SAA7335:

1. The coincidence counter: this is used to detect the coincidence of successive syncs. It generates a sync coincidence signal if 2 syncs are 588 ±1 EFM clocks apart.
2. The main counter: this is used to partition the EFM signal into 17-bit words. This counter is reset when:
   a) A sync coincidence is generated
   b) A sync is found within ±6 EFM clocks of its expected position.

The sync coincidence signal is also used to generate the lock signal which will go active HIGH when 1 sync coincidence is found. It will reset to LOW when, during 61 consecutive frames, no sync coincidence is found.

FRAME SYNC PROTECTION DVD MODE

This circuit detects the frame synchronization signals. Two synchronization counters are used in the SAA7335:

1. The coincidence counter: this is used to detect the coincidence of successive syncs. It generates a sync coincidence signal if 2 syncs are 1488 ±3 EFM+ clocks apart.
2. The main counter: this is used to partition the EFM+ signal into 16-bit words. This counter is reset when:
   a) A sync coincidence is generated
   b) A sync is found within ±10 EFM+ clocks of its expected position.

The sync coincidence signal is also used to generate the lock signal which will go active HIGH when 1 sync coincidence is found. It will reset to LOW when, during 61 consecutive frames, no sync coincidence is found.

EFM/EFM+ demodulation

The 14-bit EFM (16-bit EFM+) data and subcode words are decoded into 8-bit symbols.

Microcontroller interface

The SAA7335 has two microcontroller interfaces, one serial I²C-bus and one parallel (8051 microcontroller compatible).

The two communication modes may be operated at the same time, the modes are described below:

1. Parallel mode: protocol compatible with 8052 multiplexed bus:
   a) da0 to da7 = address/data bus
   b) ALE = Address Latch Enable, latches the address information on the bus
   c) $\overline{WRi}$ = active LOW write signal for write to SAA7335
   d) $\overline{RDi}$ = active LOW read signal for read from SAA7335
   e) CSi = active HIGH Chip Select signal (this signal gates the $\overline{RDi}$ and $\overline{WRi}$ signals).
2. I²C-bus mode: I²C-bus protocol where SAA7335 behaves as slave device where:
   a) SDA = I²C-bus data
   b) SCL = I²C-bus clock
   c) I²C-bus slave address (write mode) = 3EH
   d) I²C-bus slave address (read mode) = 3FH
   e) Maximum data transfer rate = 400 kbits/s.

Microcontroller interface (I²C-bus mode)

Bytes are transferred over the interface in single bytes of which there are two types; write data commands and read data commands.

The sequence for a write data command (1 data byte) is as follows:

- Send START condition
- Send address 3EH (write)
- Write command address byte
- Write data byte
- Send STOP condition.

The sequence for a read data command (that reads 1 data byte) is as follows:

- Send START condition
- Send address 3EH (write)
- Write status address byte
- Send STOP condition
- Send START condition
- Send address 3FH (read)
- Read data byte
- Send STOP condition.

Reading and writing data to the SAA7335

The SAA7335 has 32 × 8-bit configuration and status registers as shown in Table 1. Not all locations are currently defined and some remain reserved for future upgrades. These can be written to or read from via the microcontroller interface using either the serial or parallel control bus.

Am29LV160BT/Am29LV160BB

16 Megabit (2 M x 8-Bit/1 M x 16-Bit) CMOS 3.0 Volt-only Sector Erase Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
  - — Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **Manufactured on 0.35 µm process technology**
- **Supports Common Flash Memory Interface (CFI)**
- **High performance**
  - — Full voltage range: access times as fast as 90 ns
  - — Regulated voltage range: access times as fast as 80 ns
- **Ultra low power consumption (typical values at 5 MHz)**
  - — 200 nA Automatic Sleep mode current
  - — 200 nA standby mode current
  - — 10 mA read current
  - — 20 mA program/erase current
- **Flexible sector architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and thirty-one 64 Kbyte sectors (byte mode)
  - — One 8 Kword, two 4 Kword, one 16 Kword, and thirty-one 32 Kword sectors (word mode)
  - — Supports full chip erase
  - — Sector Protection features:

    A hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked in-system or via programming equipment

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 100,000 write cycle guarantee per sector**
- **Package option**
  - — 48-ball FBGA
  - — 48-ball µBGA
  - — 48-pin TSOP
  - — 44-pin SO
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
  - — Provides a hardware method of detecting program or erase cycle completion (not available on 44-pin SO)
- **Erase Suspend/Erase Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - — Hardware method to reset the device to reading array data

GENERAL DESCRIPTION

The Am29LV160B is a 16 Mbit, 3.0 Volt-only Flash memory organized as 2,097,152 bytes or 1,048,576 words. The device is offered in 48-ball FBGA, 48-ball µBGA, 44-pin SO, and 48-pin TSOP packages. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. This device is designed to be programmed in-system with the standard system 3.0 volt V_{CC} supply. A 12.0 V V_{PP} or 5.0 V_{CC} are not required for write or erase operations. The device can also be programmed in standard EPROM programmers.

The device offers access times of 80, 90, and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The Am29LV160B is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

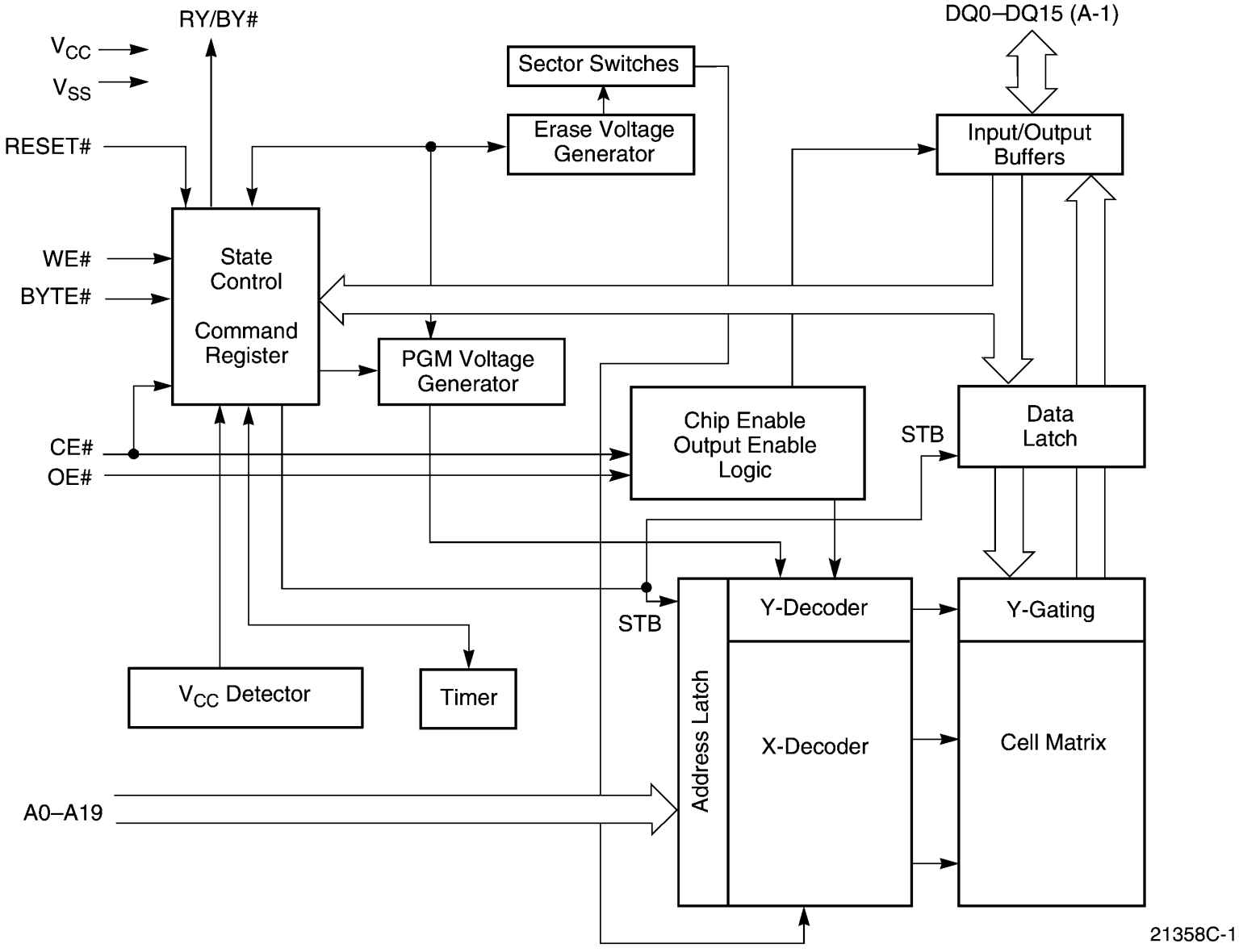
AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

PRODUCT SELECTOR GUIDE

Family Part Number	Am29LV160B		
Ordering Part Number: V_{CC} =3.0–3.6 V	**80R**		
V_{CC} = 2.7–3.6 V		**90**	**120**
Max access time, ns (t_{ACC})	80	90	120
Max CE# access time, ns (t_{CE})	80	90	120
Max OE# access time, ns (t_{OE})	30	35	50

Note: *See "AC Characteristics" for full specifications.*

BLOCK DIAGRAM



PRODUCT SELECTOR GUIDE

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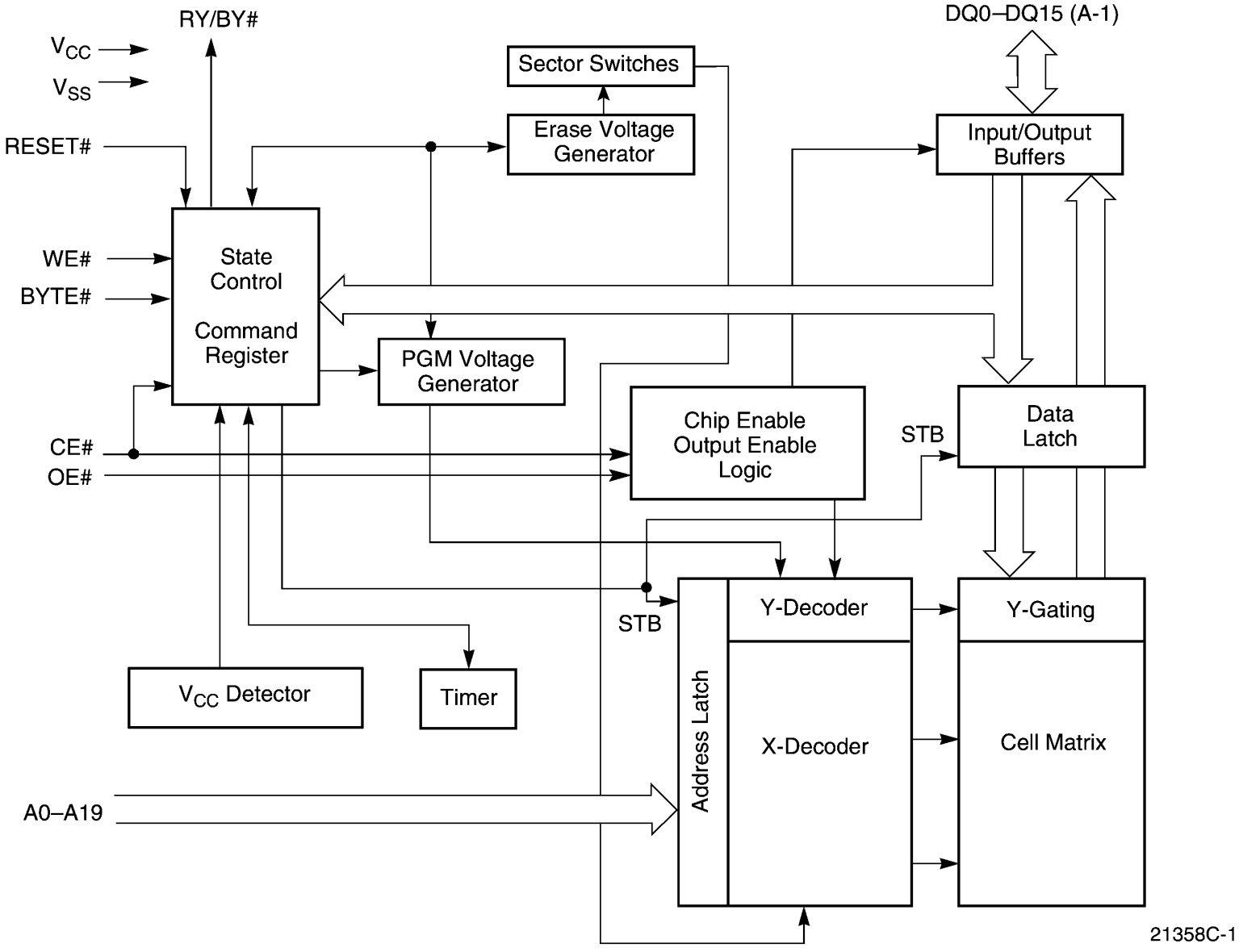
Max access time, ns (t_{ACC})	80	90	120
Max CE# access time, ns (t_{CE})	80	90	120
Max OE# access time, ns (t_{OE})	30	35	50

Note: *See "AC Characteristics" for full specifications.*

BLOCK DIAGRAM



SYNCHRONOUS DRAM

MT48LC1M16A1 S - 512K x 16 x 2 banks

FEATURES

- PC100 functionality
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
  1 Meg x 16 - 512K x 16 x 2 banks architecture with 11 row, 8 column addresses per bank
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge Mode, includes CONCURRENT AUTO PRECHARGE
- Self Refresh and Adaptable Auto Refresh Modes
  - 32ms, 2,048-cycle refresh or
  - 64ms, 2,048-cycle refresh or
  - 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply
- Supports CAS latency of 1, 2 and 3

OPTIONS — MARKING

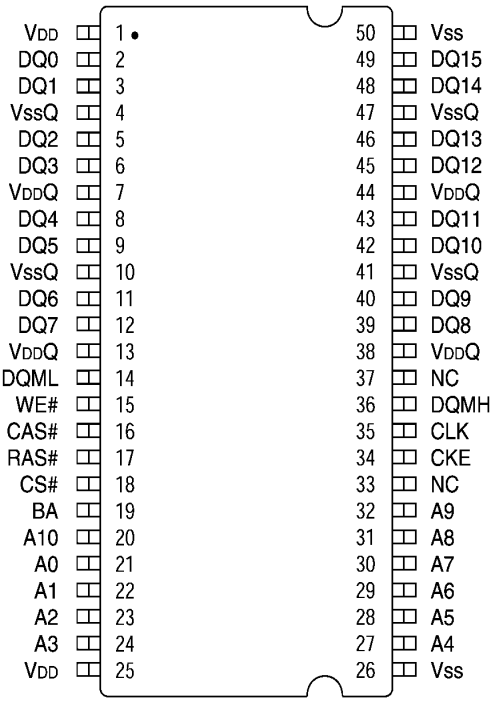
- Configuration
  1 Meg x 16 (512K x 16 x 2 banks) — 1M16A1
- Plastic Package - OCPL*
  50-pin TSOP (400 mil) — TG
- Timing (Cycle Time)
  6ns (166 MHz) — -6
  7ns (143 MHz) — -7
  8ns (125 MHz) — -8A
- Refresh
  2K or 4K with Self Refresh Mode at 64ms — S
- Part Number Example: MT48LC1M16A1TG-7S

KEY TIMING PARAMETERS

SPEED	CLOCK	ACCESS TIME CL = 3**	SETUP	HOLD
-6	166 MHz	5.5ns	2ns	1ns
-7	143 MHz	5.5ns	2ns	1ns
-8A	125 MHz	6ns	2ns	1ns

*Off-center parting line
**CL = CAS (READ) latency

PIN ASSIGNMENT (Top View)
50-Pin TSOP



Note: The # symbol indicates signal is active LOW.

	1 Meg x 16
Configuration	512K x 16 x 2 banks
Refresh Count	2K or 4K
Row Addressing	2K (A0-A10)
Bank Addressing	2 (BA)
Column Addressing	256 (A0-A7)

16Mb (x16) SDRAM PART NUMBER

PART NUMBER	ARCHITECTURE
MT48LC1M16A1TG S	1 Meg x 16

GENERAL DESCRIPTION

The 16Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 16,777,216 bits. It is internally configured as a dual 512K x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 512K x 16-bit banks is organized as 2,048 rows by 256 columns by 16 bits. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed

GENERAL DESCRIPTION (continued)

sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

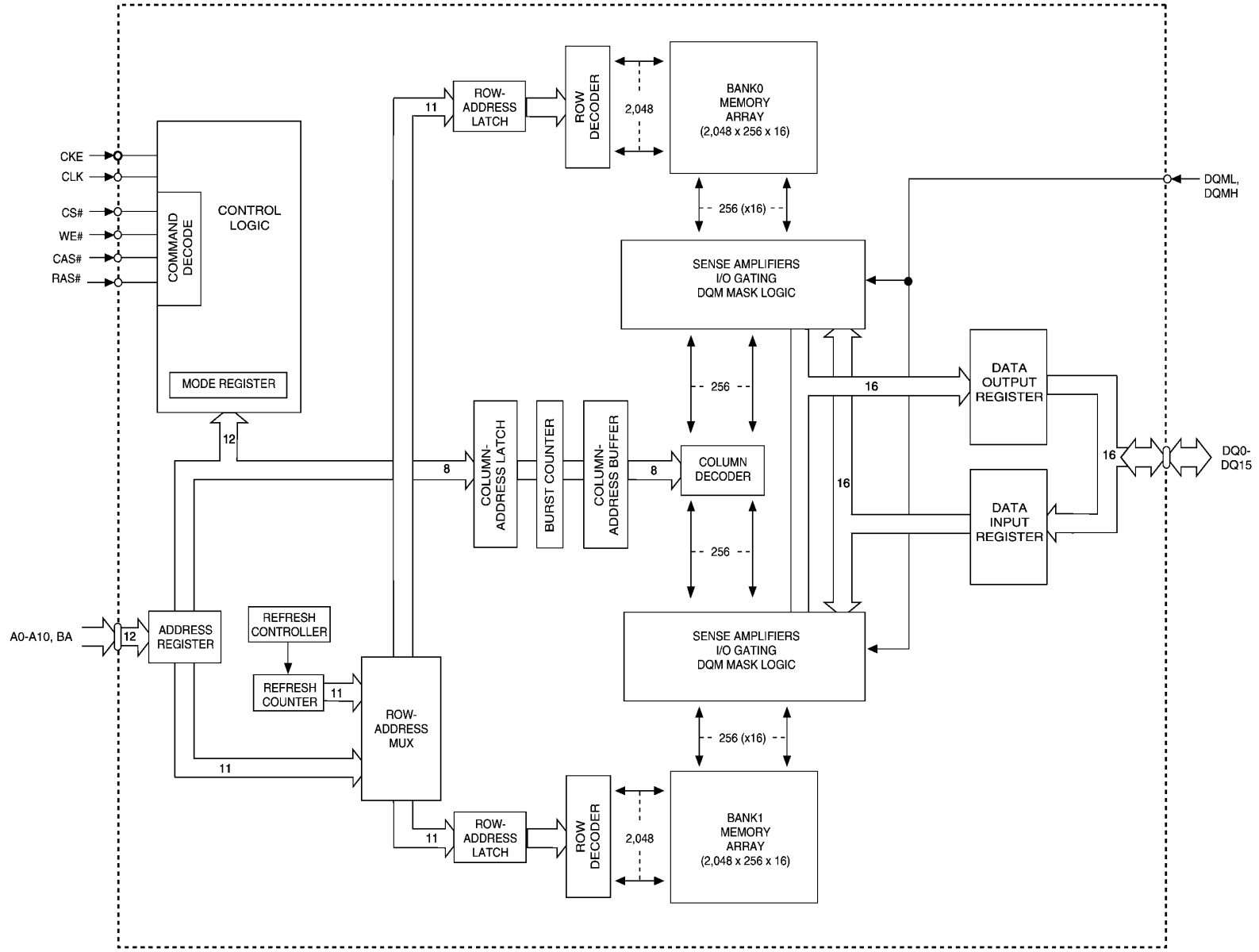
The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 1 Meg x 16 SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2 n rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The 1 Meg x 16 SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

FUNCTIONAL BLOCK DIAGRAM
1 Meg x 16 SDRAM



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
35	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
34	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), ACTIVE POWER-DOWN (row ACTIVE in either bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
18	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
15, 16, 17	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
14, 36	DQML, DQMH	Input	Input/Output Mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. DQML corresponds to DQ0-DQ7; DQMH corresponds to DQ8-DQ15. DQML and DQMH are considered same state when referenced as DQM.
19	BA	Input	Bank Address Inputs: BA defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA is also used to program the twelfth bit of the Mode Register.
21-24, 27-32, 20	A0-A10	Input	Address Inputs: A0-A10 are sampled during the ACTIVE command (row-address A0-A10) and READ/WRITE command (column-address A0-A7, with A10 defining AUTO PRECHARGE) to select one location out of the 512K available in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 3, 5, 6, 8, 9, 11, 12, 39, 40, 42, 43, 45, 46, 48, 49	DQ0-DQ15	Input/ Output	Data I/Os: Data bus.
33, 37	NC	–	No Connect: These pins should be left unconnected.
7, 13, 38, 44	$V_{DD}Q$	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
4, 10, 41, 47	$V_{SS}Q$	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 25	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
26, 50	V_{SS}	Supply	Ground.

STi5505 (Rev. Ax)

DVD BACKEND DECODER WITH INTEGRATED HOST PROCESSOR

PRODUCT PREVIEW

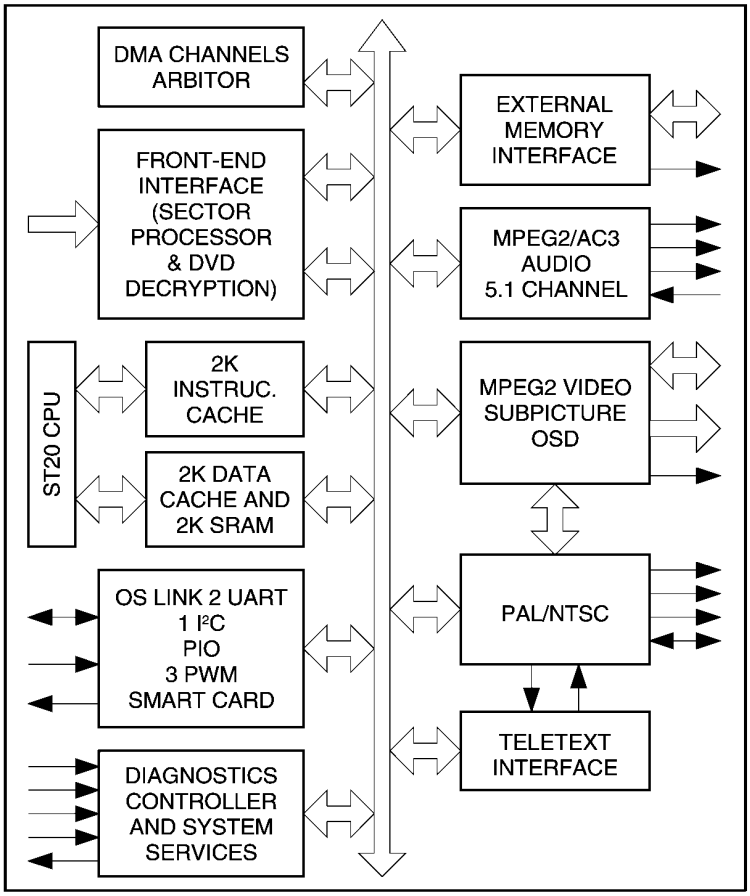
- INTEGRATED 32-BIT RISC HOST CPU
  - 2KBYTES INSTRUCTION CACHE, 2KBYTES DATA CACHE/SRAM
  - 50K DHRYSTONES/SEC (2.1) - 50MHz
- VIDEO DECODER
  - FULLY SUPPORTS MPEG-2 MP@ML
  - MEMORY REDUCTION - PAL IN 12MBITS
- SUBPICTURE DECODER
- HIGH PERFORMANCE ON-SCREEN DISPLAY
- AUDIO DECODER
  - 5.1 CHANNEL DOLBY AC-3® / MULTI CHANNEL MPEG-2 DECODING
  - DOWNMIX TO STEREO OR TO DOLBY PRO-LOGIC COMPATIBLE OUTPUTS FOR MPEG-2 AND AC-3
  - IEC6958 - IEC61937 COMPATIBLE OUTPUT
  - LPCM (DVD) MODE SUPPORTED
  - 6 CHANNELS OUTPUT
- PAL/NTSC ENCODER
  - MACROVISION™ 7.01/6.1 COMPATIBLE
  - TELETEXT, AND CLOSED CAPTION
- HIGH PERFORMANCE SDRAM INTERFACE
- PROGRAMMABLE MEMORY INTERFACE FOR DRAM, ROM, PERIPHERALS ETC.
- FRONT-END CHANNEL IC INTERFACE
  - DVD, VCD AND CD-DA COMPATIBLE
  - DSS - DVB BISTREAMS
  - SERIAL AND PARALLEL INTERFACES
  - HARDWARE SECTOR FILTERING
  - INTEGRATED CSS DECRYPTION AND TRACK BUFFER
- INTEGRATED PERIPHERALS
  - 2 UARTS, 1 I^2C CONTROLLER, 3 PWM OUTPUTS, 3 TIMERS, 3 CAPTURE TIMERS, SMART CARD
  - 34 BITS OF PROGRAMMABLE I/O
  - OS LINK
- PROFESSIONAL TOOLSET SUPPORT
  - ANSI C COMPILER AND LIBRARIES
  - OPERATING SYSTEMS SUPPORT
  - ADVANCED DEBUGGING TOOLS
- 208 PIN PQFP PACKAGE

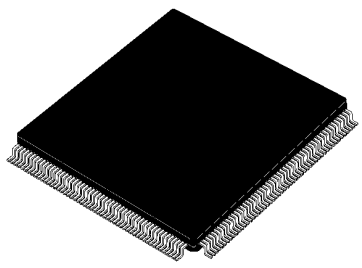
DESCRIPTION

The STi5505 provides a very highly integrated back-end solution for DVD and combo DVD-DVB (Set Top Box) applications. The STi5505 incorporates a host CPU which handles both general application (DVD navigation, CD-DA, VCD, DVB) and drivers of the different embedded periphals (audio/video, subpicture decoders, OSD, PAL/NTSC encoder...).

The STi5505 offers one of the best cost-effective (memory savings, internal peripherals availability) solution to DVD-DVB applications with rapid time to market (Reference design, DVD-DVB Software Toolkit).

Figure 1 : General Block Diagram





PQFP208 (Plastic Quad Flat Pack)

ORDER CODE : STi5505ACV

I - GENERAL DESCRIPTION

The performance offered by the ST20 CPU and its associated hardware (decoders, encoder, peripherals...) allows an integrated and unified DVD or DVD-DVB software solution.

All the following operations are performed inside the STi5505 :

- application management (DVD Navigation, VCD, CD-DA, DVB-Program Guide ...),
- device data retrieval drivers (demultiplex, stream buffer management ...),
- device presentation drivers (video decoder, subpicture decoder, on-screen display, audio decoder, PAL/NTSC encoder ...),
- embedded peripherals drivers (UART, I^2C, Programmable I/O, Smart Card ...).

I.1 - ST20 32-bit CPU

The ST20 micro-core family has been developped by SGS-THOMSON Microelectronics to provide the tools and building blocks to enable the development of highly integrated application-specific 32-bits device at the lowest cost and fastest time to market.

The STi5505 integrates a ST20 C2 core with the following characteristics :

- 50K Dhrystones/s at 50MHz,
- 8/16 bits instructions (32 most common instructions in 8 bits),
- instruction cache 2Kbytes - write back replacement policy,
- internal SRAM 2Kbytes to ensure fast access to critical code, data, interrupt handler ...
- data cache 2 Kbytes - write back replacement policy,

The STi5505's ST20 is provided with advanced debugging tools :

- on-chip real-time emulation,
- debugging with minimal impact on software and performance,
- non intrusive attachment to the host via JTAG (IEEE1149.1),
- no intrusion into the performance of the CPU core,
- no intrusion into user code space by a debug kernel,
- only 40bytes used for breakpoint handler.

I.2 - Video Decoder

The video decoder implemented in the STi5505 uses a patented memory reduction/bandwith reduction scheme to offer the user the best bandwidth/memory size compromise.
The algorithm is lossless and uses "on-the-fly" decoding to reduce the memory requirements to two frame buffers in memory reduction mode.

In this mode, PAL decoding is contained in 12Mbits. When used in bandwith reduction mode, the memory usage is the normal three buffers but the bandwith required by the decoder is significantly reduced compared to a classical implementation.

In summary, the features of the decoder are :

- MPEG-2 Main Profile/Main Level (MP@ML) support,
- MPEG-2 program streams, Packet Elementary streams and MPEG-1 system streams support,
- memory reduction architecture allowing sharing of single 16 Mbits SDRAM between MPEG decoding, micro and transport functions - memory expandable to 32 Mbits of SDRAM,
- letter box (16:9) filter,
- pan-scan, horizontal and vertical image resizing,
- automatic error concealment.

I.3 - Subpicture Decoder

The STi5505 has a hardware DVD compliant subpicture decoder. Subpicture units are copied by DMA into subpicture bit buffer.

The subpicture decoder can decode complete subpicture units without any interaction from the ST20.

The main subpicture decoder features are :

- up to 720x480 or 720x576 subpicture area,
- internal LUTs for Sub Picture, Highlight and PCI (4 bits color and contrast outputs),
- internal color LUT (4 bits from SP, HL, PCI to 24 Y,Cr,Cb bits) for SP color inputs to MPEG, OSD, SP mixer.

I.4 - Audio Decoder

The audio decoder cell is a fully compatible Dolby AC-3™ / MPEG-1/MPEG-2 decoder capable of decoding both 5.1 and 2 channel streams compatible with the DVD standard.

Downmix from 5.1 channels is supported for both Dolby and MPEG-2 streams. The output can be sent directly to external DACs or formatted for transmission in accordance with the IE6958 standard.

The decoder can also handle linear PCM in accordance with the DVD standard. An integrated downsampler is provided for conversion from 96 kHz to 48kHz.

I - GENERAL DESCRIPTION (continued)

The main features of the decoder core are :

- Decodes 5.1 Dolby AC-3 Digital surround,
- Output to 6 channels. Downmix modes : 1, 2, 3 or 4 channels for MPEG and AC-3 streams,
- Karaoke mode for DVD. MPEG-2 capable, AC-3 capable,
- MPEG-1, 2-channel audio decoder layers 1 and 2,
- MPEG-2, 6-channel audio decoder layer 2,
- PCM : transparent. downsampling 96 to 48 kHz,
- Accepts MPEG-2 PES stream format for : MPEG-2, MPEG-1, Dolby AC-3 and Linear PCM,
- IEC6958 Output Interface,
- CD-DA PCM format (subcode output in IEC6958 user data),
- Downmix for Dolby Pro Logic compatible outputs for AC-3 and MPEG-2 (Pro Logic encoder),
- Pro Logic decoder,
- PLL for Internal 44.1 and 48kHz PCM clock generation,
- On chip pink noise generator.

I.5 - High Performance On-Screen Display

The graphics performance of the STi5505 supports the new requirements for intelligent program guides and interactive applications.

The display interface supports up to 256 colors for each OSD region and a transparency feature allows mixing of video with the OSD. Fast access graphics and many other additional features are available and are supported by a graphics library.

Very high system performance is obtained by closely coupling the ST20 RISC processor and cache with the MPEG audio/video core and display memory.

Low latency RISC access and DMA engines allow rapid construction of bit maps.

I.6 - PAL/NTSC Encoder

The STi5505 integrates a PAL/NTSC encoder. It converts the digital MPEG/Sub Picture/OSD stream into a standard analog baseband PAL/NTSC signal and into RGB analog components. Six analog output pins are available on which it is possible to output CVBS, S-VHS (Y/C) and RGB formats.

The encoder handles interlaced and non-interlaced mode.

It can perform Closed Captions, CGMS or Teletext encoding and allows Macrovision 7.01/6.1 copy protection.

The encoder supports both master and slave modes for synchronization.

I.7 - Memory Interfaces

The STi5505 has been designed to minimize system costs by enabling various memory savings. Two kinds of memory interfaces are used on the STi5505 : a programmable External Memory Interface (EMI) and a high performance SDRAM interface.

The External Memory Interface supports several address ranges (memory banks). In each bank, a set of signals are entirely programmable and can be used to map 8/16 bits peripherals such as Front End channel ICs in DVD applications.

The EMI contains a zero glue logic DRAM and a low-cost EPROM interface.

This interface can be programmed to interface very easily peripherals.

The SDRAM memory interface supports gluelessly 125 MHz SDRAMs providing the adequate bandwiths to achieve MPEG decoding and display, OSD drawing and display, and general system use.

Memory savings can be realized on ROM requirements too : the ST20 VL-RISC micro-core has the highest code density of any 32 bit CPU, leading to the lowest cost program ROM.

I.8 - Front-End Interface

The STi5505 's front end interface accepts :

- DVD, VCD and CD-DA sectors,
- DVB-DSS transport stream.

In DVD mode, DVD, VCD and CD-DA information can be input into STi5505 through a serial interface or a generic parallel interface.

In serial mode, data are captured and filtered from I2S and V4 interfaces by an internal sector processor. V4 interface is used to capture VCD and CD-DA subcode information. In parallel mode, sector processor is bypassed.

I - GENERAL DESCRIPTION (continued)

The main features of the DVD interface are :

- DVD, VCD and CD-DA compatible,
- hardware sector filtering,
- subcode error correction for CD-DA,
- integrated CSS decryption,
- integrated track buffer support,
- DMA engine to ST20 memory.

In DVB-DSS mode, DVB-DSS transport stream is input through a serial interface. The STi5505 extracts and descrambles Packet Elementary Streams belonging to one user selected program to be decoded and presented.

The main features of the DVB-DSS interface are :

- descrambling (transport packet and packet elementary streams in DVB mode, transport packet in DSS mode ; up to 32 streams descrambling),
- PID and section filtering,
- clock recovery,
- DMA engine.

In DVB-DSS mode, a high speed digital interface allows to transfer packets between the Set Top Box and external units, either for recording or playback purposes. This interface provides also full support for an external IEEE1394 connection.

I.9 - Integrated Peripherals

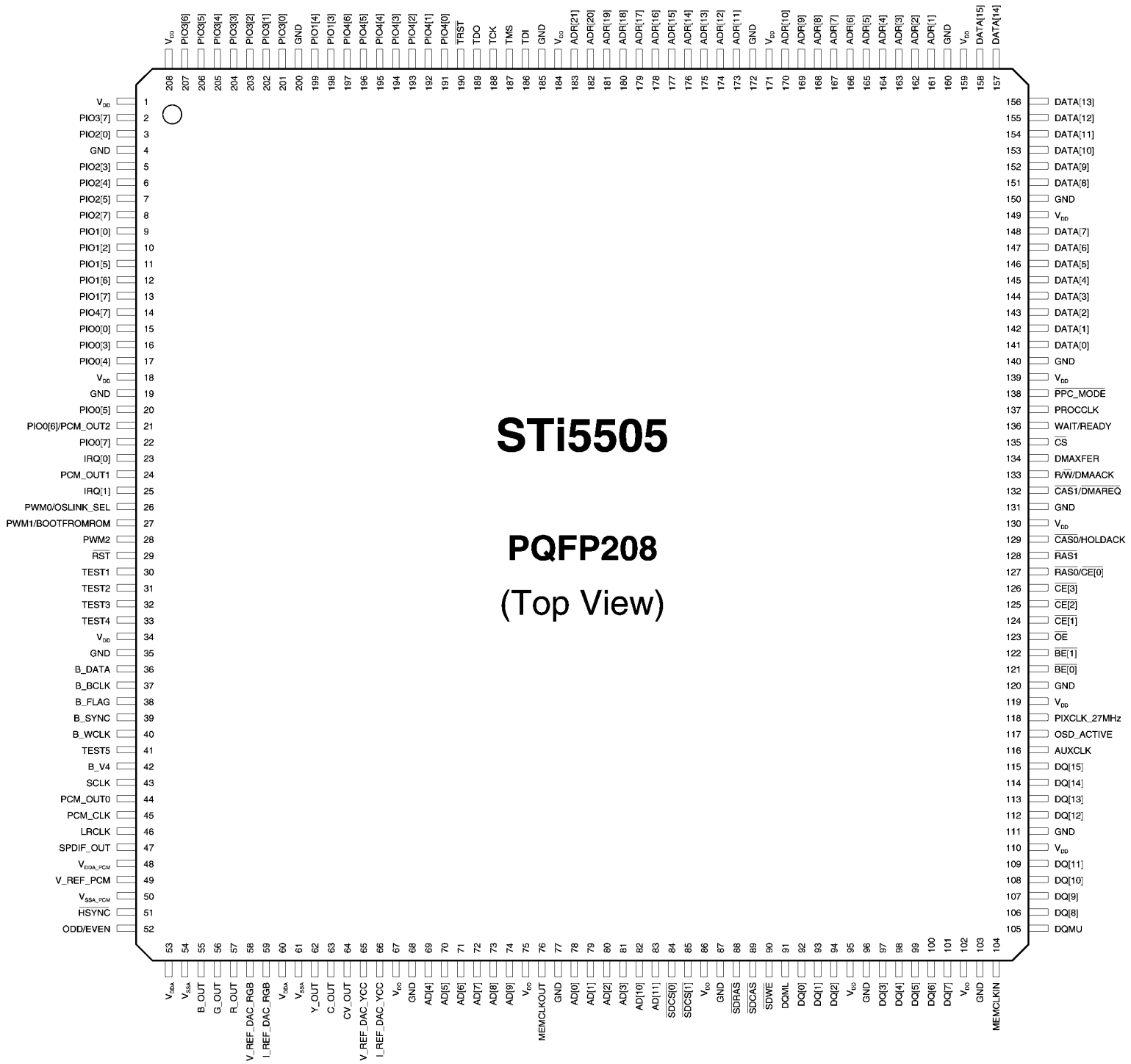
Several peripherals generally used in DVD players or DVD-DVB combos have been integrated into the STi5505.

They are :

- two UARTs to interface remote control receivers, DVD front end, modem ...,
- one I^2C controller to interface serial memories, remote control receivers, microcontrollers...,
- 2 SmartCard interfaces (ISO7816-3) for DVB-DSS conditionnal access, pay per view ...,
- PWM/timer module for control of system clock,
- 34 programmable I/O pins,
- OS Link interface,
- JTAG with boundary scan for debug.

II - PIN DESCRIPTION

II.1 - Pin Connections



II - PIN DESCRIPTION (continued)

II.2 - Pin List

Pin	Name	Type	Function
SUPPLIES			
1, 18, 34, 67, 75, 86, 95, 102, 110, 119, 130, 139, 149, 159, 171, 184, 208	V_{DD}		Power Supply
4, 19, 35, 68, 77, 87, 96, 103, 111, 120, 131, 140, 150, 160, 172, 185, 200	GND		Ground
53, 60	V_{DDA}		Analog Power Supply for DENC D/A Converters
54, 61	V_{SSA}		Analog Ground for DENC D/A Converters
48	V_{DDA_PCM}		Analog Power Supply for PLL PCM
49	V_REF_PCM		Analog Reference for PLL PCM
50	V_{SSA_PCM}		Analog Ground for PLL PCM
FRONT-END INTERFACE			
36	B_DATA	I	I^2S Data (DVD) or PARA_DATA[2] (DVD//) or Link Data (DVB/DSS)
40	B_WCLK	I/O	I^2S Word Clock or PARA_DATA[6] (DVD//) or NRSS_CLK (DVB/DSS)
37	B_BCLK	I	I^2S Bit Clock (DVD) or PARA_DATA[3] (DVD//) or Link Bit Clock (DVB/DSS)
38	B_FLAG	I	Error Flag (DVD) or PARA_DATA [4] (DVD//) or Link Sync (DVB/DSS)
39	B_SYNC	I	Sector / Abs Time Sync (DVD) or PARA_DATA[5] (DVD//) or Link Not Valid (DVB/DSS)
42	B_V4	I	Versatile Input Pin (Subcode Input) or PARA_DATA[7] (DVD//) or NRSS_IN (DVB/DSS)
VIDEO OUTPUT INTERFACE			
57	R_OUT	O	Red Output
56	G_OUT	O	Green Output
55	B_OUT	O	Blue Output
63	C_OUT	O	Chroma Output
64	CV_OUT	O	Composite Video Output
62	Y_OUT	O	Luma Output
59	I_REF_DAC_RGB	I	DAC Current Reference
66	I_REF_DAC_YCC	I	DAC Current Reference
58	V_REF_DAC_RGB	I	DAC Voltage Reference
65	V_REF_DAC_YCC	I	DAC Voltage Reference
117	OSD_ACTIVE	I/O	OSD Active
118	PIXCLK_27MHz	I	System Clock Input
51	$\overline{\text{HSYNC}}$	I/O	Horizontal Sync
52	ODD/EVEN	I/O	Vertical Sync
AC-3/MPEG1-2 AUDIO OUTPUT INTERFACE			
43	SCLK	O	Serial Bit Clock
44	PCM_OUT0	O	Audio Serial Output Data 0
24	PCM_OUT1	O	Audio Serial Output Data 1
21	PCM_OUT2	O	Audio Serial Output Data 2
45	PCM_CLK	I/O	PCM Clock In or Out
46	LRCLK	O	Left/Right Clock
47	SPDIF_OUT	O	SPDIF Output

II - PIN DESCRIPTION (continued)

II.2 - Pin List (continued)

Pin	Name	Type	Function
EXTERNAL INTERRUPTS			
23, 25	IRQ[0:1]	I	External Interrupts
PROGRAMMABLE I/O AND ALTERNATE FUNCTION (see Device Configuration Chapter)			
15	PIO0 [0]	I/O	General Purpose I/O or PARA_SYNC (DVD//Front End) or Sc1Data (Smart Card 1 Data I/O)
16	PIO0 [3]	I/O	General Purpose I/O or PARA_REQ (DVD//Front End) or Sc1Clk (Smart Card 1 Clock)
17	PIO0 [4]	I/O	General Purpose I/O or PARA_STR (DVD//Front End) or Sc1RST (Smart Card 1 Reset)
20	PIO0 [5]	I/O	General Purpose I/O or PARA_DATA[0] (DVD//Front End) or Sc1Cmd V_{CC} (Smart Card 1 Voltage Enable)
21	PIO0 [6]	I/O	General Purpose IO or Sc1DataDir (Smart Card 1 Dir)
22	PIO0 [7]	I/O	General Purpose I/O or PARA_DATA[1] (DVD//Front End) or Sc1Detect(Smart Card 1 Detect)
9	PIO1 [0]	I/O	General Purpose I/O or I^2C Data
10	PIO1 [2]	I/O	General Purpose I/O or I^2C Clock
198, 199	PIO1 [3:4]	I/O	General Purpose IO
11	PIO1 [5]	I/O	General Purpose IO or ASC1 TXD
12	PIO1 [6]	I/O	General Purpose IO or ASC1 RXD
13	PIO1 [7]	I/O	General Purpose IO or ASC3 TXD
3	PIO2 [0]	I/O	General Purpose I/O or Sc0Data (Smart Card 0 Data I/O)
5	PIO2 [3]	I/O	General Purpose I/O or Sc0Clk (Smart Card 0 Clock)
6	PIO2 [4]	I/O	General Purpose I/O or Sc0RST (Smart Card 0 Reset)
7	PIO2 [5]	I/O	General Purpose I/O or Sc0CmdV_{CC} (Smart Card 0 Voltage Enable)
8	PIO2 [7]	I/O	General Purpose I/O or Sc0Detect (Smart Card 0 Detect)
201	PIO3 [0]	I/O	General Purpose IO or OSLink In
202	PIO3 [1]	I/O	General Purpose IO or OSLink Out
203	PIO3 [2]	I/O	General Purpose IO or CPUReset
204	PIO3 [3]	I/O	General Purpose IO or CPU Analyse
205	PIO3 [4]	I/O	General Purpose IO or ErrorOut
206, 207, 2	PIO3 [5:7]	I/O	General Purpose IO
191-197	PIO4 [0:6]	I/O	General Purpose IO
14	PIO4 [7]	I/O	General Purpose IO or ASC3 RXD
JTAG INTERFACE			
188	TCK	I	Test Clock
186	TDI	I	Test Data Input
189	TDO	O	Test Data Input
187	TMS	I	Test Mode Select
190	$\overline{\text{TRST}}$	I	Test Reset
SYSTEM USE			
28	PWM2	O	PWM2 Output
27	PWM1/BOOTFROMROM	O/I	PWM1 Output or Configuration Oslink Pins
26	PWM0/OSLINK_SEL	O/I	PWM0 Output or Boot from ROM during Reset
29	$\overline{\text{RST}}$	I	Reset
116	AUXCLK	O	Auxilary Clock for Any Purpose

II - PIN DESCRIPTION (continued)

II.2 - Pin List (continued)

Pin	Name	Type	Function
SDRAM INTERFACE			
78-81, 69, 70-74, 82, 83	AD[0:11]	O	SDRAM Address Bus
92-94, 97-101, 106-109, 112-115	DQ[0:15]	I/O	SDRAM Data (Lower Byte)
84, 85	$\overline{\text{SDCS}}$[0:1]	O	SDRAM Chip Selects
89	$\overline{\text{SDCAS}}$	O	SDRAM CAS
88	$\overline{\text{SDRAS}}$	O	SDRAM RAS
90	$\overline{\text{SDWE}}$	O	SDRAM Write Enable
104	MEMCLKIN	I	SDRAM Memory Clock Input
76	MEMCLKOUT	O	SDRAM Memory Clock Output
91	DQML	O	DQ Mask Enable (Lower)
105	DQMU	O	DQ Mask Enable (Upper)
EXTERNAL MEMORY INTERFACE			
161-170, 173-183	ADR[1:21]	I/O	External Memory Address Bus
141-148, 151-158	DATA[0:15]	I/O	External Memory Data Bus
128	$\overline{\text{RAS1}}$/HOLDREQ	O	DRAM RAS or reserved
136	WAIT/READY	I/O	External Wait States or Reserved
133	R/$\overline{\text{W}}$/DMAACK	I/O	DRAM R/$\overline{\text{W}}$ Strobe or Reserved
121, 122	$\overline{\text{BE}}$[0:1]	O	Byte enable
129	$\overline{\text{CAS0}}$/HOLDACK	O/I	DRAM CAS or Reserved
132	$\overline{\text{CAS1}}$/DMAREQ	O	DRAM CAS or Reserved
124-126	$\overline{\text{CE}}$[1:3]	O	Chip Select for Banks 1 - 3
135	$\overline{\text{CS}}$	I	Reserved
137	PROCCLK	I/O	ST20 Clock or Reserved
127	$\overline{\text{RAS0}}$/$\overline{\text{CE0}}$	O	DRAM RAS or Chip Select for Bank 0
134	DMAXFER	I	Reserved
138	$\overline{\text{PPC\_MODE}}$	I	Reserved
123	$\overline{\text{OE}}$	I/O	Output Enable or Reserved
SDAV/P1394 INTERFACE			
30	TEST1	I/O	DATA_RX/STROBE_TX (SDAV Mode) or SDAV_CLK (P1394 Mode)
31	TEST2	I/O	STROBE_RX/DATA_TX (SDAV Mode) or DATA_IN/DATA_OUT (P1394 Mode)
32	TEST3	I/O	Direction (SDAV Mode) or DATA_VALID In/Out (P1394 Mode)
MISCELLANEOUS			
41	TEST5	O	NRSS_OUT (DVB/DSS)

III - FUNCTIONAL DESCRIPTION

III.1 - Functional Modules

Figure 1 shows the subsystem modules that make up the STi5505. These modules are outlined below.

III.1 - CPU

The Central Processing Unit (CPU) on the STi5505 is the ST20-C2 32-bit processor core. It contains instruction processing logic, instruction and data pointers and an operand register. It directly accesses the high speed on-chip SRAM memory, which can store data or programs, and uses the Caches to reduce access time to off chip program and data memory.

The processor can access memory via the general purpose External Memory Interface (EMI) or via the SDRAM EMI which is shared with the MPEG decoder.

III.2 - Memory Subsystem

The STi5505 on-chip SRAM memory system provides 160 Mbytes/s internal data bandwidth, supporting pipelined 2 cycles internal memory access at 25ns cycle times. The STi5505 memory system consists of 2 Kbytes of SRAM, 2Kbytes of instruction cache, a 2Kbytes data cache that can be programmed to be SRAM, and an external memory interface (EMI).

The STi5505 product has 2 Kbytes of on-chip SRAM. The advantage of this is the ability to store time critical code on chip, for instance interrupt routines, software kernels or device drivers, and even frequently used data without these being flushed from the caches.

The instruction and data caches are direct mapped with a write-back system for the data cache and support burst accesses to the external memories for refill and write-back which are effective for increasing performance with page-mode and SDRAM memories.

The STi5505 EMI controls access to the external memory and peripherals while the SDRAM EMI provides access to the SDRAM buffer for the MPEG decoders, ST20 and DMA peripherals.

The STi5505 EMI can access a 16 Mbytes (or greater if DRAM is used) physical address space in each of the four general purpose memory banks, and provides sustained transfer rates of up to 80 Mbytes/s. Peripherals that support an asynchronous data acknowledge are supported as is an external Power PC which can share the bus with the STi5505 and access the SDRAM buffer through the device.

High memory bandwidths up to 200 Mbytes/s can be supported by the SDRAM EMI.

The STi5505 internal memory interconnect provides buffering and arbitration of memory access requests to sustain very high throughput of memory accesses.

III.3 - Syste m Services Module

The STi5505 system services module includes :

- Phase locked loop (PLL) - accepts 27MHz input and generates all the internal high frequency clocks needed for the CPU and the OS-Link.
- test access port - JTAG compatible.
- Diagnostics controller accessed via the JTAG port providing :
- Bootstrapping during development
- Hardware breakpoint and watchpoint
- Real time trace
- External LSA triggering support.

III.4 - Serial Communications

To facilitate the connection of this system the front end device and other peripherals, two UARTs (ASCs) are included in the device. The UARTs provide an asynchronous serial interface.

The UART can be programmed to support a range of baud rates and data formats, for example, data size, stop bits and parity. Two synchronous serial communications (SSC) interfaces are provided on the device. These can be used for a remote control device for example via an I^2C or SPI bus.

III.5 - Interrupt Subsystem

The STi5505 interrupt subsystem supports eight prioritized interrupt levels. Two external interrupt pins are provided. Level assignment logic allows any of the internal or external interrupts to be assigned and, if necessary, share any interrupt level.

III.6 - Front End Interf ace & DVD Decryption

The front end interface accepts sectors in the case of DVD, MPEG-1 system stream in the case of VCD and PCM data for CD-DA applications on an I2S interface. In the case of VCD and CD-DA disks the subcode information is input via a simple asynchronous serial interface similar to a UART.

The bitstream and subcode stream then pass through a "sector processor" block which handles sector filtering in the case of DVD and sectorizing using the subcode stream for VCD and CD-DA systems.

III - FUNCTIONAL DESCRIPTION (continued)

The block also handles overspeed processing for all systems. The capturing of CD-DA sectors is based on a flywheel tiner to improve robusters by concealing erros in the subcode stream. For DVD the data, having had sector headers removed, then passes through a DVD conformant de-cryption stage and is written into any of the system memories using a programmable DMA engine. When a subcode stream is present it is locally buffered, by subcode block and can be read by the CPU for subsequent processing, if required.

III.7 - PWM and counter module

This unit includes three separate pulse width modulator (PWM) generators using a shared counter, and three timer compare and capture channels sharing a second counter.

The counters can be clocked from a pre-scaled internal clock or from a pre-scaled external clock via the capture clock input and the event on which the timer value is captured is also programmable.

The PWM counters are 8-bit with 8-bit registers to set the output high time. The capture/compare counter and the compare and capture registers are 32-bit.

III.8 - Parallel Programmable IO module

40 bits of parallel I/O are provided. 34 of then are connected to actual PIO pins. Each bit is programmable as an output or an input. The output can be configured as a totem pole or open drain driver. Input compare logic is provided which can generate an interrupt on any change on any input bit.

Many pins of the STi5505 device are multi-function and can either be configured as PIO or connected to an internal peripheral signal.

III.9 - MPEG Video decoder

The video decoder is a real-time video compression processor supporting the MPEG-1 and MPEG-2 standards at video rates up to 720 x 480 x 60 Hz and 720 x 576 x 50 Hz. Picture format conversion for display is performed by vertical and horizontal filters. User-defined bitmaps may be superimposed on the display picture through use of the on-screen display function.

III.10 - PAL/NTSC encoder

The digital encoder which is integrated in the STi5505 converts a multiplexed 4:2:2 YUV stream into a standard analog baseband PAL/NTSC signal and into RGB analog components. The encoder can also perform closed-caption, CGMS or teletext encoding and allows Macrovision™ 7.01/6.1 copy protection.

III.11 - MPEG-2 Audio / Dolby AC-3 Decoder

The audio decoder is a Dolby AC-3 decoder capable of decoding both 5.1 and 2 channel DVD comformant bitstreams. The decoder also handles MPEG-1 (layers 1 & 2) and MPEG-2 layer 2 (6 channels). Downmix to 2 channels is possible for Dolby and MPEG standards with optional pro-logic encoding.

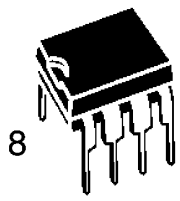
The decoder directly accepts MPEG-2 PES streams as input. The decoder is capable of supporting IEC6958-IEC61937 formatted outputs for AC-3 and MPEG audio, linear PCM (left & right,16, 18, 20 & 24 bits), zero output (Mute mode) and PCM audio.

ST24E32
ST25E32

32K SERIAL I²C EEPROM with EXTENDED ADDRESSING

NOT FOR NEW DESIGN

- COMPATIBLE with I²C EXTENDED ADDRESSING
- TWO WIRE SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- 1 MILLION ERASE/WRITE CYCLES, OVER the FULL SUPPLY VOLTAGE RANGE
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - ± 4.5V to 5.5V for ST24E32 version
  - ± 2.5V to 5.5V for ST25E32 version
- WRITE CONTROL FEATURE
- BYTE and PAGE WRITE (up to 32 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES
- ***ST24E32 and ST25E32 are replaced by the M24C32***



PSDIP8 (B)
0.25mm Frame

SO8 (M)
200mil Width

DESCRIPTION

The ST24/25E32 are 32K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 512 x 8 bits. The ST25E32 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

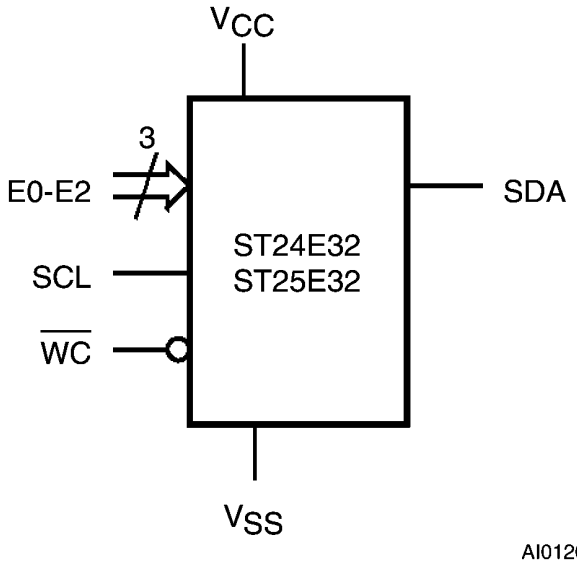


Figure 2A. DIP Pin Connections

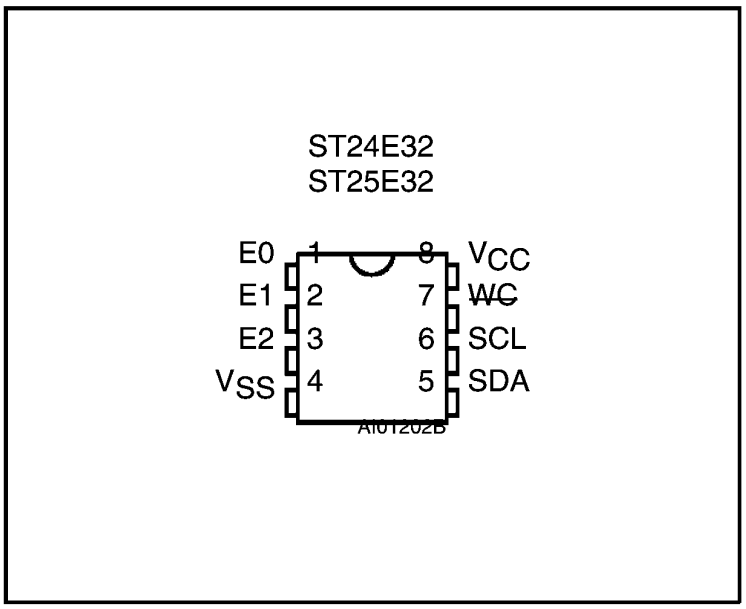


Figure 2B. SO Pin Connections

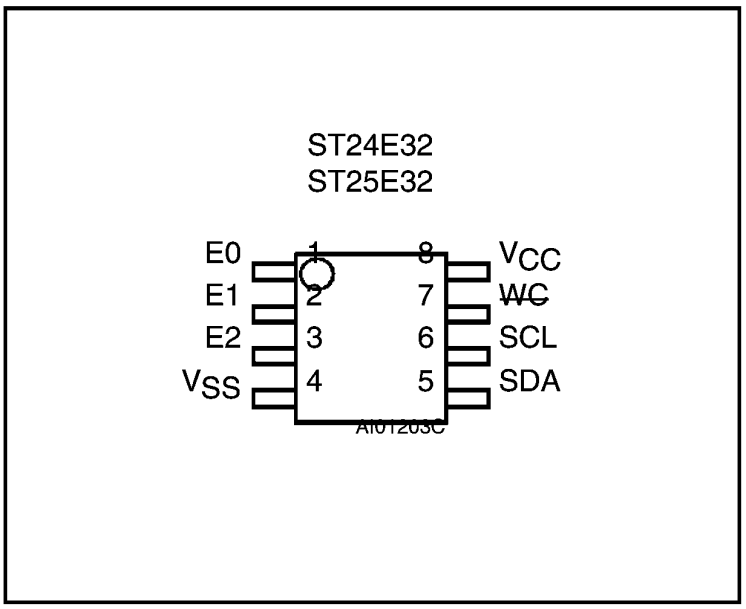


Table 2. Absolute Maximum Ratings (1)

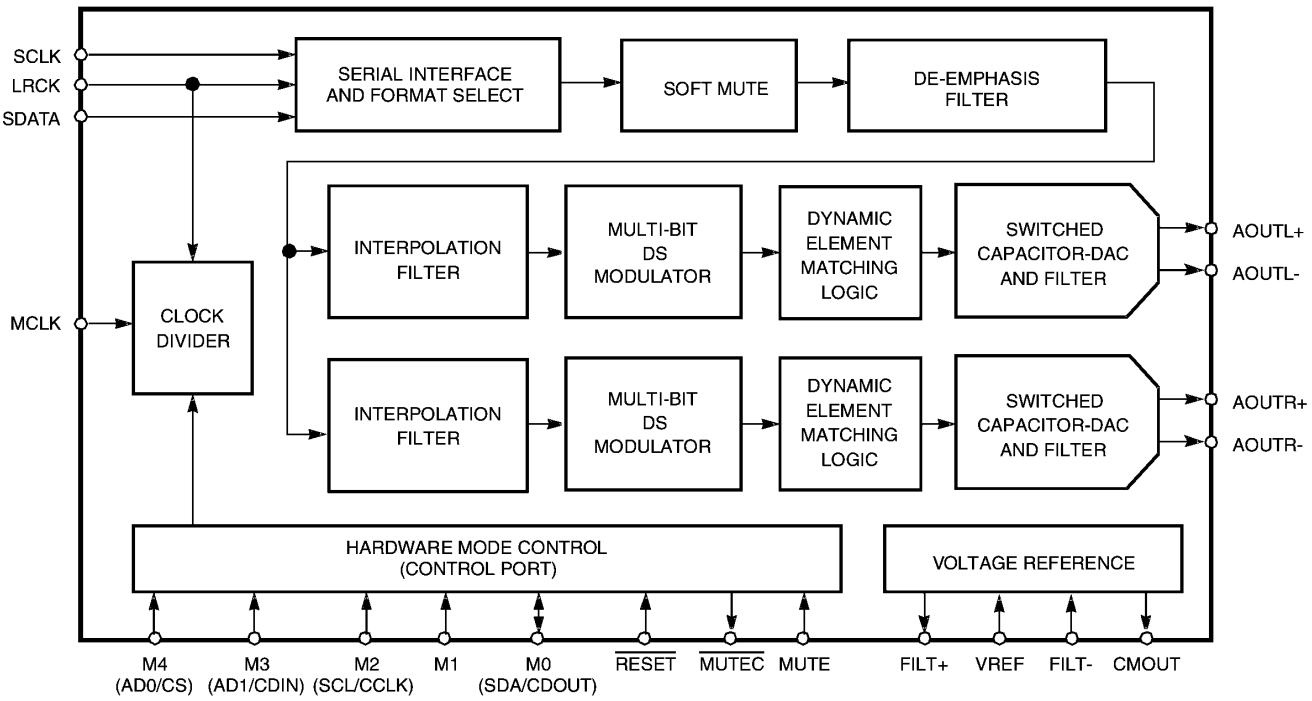
Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			±40 to 125	°C
T_{STG}	Storage Temperature			±65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			±0.6 to 6.5	V
V_{CC}	Supply Voltage			±0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

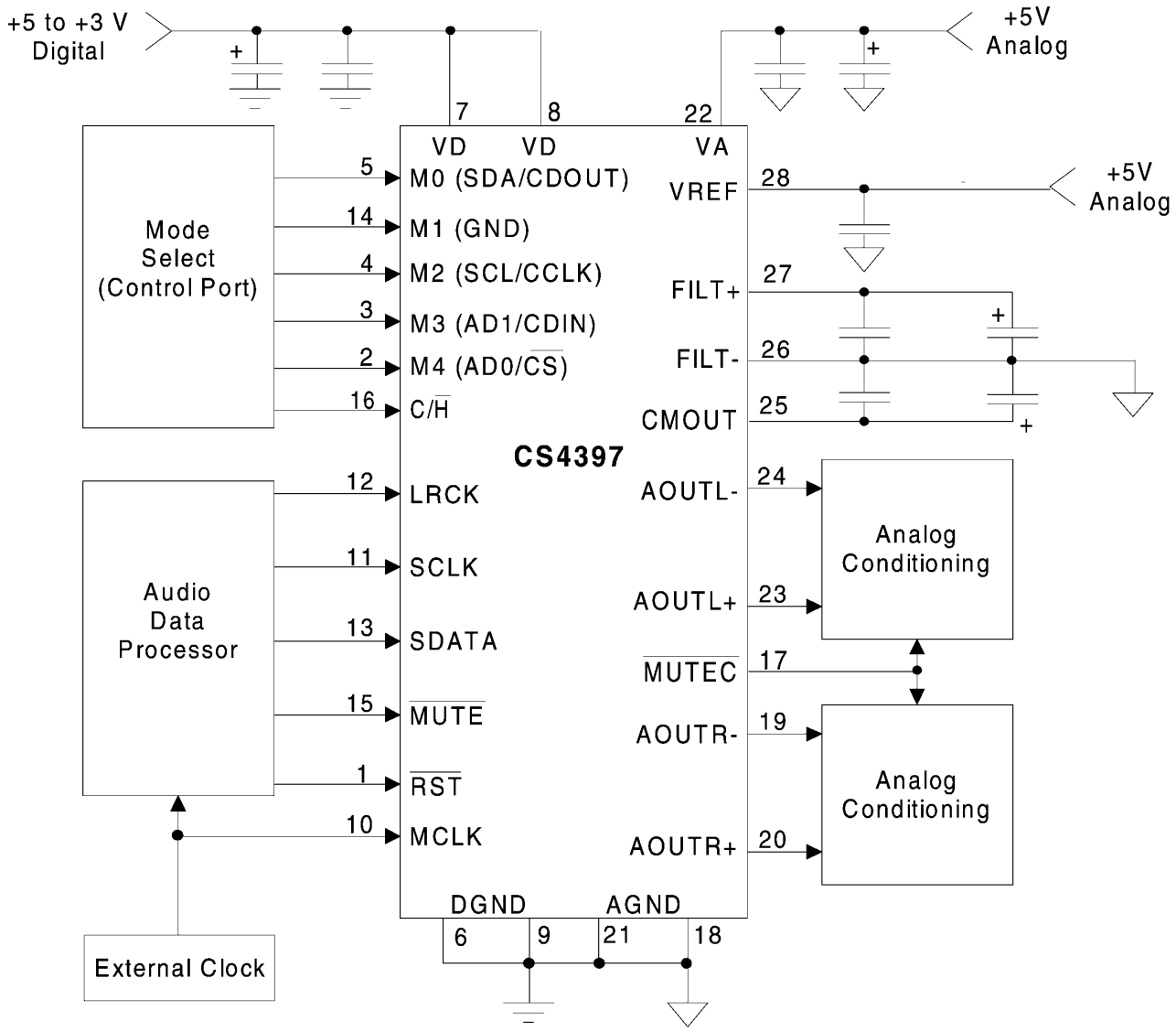
DESCRIPTION (cont'd)

Each memory is compatible with the I^2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The ST24/25E32 carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The ST24/25E32 behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/write bit and terminated by an acknowledge bit.

Block Diagram



Pin Configuration



Typical Connection Diagram - Hardware Mode (Control Port Mode)

CL 06532152_099.eps
131200

Pin Function

No.	Pin Name	I/O	Description
1	RST	I	Reset input (Low active)
2	M4(AD0/CS)	I	Chip address bit0 for I2C
3	M3(AD1/CDIN)	I	Chip address bit1 for I2C
4	M2(SCL/CCLK))	I	Serial clock for I2C
5	M0(SDA/CDOUT)	I/O	Serial data for I2C
6	DGND		Digital ground
7	VD		Digital power supply +3.3V
8	VD		Digital power supply +3.3V
9	DGND		Digital ground
10	MCLK	I	Master clock PCM mode:256Fs DSD mode:192Fs (8.4672MHz)
11	SCLK	I	Serial data clock
12	LRCK(PCM) CLKMODE(DSD)	I I	PCM mode:Left/Right channel clock DSD mode:Select MCLK to DSD data rate clock rations
13	SDATA(PCM) DSD_L(DSD)	I	PCM mode:Serial audio data DSD mode:Direct Stream Digital audio data (Left)
14	M1(PCM) DSD_R(DSD)	I	PCM mode:(Low) DSD mode:Direct Stream Digital audio data (Right)
15	MUTE	I	Mute input (Low active)
16	C/H	I	Control port (H) /Hardware (L) mode select
17	MUTEC	O	Mute control (Low active)
18	AGND		Analog ground
19	AOUTR-	O	Right channel negative Analog out
20	AOUTR+	O	Right channel positive Analog out
21	AND		Analog ground
22	VA		Analog power supply +5.5V
23	AOUTL+	O	Left channel positive Analog out
24	AOUTL-	O	Left channel negative Analog out
25	CMOUT	O	Common mode voltage
26	FILT-	I	Reference ground
27	FILT+	O	Reference filter
28	VREF		Voltage reference input

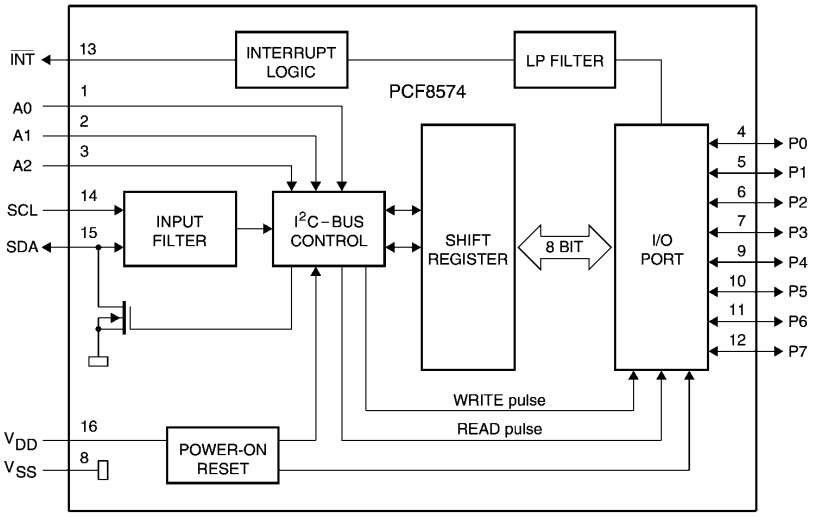
CL 06532152_100.eps
131200

9.6.1 Description of I²C Controller PC8574

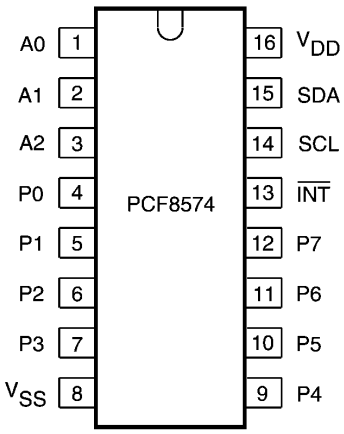
Block Diagram

PC8574

Block Diagram



Pin Configuration



Pin Function

SYMBOL	PIN		DESCRIPTION
	DIP16; SO16	SSOP20	
A0	1	6	address input 0
A1	2	7	address input 1
A2	3	9	address input 2
P0	4	10	quasi-bidirectional I/O 0
P1	5	11	quasi-bidirectional I/O 1
P2	6	12	quasi-bidirectional I/O 2
P3	7	14	quasi-bidirectional I/O 3
V_{SS}	8	15	supply ground
P4	9	16	quasi-bidirectional I/O 4
P5	10	17	quasi-bidirectional I/O 5
P6	11	19	quasi-bidirectional I/O 6
P7	12	20	quasi-bidirectional I/O 7
$\overline{INT}$	13	1	interrupt output (active LOW)
SCL	14	2	serial clock line
SDA	15	4	serial data line
V_{DD}	16	5	supply voltage
n.c.	-	3	not connected
n.c.	-	8	not connected
n.c.	-	13	not connected
n.c.	-	18	not connected

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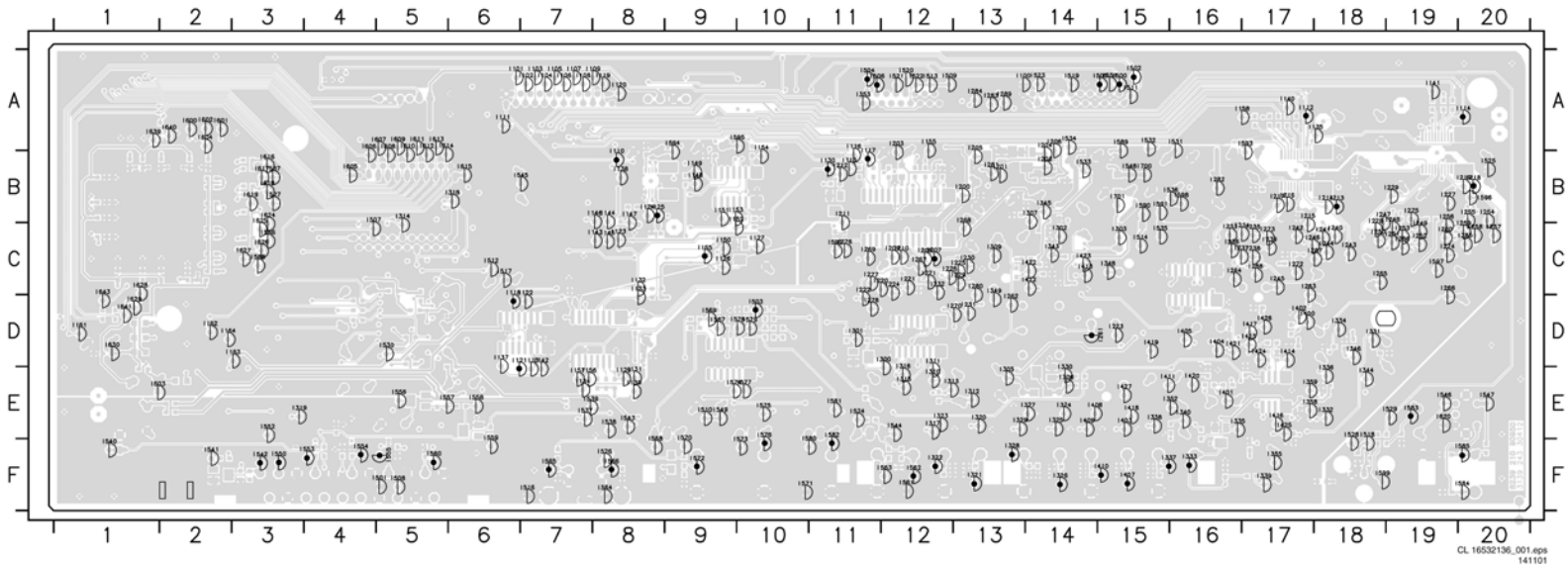
131200

9.7 Abbreviation list

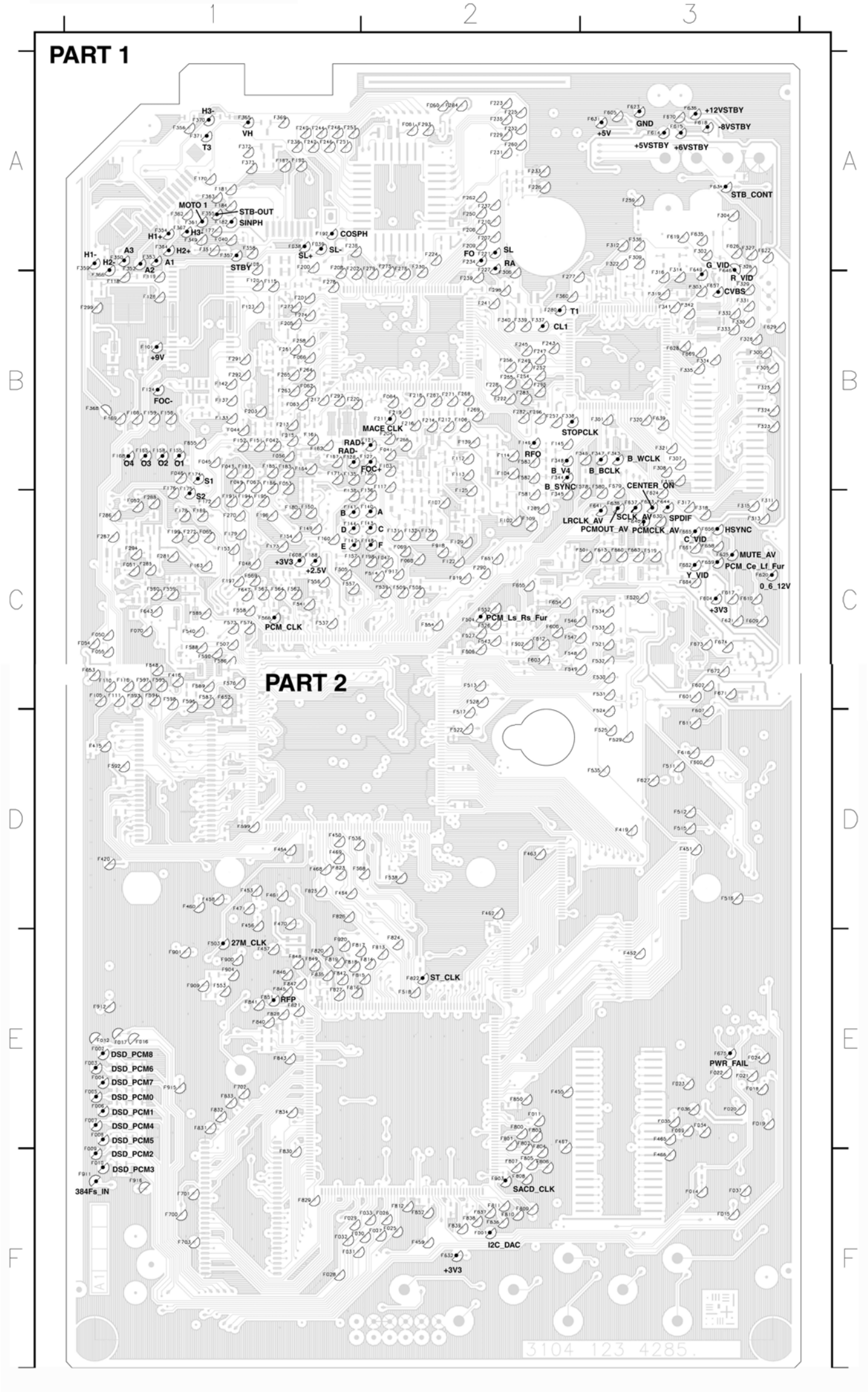
ADC	Analogue to Digital Converter
AM	Amplitude Modulation
AP	Asia Pacific
AV	External Audio Video
BE	Basic Engine
B/G	Monochrome TV system. Sound carrier distance is 5.5 MHz
BTSC	Broadcast Television Standard Committee. Multiplex FM stereo sound system, originating from the USA and used e.g. in LATAM and AP-NTSC countries
ComPair	Computer aided rePair
CC	Closed Caption
CD-DA	CD Digital Audio
CS	Chip Select
CVBS	Composite Video Blanking and Synchronisation
DAC	Digital to Analogue Converter
DAIO	Digital Audio Input Output
DENC	Digital Encoder
D/K	Monochrome TV system. Sound carrier distance is 6.5 MHz
DFU	Direction For Use: description for the end user
DNR	Dynamic Noise Reduction
DRAM	Dynamic RAM
DSD	Direct Stream Digital
DSP	Digital Signal Processing
DTS	Digital Theatre Sound
DVD	Digital Versatile Disc
EEPROM	Electrically Erasable and Programmable Read Only Memory
EFM	Eight to Fourteen bit Modulation
EMI	External Memory Interface (STi5505)
EU	Europe
EXT	External (source), entering the set via SCART or Cinch
FLASH	Flash memory
FM	Frequency Modulation
HP	Headphone
HPF	High Pass Filter
HW	Hardware
I	Monochrome TV system. Sound carrier distance is 6.0 MHz
I^2C	Integrated IC bus
I2S	Integrated IC Sound bus
IF	Intermediate Frequency
Interlaced	Scan mode where two fields are used to form one frame. Each field contains half the number of the total amount of lines. The fields are written in 'pairs', causing line flicker.
IR	Infra Red
IRQ	Interrupt Request
LATAM	Latin America
LED	Light Emitting Diode
L/L'	Monochrome TV system. Sound carrier distance is 6.5 MHz. L' is Band I, L is all bands except for Band I
LLD	Loss Less Decoder
LPCM	Linear Pulse Code Modulation
LPF	Low Pass Filter
LRCLK	Left/Right clock
LS	Loudspeaker
M/N	Monochrome TV system. Sound carrier distance is 4.5 MHz
MACE	Mini All Compact Disc Engine
MPEG	Motion Pictures Experts Group
NC	Not Connected
NICAM	Near Instantaneous Compounded Audio Multiplexing. This is a digital sound system, mainly used in Europe.
NTSC	National Television Standard Committee. Colour system mainly used in North America and Japan. Colour carrier NTSC M/N = 3.579545 MHz, NTSC 4.43 = 4.433619 MHz (this is a VCR norm, it is not transmitted off-air)
NVM	Non Volatile Memory: IC containing TV related data e.g. alignments
OC	Open Circuit
OPU	Optical Pick up Unit
OSD	On Screen Display
P50	Project 50 or Easy Link
PAL	Phase Alternating Line. Colour system mainly used in West Europe (colour carrier = 4.433619 MHz) and South America (colour carrier PAL M = 3.575612 MHz and PAL N = 3.582056 MHz)
PCB	Printed Circuit Board (see PWB)
PCM	Pulse Code Modulation
PCM_CLK	Audio system clock for DAC
PCM_OUTx	Audio serial output data
PDM	Physical Disc Mark
PLL	Phase Locked Loop. Used for e.g. FST tuning systems. The customer can give directly the desired frequency
Progressive Scan	Scan mode where all scan lines are displayed in one frame at the same time, creating a double vertical resolution.
PSP	Pit Signal Processing
PWB	Printed Wiring Board (see PCB)
RAM	Random Access Memory
RC	Remote Control handset
RC5	Remote Control system 5, signal from the remote control receiver
RGB	Red Green Blue
ROM	Read Only Memory
S2B	Serial to Basic Engine, communication bus between host- and servo processor
SACD	Super Audio Compact Disc
SCART	Syndicat des Constructeurs d'Appareils Radiorecepteurs et Televisieurs
SCL	Serial Clock I^2C
SCLK	Audio serial bit clock
SDA	Serial Data I^2C
SDRAM	Synchronous DRAM
SECAM	SEequence Couleur Avec Memoire. Colour system mainly used in France and East Europe. Colour carriers = 4.406250 MHz and 4.250000 MHz
S/PDIF	Sony Philips Digital InterFace
SRAM	Static RAM
STBY	Standby
SVHS	Super Video Home System
SW	Software
THD	Total Harmonic Distortion
TXT	Teletext
uP	Microprocessor
VCD	Video CD
VCR	Video Cassette Recorder
Y/C	Luminance (Y) and Chrominance (C) signal
YUV	Component video
0/6/12	SCART switch control signal on A/V board. 0 = loop through (AUX to TV), 6 = play 16:9 format, 12 = play 4:3 forma

AV CBA (COPPER SIDE) TEST POINT OVERVIEW

I100 A13	I134 E7	I204 A14	I237 C16	I270 D13	I315 E12	I353 A11	I502 A15	I536 B16	I569 D9	I602 A2
I101 A6	I135 A18	I205 A13	I238 C17	I271 C12	I316 D12	I355 F17	I503 D10	I537 E7	I570 E9	I603 E1
I102 A7	I137 D6	I206 A14	I239 C17	I272 C17	I317 E12	I358 E17	I504 A11	I538 E8	I571 F10	I604 A2
I103 A7	I138 B8	I207 C12	I240 C18	I273 C17	I318 B6	I359 E17	I505 A15	I539 E7	I572 F9	I605 B4
I104 A7	I139 E8	I208 C12	I241 C18	I274 C19	I319 E3	I400 D17	I506 A11	I540 F1	I573 F10	I606 A4
I105 A7	I140 A17	I209 C12	I242 C17	I275 B19	I320 E13	I401 E16	I507 B4	I541 F2	I574 E9	I607 A5
I106 A7	I141 A19	I210 C12	I243 C18	I276 C11	I321 F13	I402 D17	I508 F5	I542 F3	I575 E10	I608 A5
I107 A7	I142 D7	I211 B11	I244 C18	I277 C11	I322 F12	I403 E15	I509 A12	I543 E8	I576 E10	I609 A5
I108 A7	I143 C8	I212 B11	I245 C17	I278 D11	I323 E12	I404 D16	I510 E9	I544 E12	I577 E10	I610 A5
I109 A8	I144 B8	I213 B18	I246 C17	I279 C13	I324 E14	I405 D16	I511 A15	I545 B7	I578 D10	I611 A5
I110 B8	I145 C8	I214 B18	I247 B18	I280 C13	I325 E14	I407 F15	I512 C6	I546 E19	I579 D10	I612 A5
I111 A6	I146 B8	I215 B17	I248 B19	I281 B13	I326 F14	I408 E14	I513 A12	I547 E20	I580 E10	I613 A5
I112 A17	I147 B8	I216 B17	I249 C19	I282 B16	I327 E14	I409 E14	I514 C15	I548 B15	I581 E11	I614 A5
I113 D7	I148 B9	I217 B17	I250 C18	I283 A13	I328 F13	I410 F15	I516 F7	I549 E9	I582 E11	I615 B6
I114 A20	I149 B9	I218 B20	I251 C19	I284 A13	I329 E13	I411 E15	I517 C6	I550 F3	I583 E19	I616 B3
I115 B11	I150 C9	I219 B20	I252 C19	I285 C20	I330 E14	I412 C14	I518 E18	I551 A15	I584 F20	I617 B3
I116 A11	I151 B9	I220 C11	I253 C19	I286 C19	I331 D18	I413 C14	I519 A14	I552 E3	I585 F20	I618 B3
I117 A11	I152 B9	I221 C12	I254 B20	I287 C18	I332 E18	I414 D17	I520 A12	I553 F4	I586 C3	I619 B3
I118 C6	I153 B9	I222 C11	I255 B20	I288 C17	I333 F16	I415 D17	I521 A12	I554 F4	I587 B3	I620 E19
I119 A8	I154 A10	I223 D15	I256 B19	I289 A13	I334 D18	I416 E17	I522 A12	I555 F5	I588 C3	I624 B3
I120 A8	I155 A12	I224 C12	I257 C20	I300 D12	I335 E16	I417 D17	I523 A14	I556 E5	I589 A15	I625 B3
I121 D6	I156 E7	I225 C13	I258 C20	I301 D11	I336 E18	I418 E15	I524 E11	I557 E5	I590 B15	I626 C3
I122 C7	I157 E7	I226 C12	I259 C20	I302 C14	I337 F15	I419 D15	I525 B20	I558 E6	I591 B15	I627 C3
I123 C8	I158 A17	I227 B19	I260 C19	I303 C15	I338 E15	I420 E16	I526 F8	I559 E6	I592 C11	I628 C1
I124 B8	I161 D1	I228 B18	I261 D14	I305 E13	I339 F17	I421 D16	I527 B3	I560 F5	I593 A17	I629 D1
I125 B8	I162 D2	I229 B19	I262 D13	I306 E14	I340 E16	I422 C14	I528 E18	I561 F12	I594 A9	I630 D1
I126 C9	I163 D3	I230 C13	I263 C17	I307 B14	I343 C14	I423 C14	I529 E19	I562 F12	I595 A10	I639 A1
I127 C10	I164 D2	I231 D13	I264 C16	I309 C13	I344 E18	I424 D17	I530 D5	I563 F12	I596 B20	I640 A2
I129 E8	I165 C9	I232 C12	I265 C18	I310 E12	I345 B14	I425 E17	I531 A16	I564 F8	I597 C19	I641 D1
I130 B11	I200 B13	I233 C16	I266 C19	I311 D12	I346 D18	I426 D17	I532 A15	I565 F7	I598 B16	I643 C1
I131 E8	I201 B13	I234 C17	I267 C12	I312 E13	I348 C15	I427 E15	I533 B14	I566 F8	I599 F18	I700 B15
I132 C8	I202 B14	I235 C17	I268 B13	I313 E12	I349 C13	I500 A15	I534 A14	I567 D9	I600 A2	I701 B15
I133 C8	I203 A12	I236 C16	I269 C11	I314 B5	I352 E16	I501 F5	I535 C15	I568 E8	I601 A2	



MONOBOARD CBA (COPPER SIDE) TEST POINT OVERVIEW



PHILIPS

DVD962SA / SACD900
DVD / SUPER AUDIO CD PLAYER

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051101

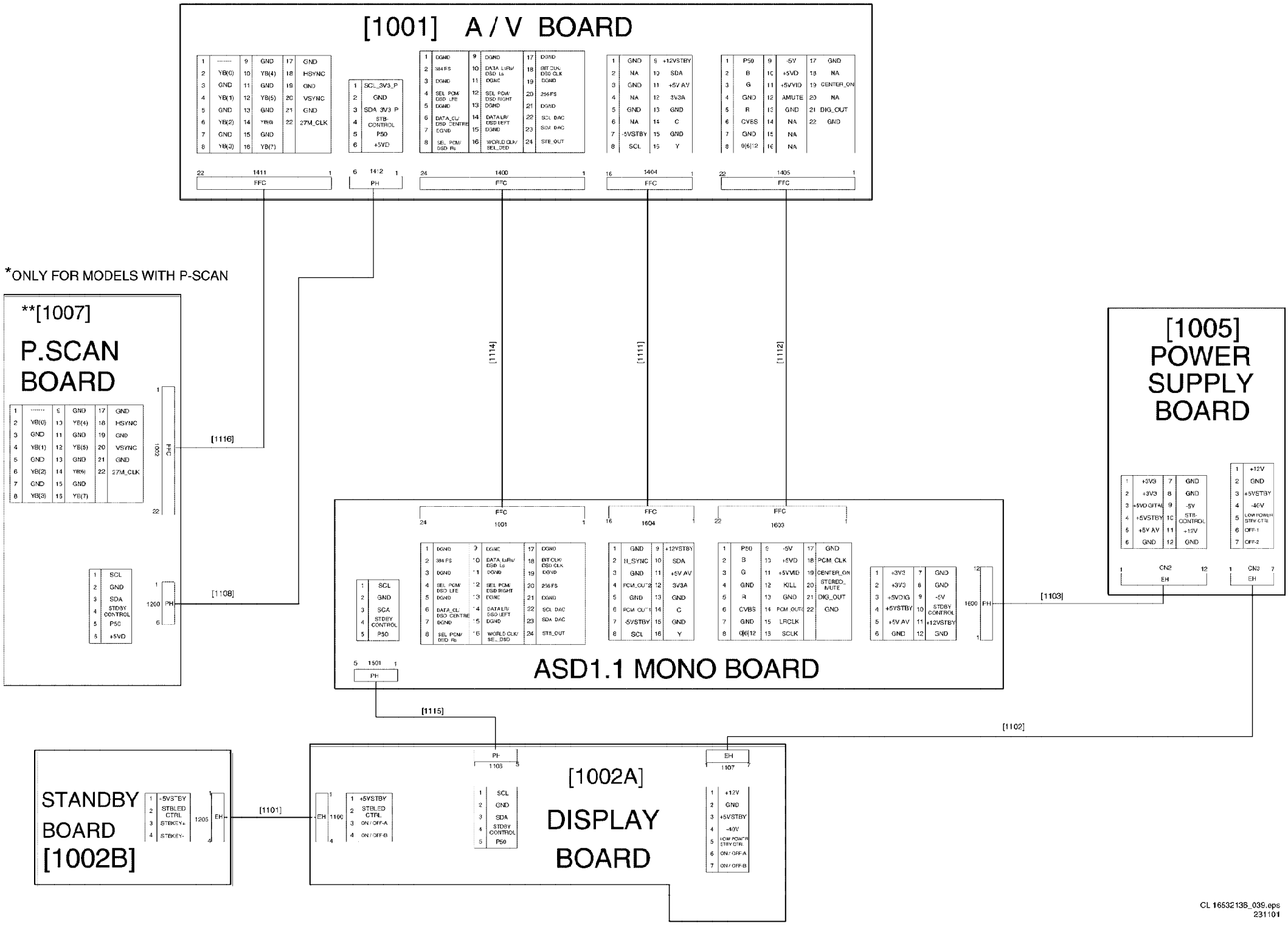
CLASS 1
LASER PRODUCT

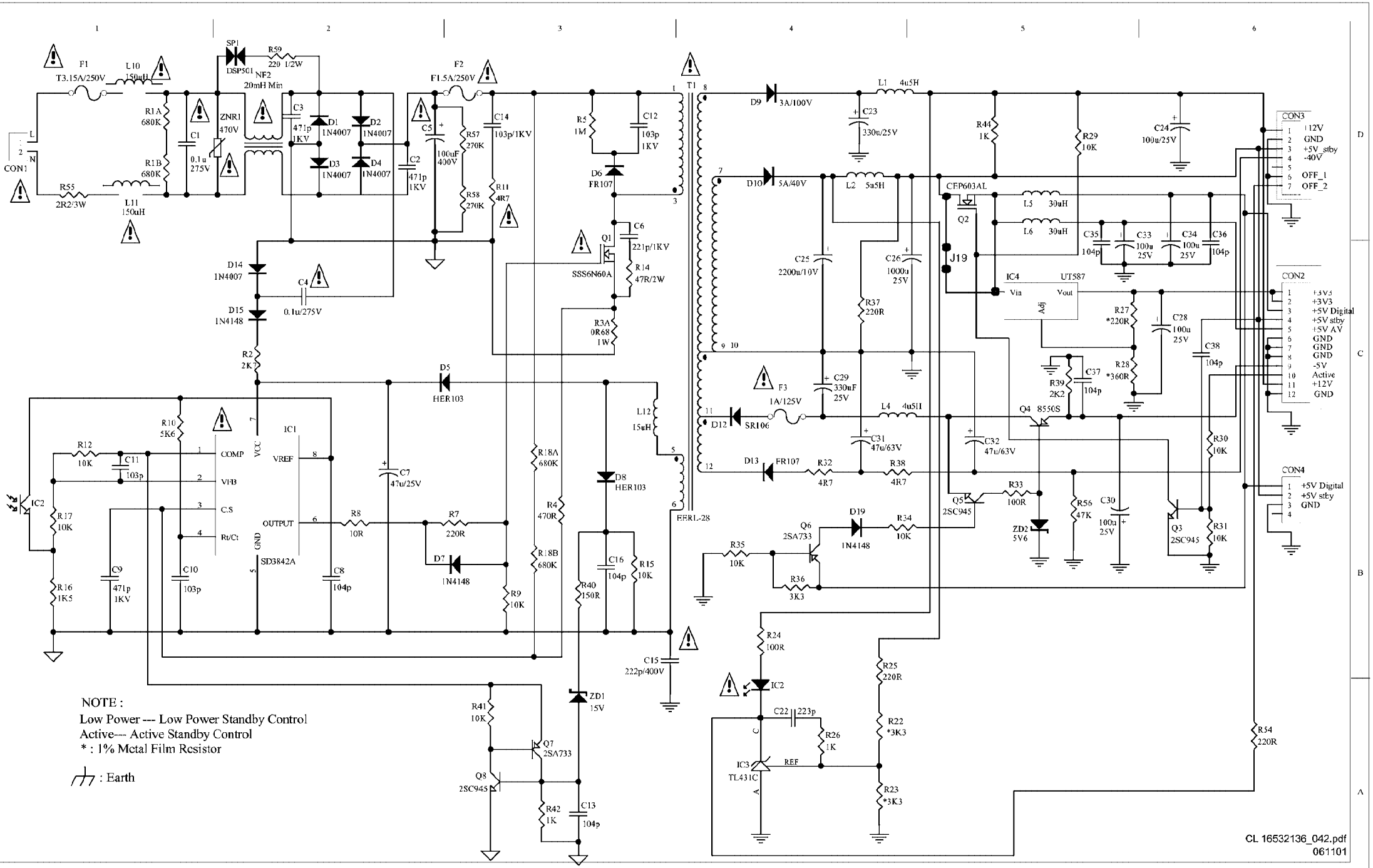
SUPER AUDIO CD

DVD VIDEO™

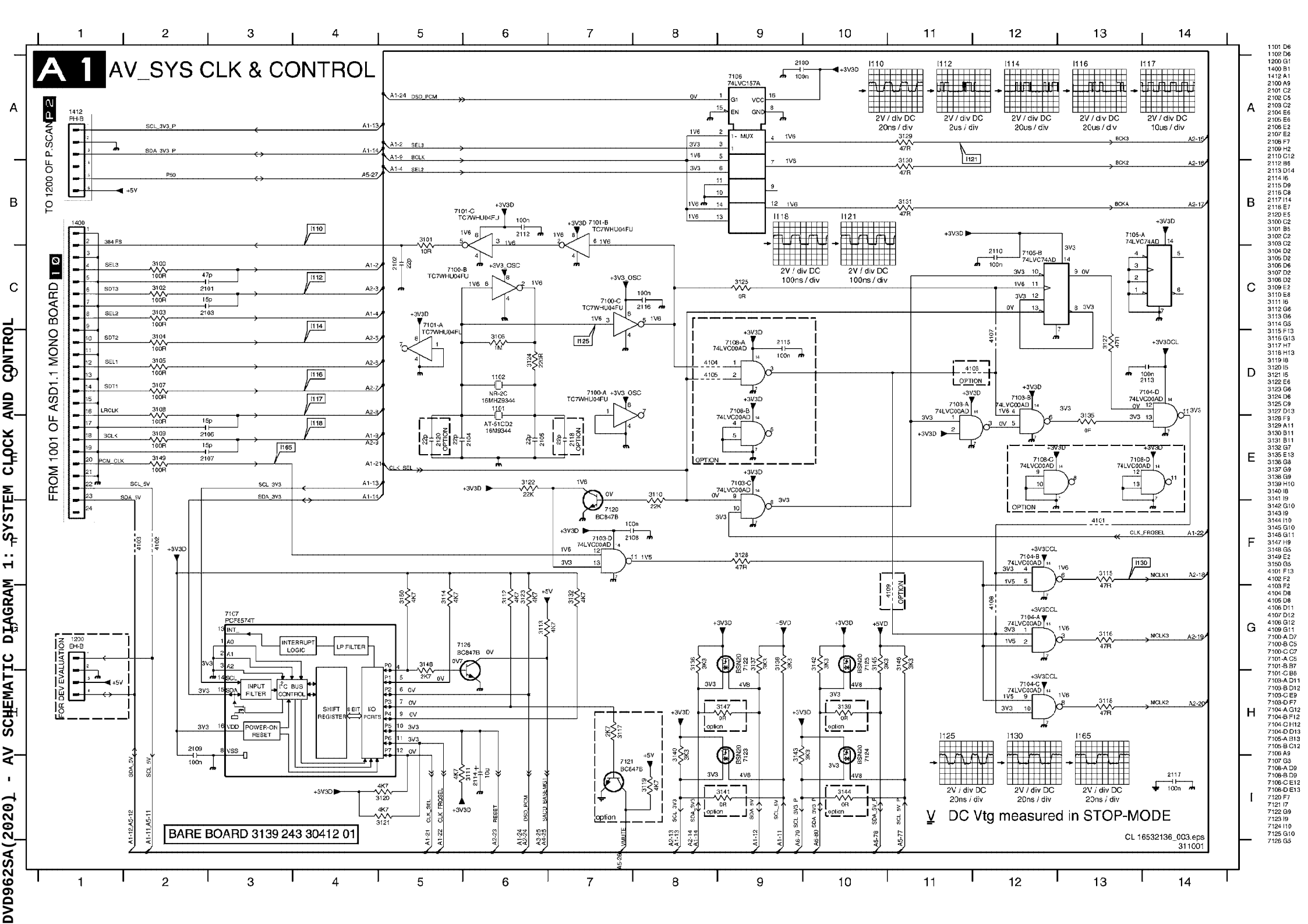
COMPACT disc DIGITAL VIDEO

COMPACT disc DIGITAL AUDIO

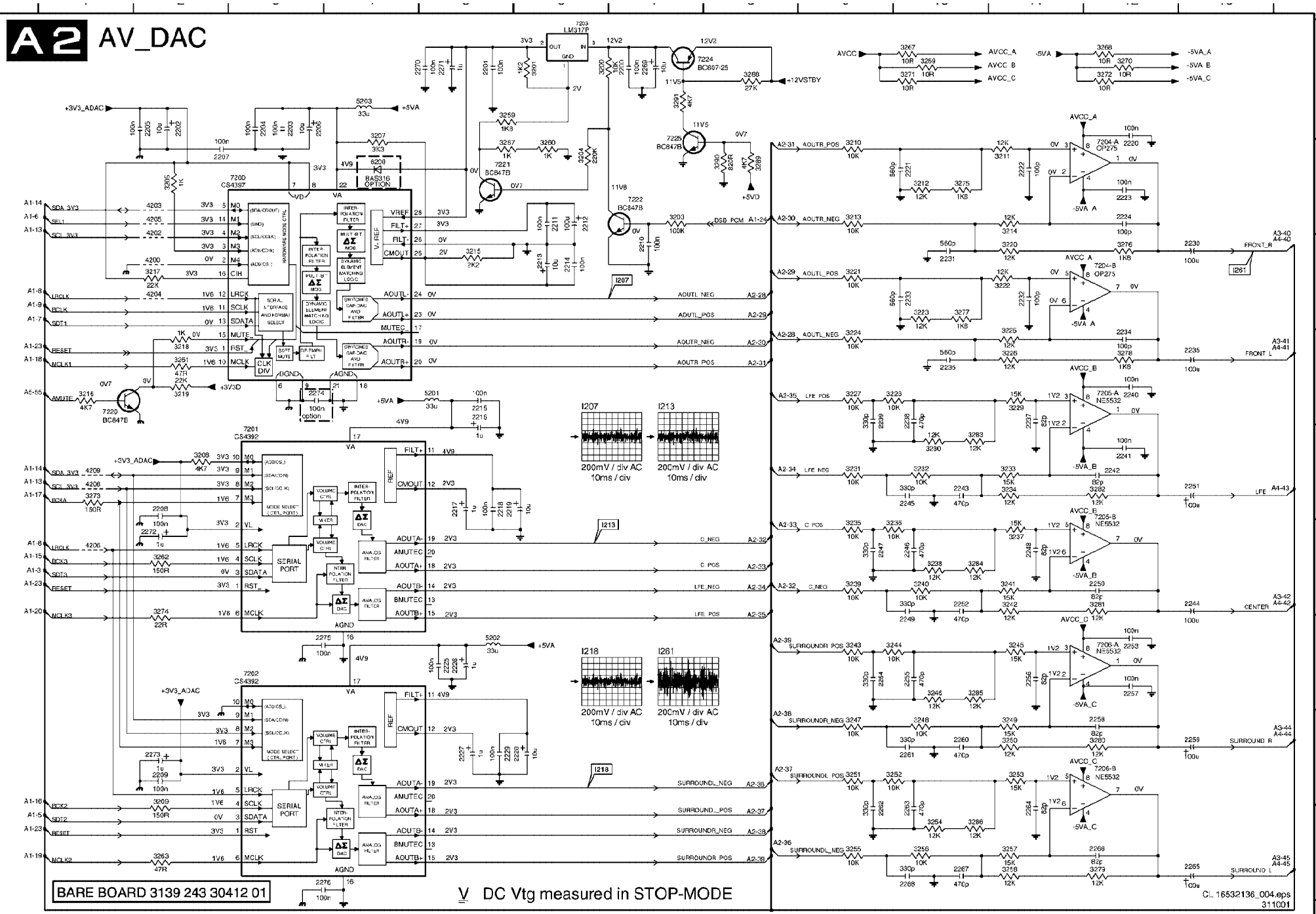

[1001] A / V BOARD
*ONLY FOR MODELS WITH P-SCAN
**[1007]
P.SCAN BOARD
[1005] POWER SUPPLY BOARD
ASD1.1 MONO BOARD
[1002A] DISPLAY BOARD
STANDBY BOARD [1002B]
[1114]
[1111]
[1112]
[1116]
[1108]
[1115]
[1103]
[1102]
[1101]
1411
1412
1400
1404
1405
1001
1604
1603
1002
1200
1501
1603
1100
1205
1103
1107
DVD962SA(2020) - OVERALL WIRING DIAGRAM
CL 16532135_039.eps
231101



DVD962SA(2020) - POWER SUPPLY UNIT SCHEMATIC DIAGRAM


A 1 AV_SYS CLK & CONTROL
FROM 1001 OF ASD1.1 MONO BOARD
TO 1200 OF P.SCAN
BARE BOARD 3139 243 30412 01
DC Vtg measured in STOP-MODE
CL 16532136_003.eps
311001
DVD962SA(2020) - AV SCHEMATIC DIAGRAM 1: SYSTEM CLOCK AND CONTROL

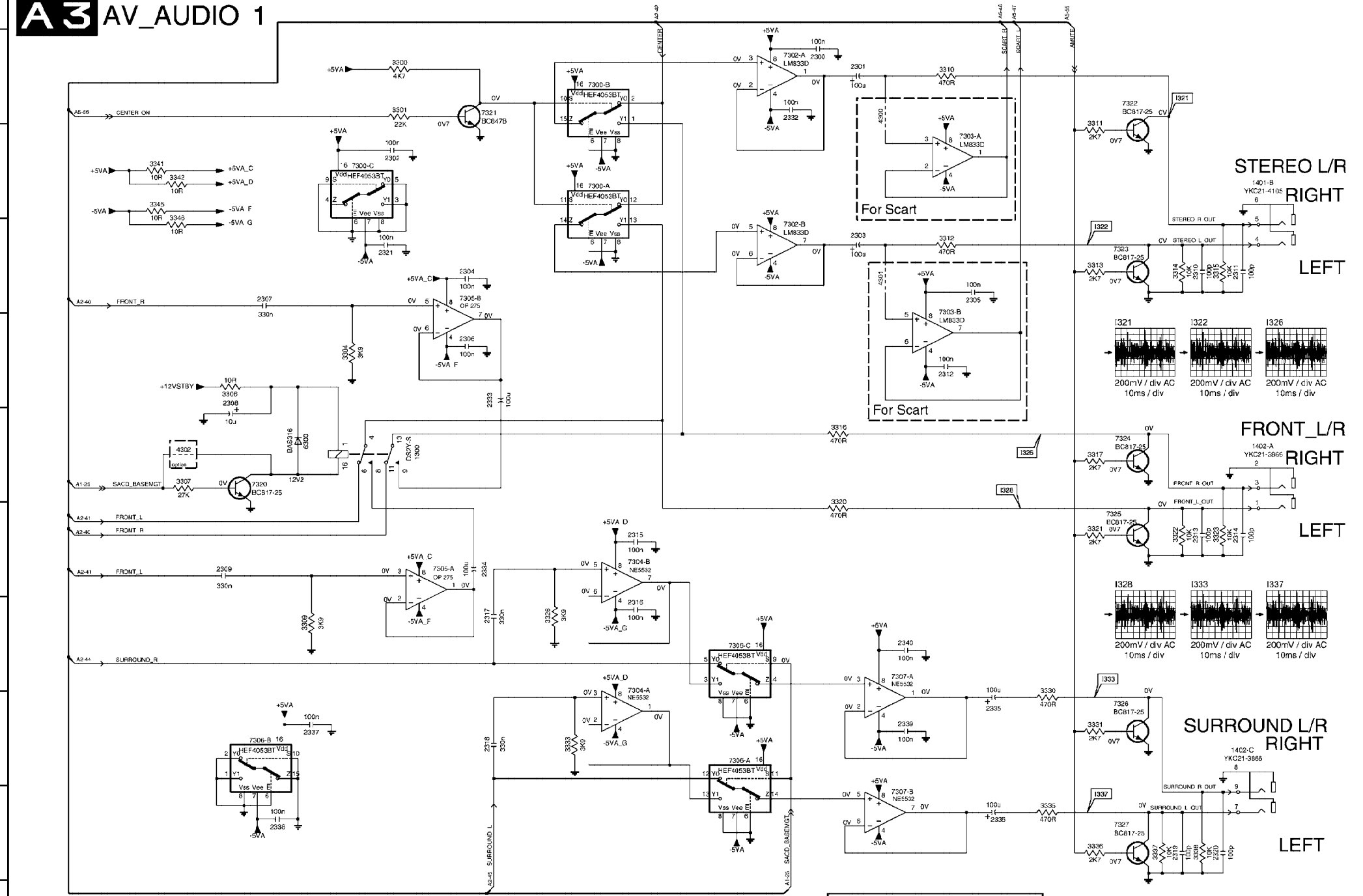
A2 AV_DAC



DVD962SA(2020) - AV SCHEMATIC DIAGRAM 2: DAC

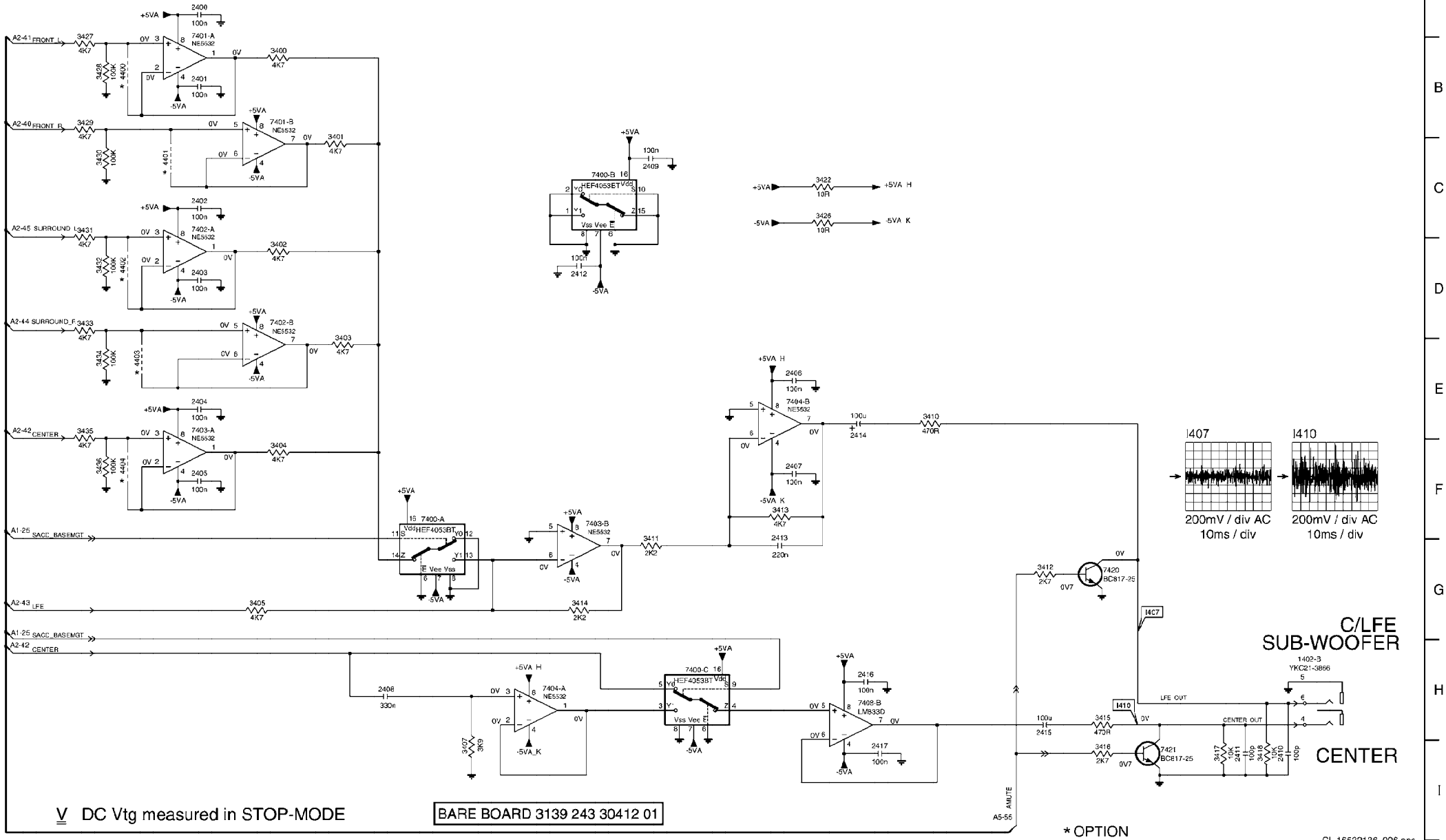
2200 A7
2201 A5
2202 A2
2203 A3
2204 A3
2205 A2
2206 A3
2207 B2
2208 E2
2209 H2
2210 C7
2211 B6
2212 B6
2213 C6
2214 C6
2215 D5
2216 D5
2217 E5
2218 E5
2220 B12
2221 B10
2222 B11
2223 B12
2224 B12
2225 G5
2226 G5
2227 H5
2228 H5
2230 C13
2231 C10
2232 C11
2233 C10
2234 D12
2235 D13
2236 D10
2237 D11
2238 D10
2239 D9
2240 D12
2241 E12
2242 E12
2243 E10
2244 F13
2245 E10
2246 F10
2247 F8
2248 F11
2249 G10
2250 F12
2251 E13
2252 F10
2253 G12
2254 G9
2255 G10
2256 G11
2257 G12
2258 H12
2259 H13
2260 H10
2261 H10
2262 I9
2263 I10
2264 I11
2265 I13
2266 I12
2267 I10
2268 I10
2269 A7
2270 A5
2271 A5
2272 F2
2273 H2
2274 D3
2275 G3
2276 I3
3200 A6
3201 A6
3203 B7
3204 B6
3205 B2
3207 A4
3208 E2
3209 H2
3210 B9
3211 B11
3212 B10
3213 B9
3214 B11
3215 C5
3216 D1
3217 C2
3218 D2
3219 D2
3220 C11
3221 C9
3222 C11
3223 C10
3224 D9
3225 C11
3226 D11
3227 D9
3228 D10
3229 D11
3230 E10
3231 E9
3232 E10
3233 E11
3234 E11
3235 F9
3236 F10
3237 F11
3238 F10
3239 F9
3240 F10
3241 F11
3242 F11
3243 G9
3244 G10
3245 G11
3246 G10
3247 H9
3248 H10
3249 H11
3250 H11
3251 H9
3252 H10
3253 H11
3254 I10
3255 I9
3256 I10
3257 I11
3258 I11
3259 A5
3260 B6
3261 D2
3262 F2
3263 I2
3267 A10
3268 A12
3269 A10
3270 A12
3271 A10
3272 A12
3273 E1
3274 F2
3275 B10
3276 C12
3277 C10
3278 D12
3279 I12
3280 H12
3281 F12
3282 E12
3283 E10
3284 F10
3285 G10
3286 I10
3287 B5
3288 A8
3289 B8
3290 B8
3291 A7
4200 C2
4202 C2
4203 B2
4204 C2
4205 B2
4206 F1
4208 E1
4209 E1
5201 D5
5202 G5
5203 A4
6200 B4
7200 B3
7201 E3
7202 G3
7203 A6
7204-A B12
7204-B C12
7205-A D12
7205-B E12
7206-A G12
7206-B H12
7220 D1
7221 B5
7222 B7
7224 A7
7225 B7

A3 AV_AUDIO 1



DVD962SA(2020) - AV SCHEMATIC DIAGRAM 3: AUDIO 1

A4 AV_AUDIO 2



1402-B H13
2400 A2
2401 B2
2402 C2
2403 D2
2404 E2
2405 F2
2406 E8
2407 F8
2408 H4
2409 C7
2410 I13
2411 I13
2412 D6
2413 G6
2414 E9
2415 H11
2416 H9
2417 I9
3400 B3
3401 C4
3402 D3
3403 E4
3404 F3
3405 G3
3407 I5
3410 E10
3411 G7
3412 G11
3413 F8
3414 G6
3415 H11
3416 I11
3417 I13
3418 I13
3422 C9
3426 C9
3427 B1
3428 B1
3429 B1
3430 C1
3431 C1
3432 D1
3433 D1
3434 E1
3435 E1
3436 F1
4400 B2
4401 C2
4402 D2
4403 E2
4404 F2
7400-A F5
7400-B C6
7400-C H7
7401-A B2
7401-B B3
7402-A C2
7402-B D3
7403-A E2
7403-B F6
7404-A H6
7404-B E8
7408-B H9
7420 G11
7421 I12

A5 AV_VIDEO & SCART

RESERVED FOR DOUBLE SCART

FROM 1604 OF MONO BOARD 6

FROM 1603 OF MONO BOARD 6

For Single Scart

SCART

VIDEO CVBS

S.VIDEO

OPTICAL

DIGITAL

* OPTION

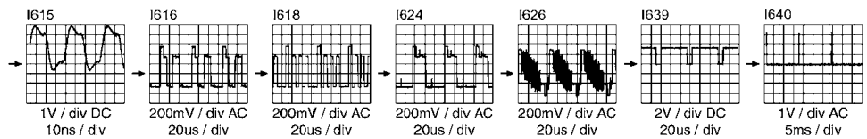
V DC Vtg measured in STOP-MODE

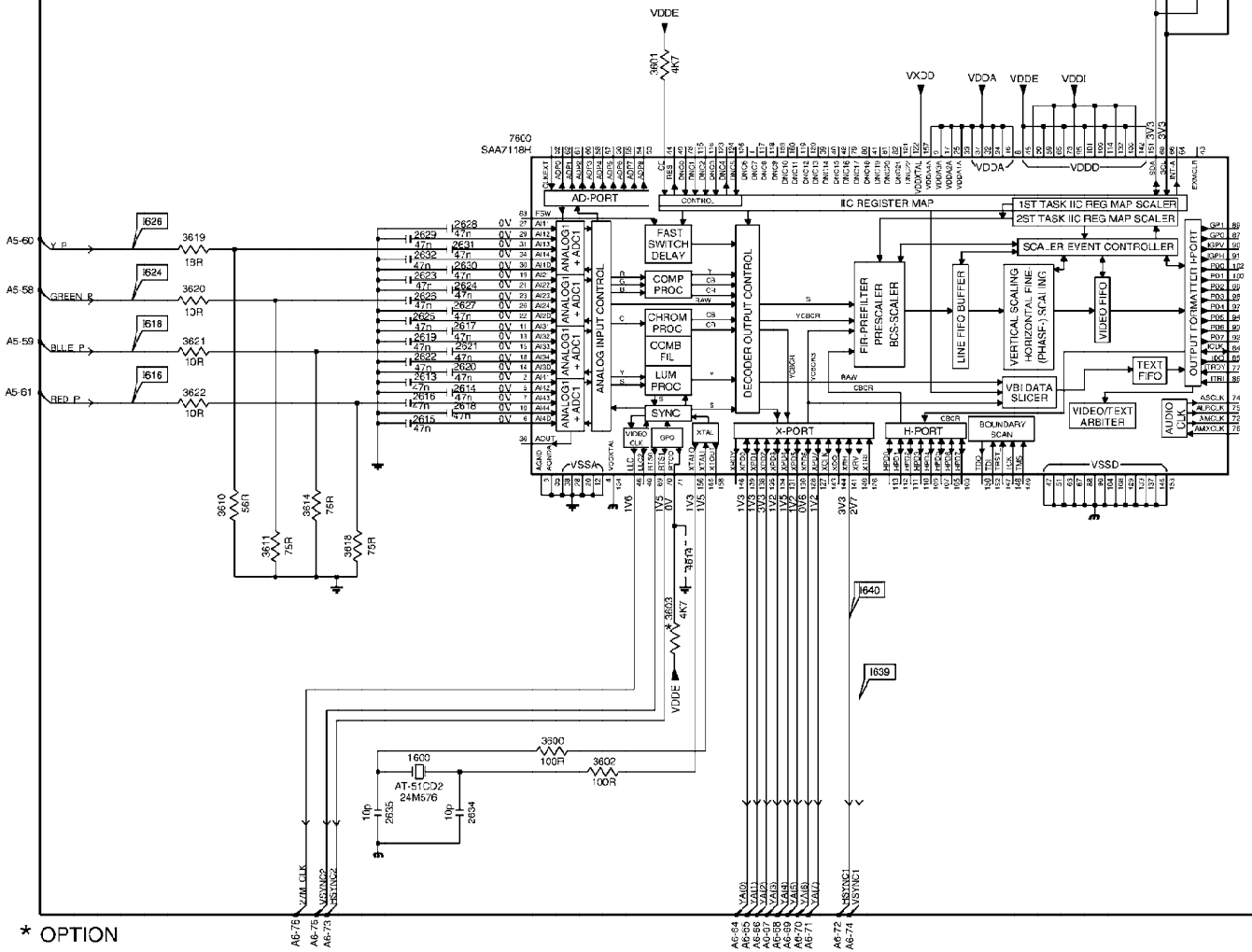
BARE BOARD 3139 243 30412 01

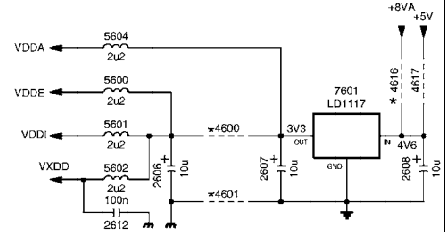
CL 16532136_007.eps
141101

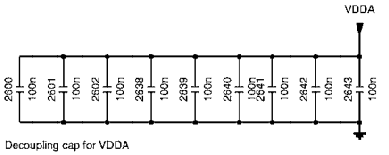
I553 500mV / div AC 20us / div
I554 500mV / div AC 20us / div
I555 500mV / div AC 20us / div
I560 500mV / div AC 20us / div
I562 500mV / div AC 20us / div
I500 200mV / div AC 20us / div
I565 500mV / div AC 20us / div
I502 200mV / div AC 20us / div
I566 500mV / div AC 20us / div
I503 200mV / div AC 20us / div
I572 500mV / div AC 20us / div
I504 200mV / div AC 20us / div
I576 500mV / div AC 20us / div
I505 200mV / div AC 20us / div
I582 500mV / div AC 20us / div
I506 200mV / div AC 20us / div
I583 2V / div DC 200ns / div
I542-I550 200mV / div AC 10ms / div
I585 500mV / div DC 200ns / div

A6 AV_DIGITAL YUV

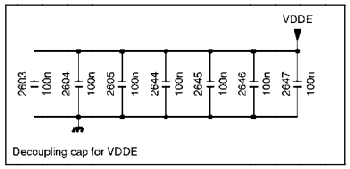




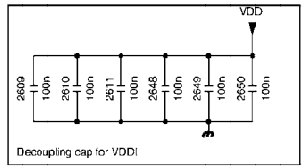




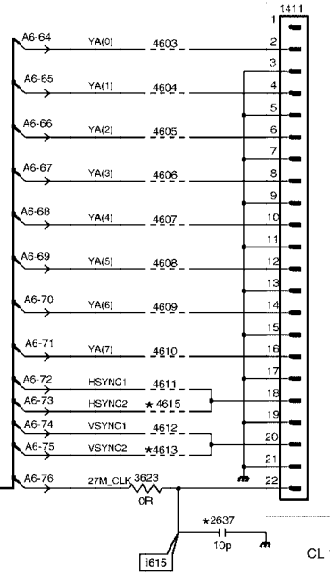
Decoupling cap for VDDA



Decoupling cap for VDDE



Decoupling cap for VDDI



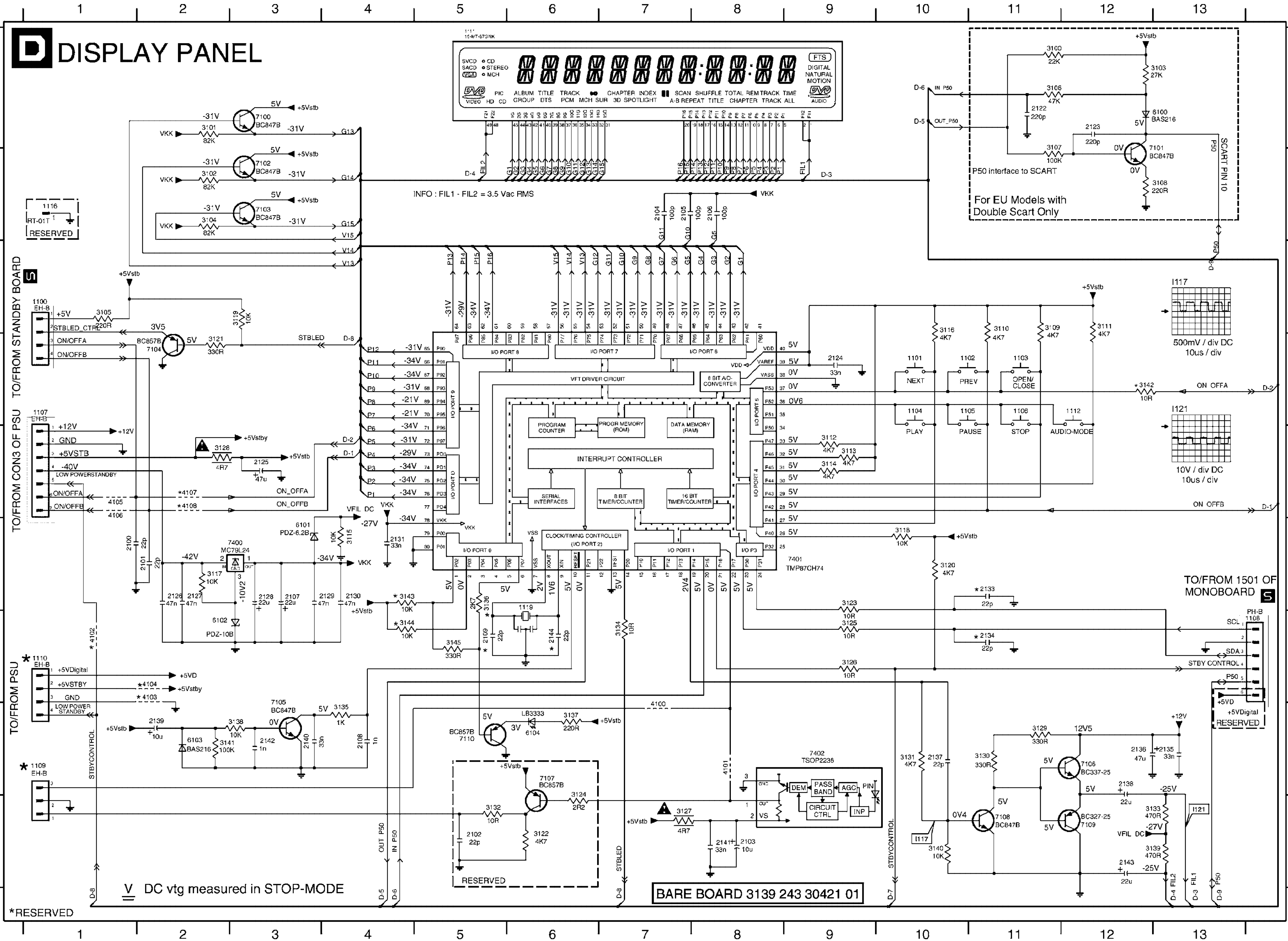
* OPTION

V DC Vtg measured in STOP-MODE

BARE BOARD 3139 243 30412 01

CL 16532136_008.eps
311001

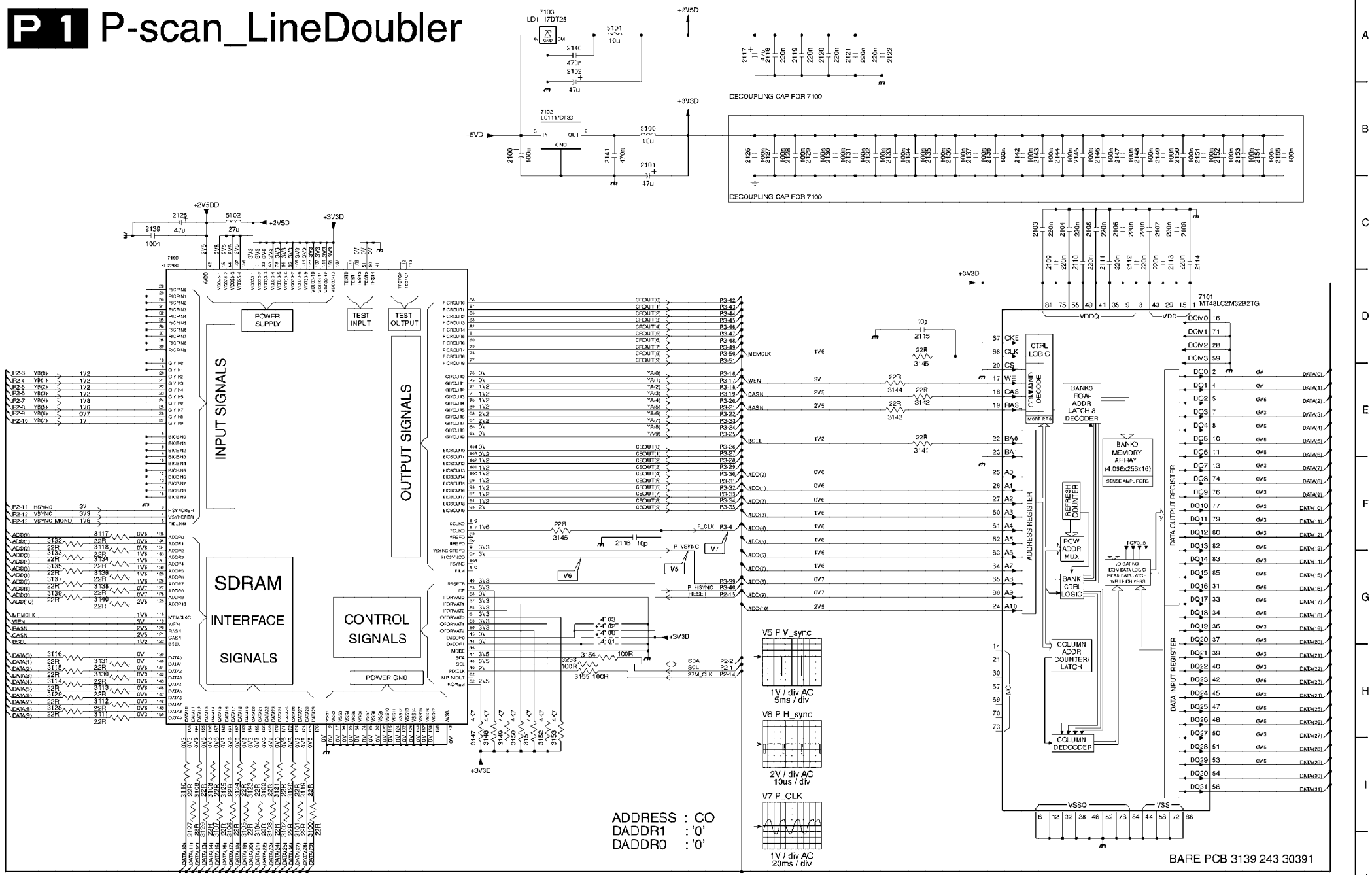
1411 F12
1600 H3
2600 C11
2601 C11
2602 C11
2603 D11
2604 D11
2605 D12
2606 B12
2607 B12
2608 B13
2609 E11
2610 E12
2611 E12
2612 B11
2613 E4
2614 E4
2615 F4
2616 E4
2617 E4
2618 F4
2619 E4
2620 E4
2621 E4
2622 E4
2623 E4
2624 E4
2625 E4
2626 E4
2627 E4
2628 D4
2629 D4
2630 E4
2631 D4
2632 E4
2634 H4
2635 H3
2637 I12
2638 C12
2639 C12
2640 C12
2641 C12
2642 C13
2643 C13
2644 D12
2645 D12
2646 D13
2647 D13
2648 E12
2649 E13
2650 E13
3600 H4
3601 C5
3602 H5
3603 G5
3610 F2
3611 G2
3614 F3
3618 G3
3619 D2
3620 E2
3621 E2
3622 F2
3623 I11
3624 C9
3625 B8
3627 B9
3628 B9
4600 B12
4601 B12
4603 F12
4604 G12
4605 G12
4606 G12
4607 G12
4608 H12
4609 H12
4610 H12
4611 H12
4612 I12
4613 I12
4614 G5
4615 I12
4616 A13
4617 A13
5600 A11
5601 B11
5602 B11
5604 A11
7600 D4
7601 A13



1100 C1	7109 I12
1101 D10	7110 H5
1102 D10	7400 F3
1103 D11	7401 F9
1104 D10	7402 H9
1105 D10	
1106 D11	
1107 D1	
1108 G13	
1109 H1	
1110 G1	
1111 A5	
1112 D12	
1116 B1	
1119 F6	
2100 F1	
2101 F2	
2102 I5	
2103 I8	
2104 B7	
2105 B7	
2106 B8	
2107 F3	
2108 H4	
2109 G5	
2122 A11	
2123 A12	
2124 D9	
2125 E3	
2126 F2	
2127 F2	
2128 F3	
2129 F4	
2130 F4	
2131 F4	
2133 F11	
2134 G11	
2135 H13	
2136 H12	
2137 H10	
2138 H12	
2139 H2	
2140 H3	
2141 I8	
2142 H3	
2143 I12	
2144 G6	
3100 A11	
3101 A2	
3102 B2	
3103 A13	
3104 B2	
3105 C1	
3106 A11	
3107 B11	
3108 B13	
3109 C11	
3110 C11	
3111 C12	
3112 E9	
3113 E9	
3114 E9	
3115 F4	
3116 C10	
3117 F2	
3118 F10	
3119 C3	
3120 F10	
3121 D2	
3122 I6	
3123 F9	
3124 I6	
3125 G9	
3126 G9	
3127 I7	
3128 E2	
3129 H11	
3130 H11	
3131 H10	
3132 I5	
3133 I12	
3134 G7	
3135 H4	
3136 F5	
3137 H6	
3138 H3	
3139 I12	
3140 I10	
3141 H2	
3142 D12	
3143 F4	
3144 G4	
3145 G5	
4100 H7	
4101 H8	
4102 G1	
4103 G2	
4104 G2	
4105 E1	
4106 E1	
4107 E2	
4108 E2	
6100 A13	
6101 F3	
6102 G2	
6103 H2	
6104 H6	
7100 A3	
7101 B12	
7102 B3	
7103 B3	
7104 D2	
7105 H3	
7106 H12	
7107 H6	
7108 I11	

CL 16532136_013.eps
311001

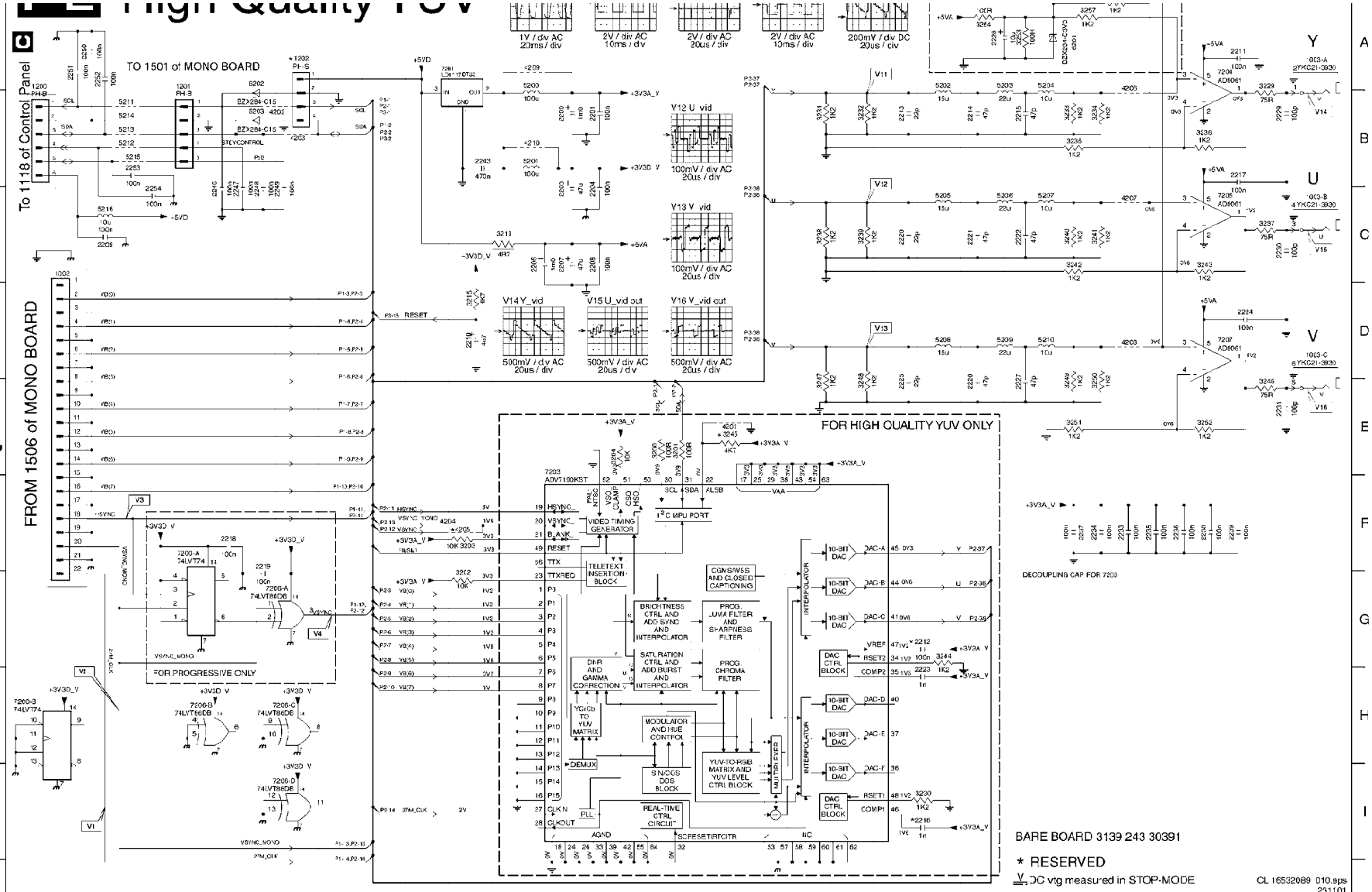
P 1 P-scan_LineDoubler



* RESERVED

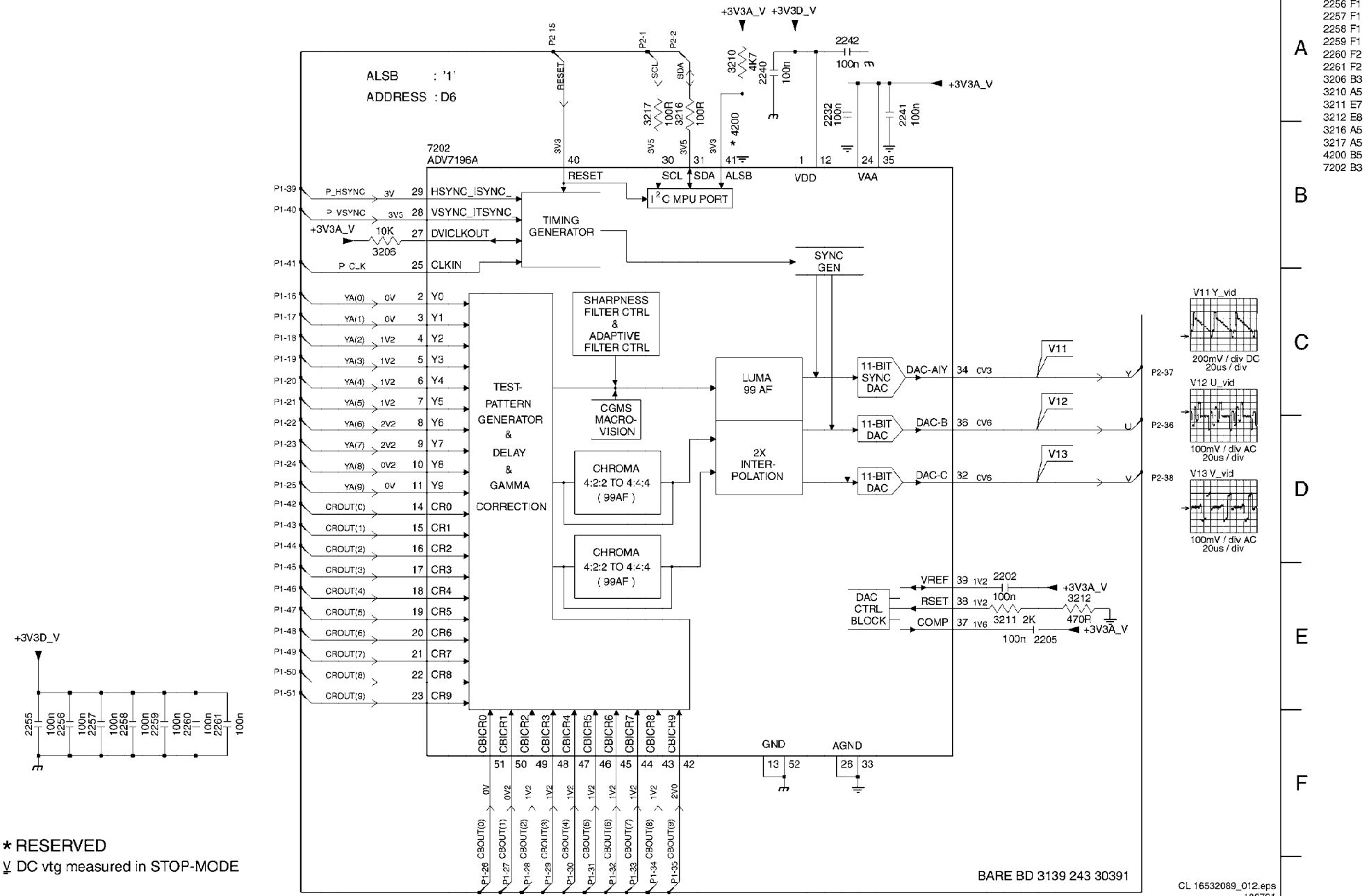
V DC vtg measured in STOP-MODE

CL 16532089_009.eps
250701



ITEM NO	DESCRIPTION	DVD9623A/091 DVD9623A/171 Progressive YUV	(Not use) High Quality YUV
2212	CER2 0603 X7R 16V 100N COL		X
2213	CER1 0603 NP0 50V 6P8 COL	X	
2213	CER1 0603 NP0 50V 27P COL		X
2214	CER1 0603 NP0 50V 22P COL	X	
2214	CER1 0603 NP0 50V 68P COL		X
2215	CER1 0603 NP0 50V 18P COL		
2216	CER2 0603 X7R 50V 1N COL		X
2218	CER2 0603 X7R 16V 100N COL	X	
2219	CER2 0603 X7R 16V 100N COL	X	
2220	CER1 0603 NP0 50V 6P8 COL	X	
2220	CER1 0603 NP0 50V 27P COL		X
2221	CER1 0603 NP0 50V 22P COL	X	
2221	CER1 0603 NP0 50V 68P COL		X
2222	CER1 0603 NP0 50V 18P COL	X	
2223	CER2 0603 X7R 50V 1N COL		X
2225	CER1 0603 NP0 50V 6P8 COL	X	
2225	CER1 0603 NP0 50V 27P COL		X
2226	CER1 0603 NP0 50V 22P COL	X	
2226	CER1 0603 NP0 50V 68P COL		X
2227	CER1 0603 NP0 50V 18P COL	X	
2229	CER1 0603 NP0 50V 100P COL		X
2230	CER1 0603 NP0 50V 100P COL		X
2231	CER1 0603 NP0 50V 100P COL		X
2232	CER2 0603 X7R 16V 100N COL	X	
2233	CER2 0603 X7R 16V 100N COL		X
2234	CER2 0603 X7R 16V 100N COL		X
2235	CER2 0603 X7R 16V 100N COL		X
2236	CER2 0603 X7R 16V 100N COL		X
2237	CER2 0603 X7R 16V 100N COL		X
2238	CER2 0603 X7R 16V 100N COL		X
2239	CER2 0603 X7R 16V 100N COL		X
3200	RST SM 0603 100R PM5 COL		X
3201	RST SM 0603 100R PM5 COL		X
3204	RST SM 0603 10K PM5 COL		X
3230	RST SM 0603 1K2 PM5 COL		X
3244	RST SM 0603 1K2 PM5 COL		X
3245	RST SM 0603 4K7 PM5 COL	X	
3204	RST SM 0603 JUMP 0R05 COL		X
5202	FKDIND SM 0805 6U8 PM10 COL R	X	
5202	FKDIND SM 0805 22U PM20 COL R		X
5203	FKDIND SM 0805 10U PM10 COL R	X	
5203	RST SM 0805 JUMP 0R05 COL R		
5204	FKDIND SM 0805 2U2 PM10 COL R	X	
5204	FKDIND SM 0805 10U PM10 COL R		X
5205	FKDIND SM 0805 6U8 PM10 COL R	X	
5205	FKDIND SM 0805 22U PM20 COL R		X
5206	FKDIND SM 0805 10U PM10 COL R	X	
5206	RST SM 0805 JUMP 0R05 COL R		X
5207	FKDIND SM 0805 2U2 PM10 COL R	X	
5207	FKDIND SM 0805 10U PM10 COL R		X
5208	FKDIND SM 0805 6U8 PM10 COL R	X	
5208	FKDIND SM 0805 22U PM20 COL R		X
5209	FKDIND SM 0805 10U PM10 COL R	X	
5209	RST SM 0805 JUMP 0R05 COL R		X
5210	FKDIND SM 0805 2U2 PM10 COL R	X	
5210	FKDIND SM 0805 10U PM10 COL R		X
7200	IC SM 74_VT74DB (PHSE) R	X	
7203	IC SM ADV7150KST (ANAD) Y		X
7206	IC SM 74_VT86DB (PHSE) R	X	

P3 P_scan_Encoder



* RESERVED

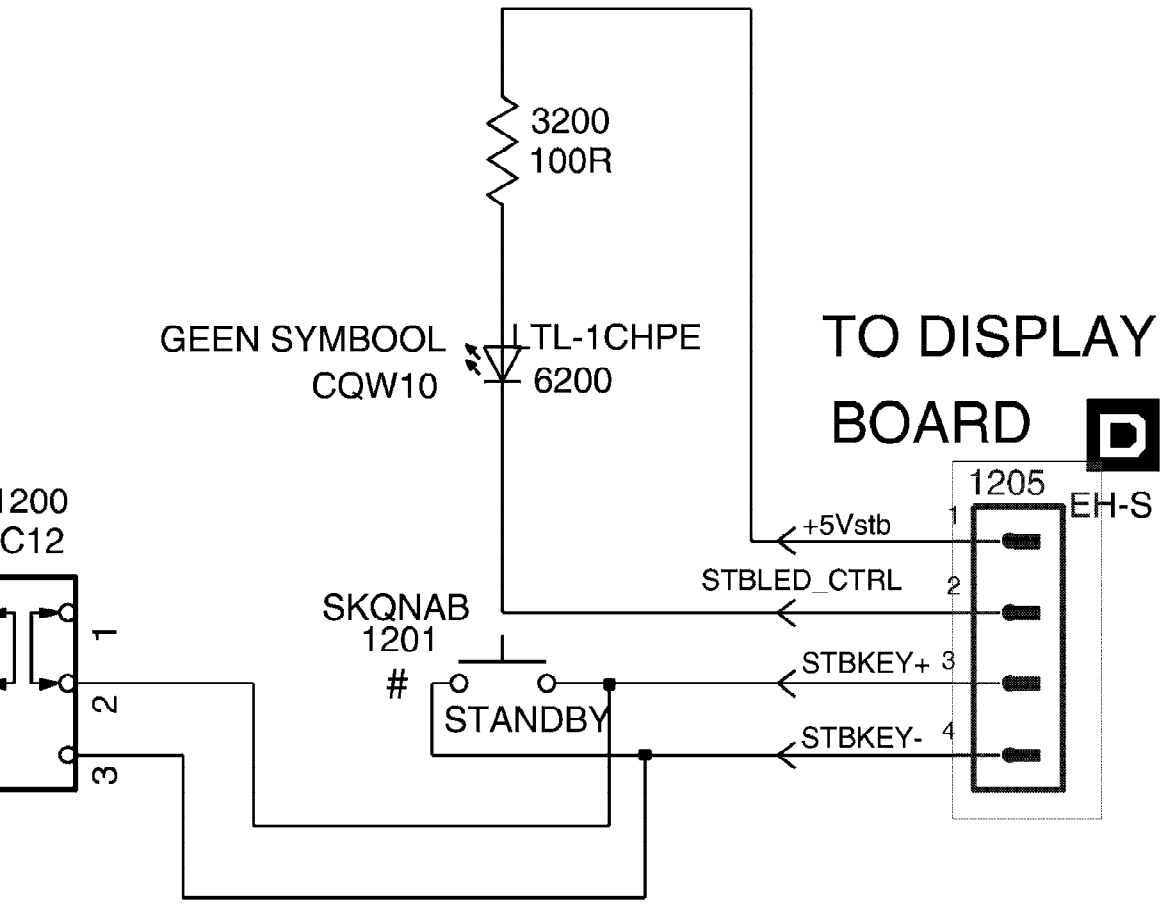
V DC vtg measured in STOP-MODE

2202 E7
2205 E7
2232 A6
2240 A5
2241 A6
2242 A6
2255 F1
2256 F1
2257 F1
2258 F1
2259 F1
2260 F2
2261 F2
3206 B3
3210 A5
3211 E7
3212 E8
3216 A5
3217 A5
4200 B5
7202 B3

oard

Standby Board

1200 C1
1201 C3
1205 C5
3200 A3
6200 B3



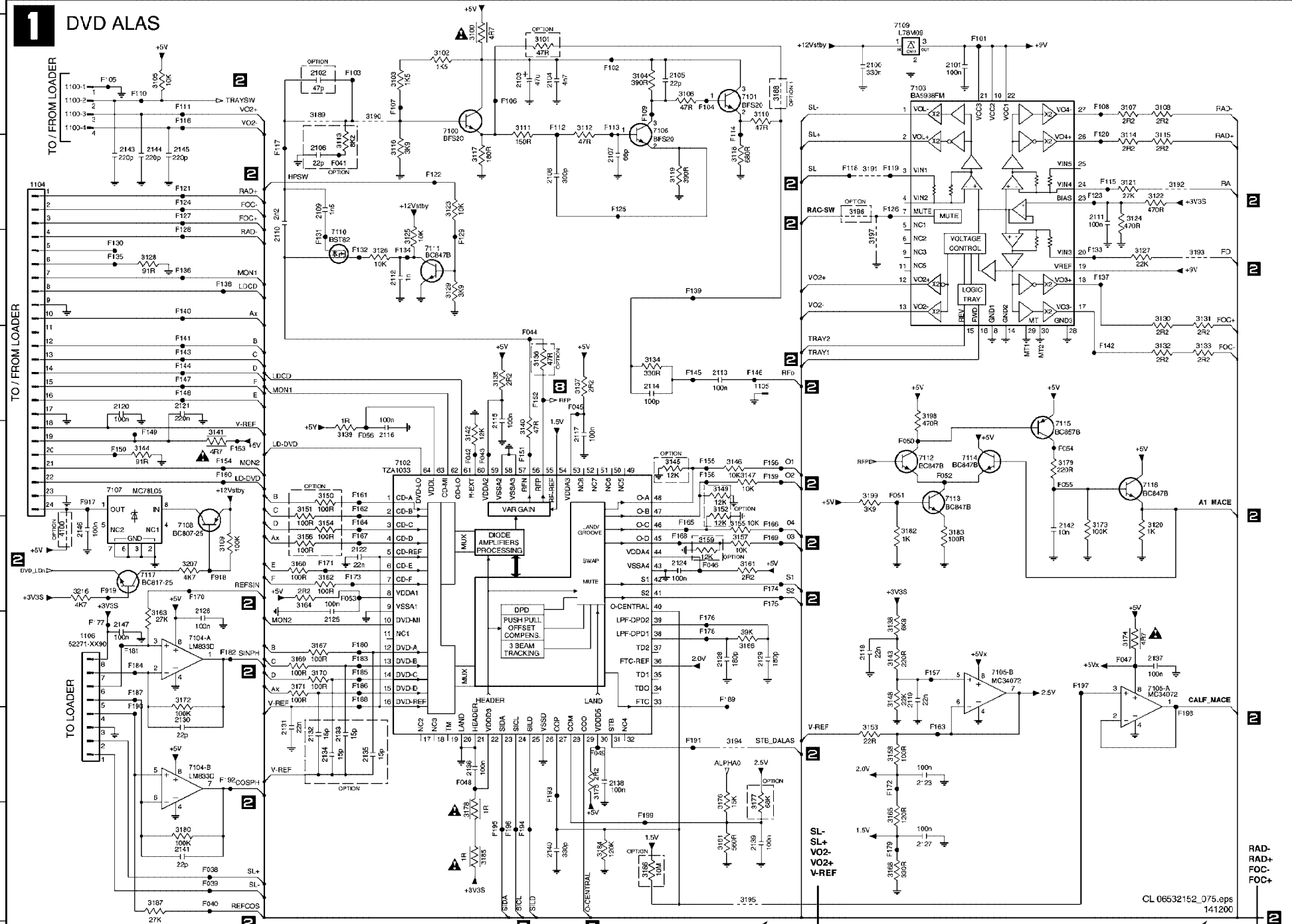
RSITY TABLE FOR STANDBY BOARD

Model using Mech SW	Mode using Tact SW
*	
	*

BOARD 3139 243 30421 01

CL 16532136_014.eps
141101

1 DVD ALAS



1100-1 A1	3162 F4	F138 C3
1100-2 A1	3163 G2	F139 C7
1100-3 A1	3164 F3	F140 C2
1100-4 A1	3165 I10	F141 D2
1104 B1	3166 G8	F142 D12
1105 D8	3167 G4	F143 D2
1106 G1	3168 I10	F144 D2
2100 A9	3169 G3	F145 D7
2101 A10	3170 G4	F146 D8
2102 A4	3171 G3	F147 D2
2103 A6	3172 G2	F148 D2
2104 A6	3173 F12	F149 E2
2105 A7	3174 G12	F150 E1
2106 B4	3175 H6	F151 E6
2107 B7	3176 H8	F152 D6
2108 B6	3177 H8	F153 E3
2109 B4	3178 I5	F154 E3
2110 C3	3179 E11	F155 E8
2111 B12	3180 I2	F156 E8
2112 C4	3181 I8	F157 G10
2113 D8	3182 F10	F158 E8
2114 D7	3183 F10	F159 E8
2115 E5	3184 I6	F160 E3
2116 E4	3185 I5	F161 E4
2117 E6	3186 I7	F162 E4
2118 G9	3187 I2	F163 H10
2119 G10	3188 A8	F164 F4
2120 D1	3189 A4	F165 F7
2121 D2	3190 A4	F166 F8
2122 F4	3191 B9	F167 F4
2123 H10	3192 B13	F168 F7
2124 F7	3193 C13	F169 F8
2125 G4	3194 H8	F170 F2
2126 G2	3195 I8	F171 F4
2127 I10	3196 B9	F172 H10
2128 G8	3197 C9	F173 F4
2129 G8	3198 D10	F174 F8
2130 H2	3199 E9	F175 F8
2131 H3	3207 F2	F176 G8
2132 H3	3216 F1	F177 G1
2133 H4	4100 F1	F178 G8
2134 H4	7100 A5	F179 I10
2135 H4	7101 A8	F180 G4
2136 H5	7102 E4	F181 G2
2137 G12	7103 A10	F182 G3
2138 H7	7104-A G2	F183 G4
2139 I8	7104-B H2	F184 G2
2140 I6	7105-A G12	F185 G4
2141 I2	7105-B G11	F186 G4
2142 F11	7106 A7	F187 G2
2143 B2	7107 E1	F188 G4
2144 B2	7108 F2	F189 G8
2145 B2	7109 A10	F190 H2
2146 F1	7110 C4	F191 H7
2147 G1	7111 C5	F192 H3
3100 A5	7112 E10	F193 H6
3101 A6	7113 E10	F194 I6
3102 A5	7114 E10	F195 I5
3103 A4	7115 E11	F196 I6
3104 A7	7116 E12	F197 G12
3105 A2	7117 F2	F198 H13
3106 A7	F038 I2	F199 I7
3107 A12	F039 I2	F917 E1
3108 A12	F040 I2	F918 F2
3109 F2	F041 B4	F919 F1
3110 A8	F042 E5	
3111 A6	F043 E5	
3112 A6	F044 D6	
3113 B4	F045 D6	
3114 B12	F046 F8	
3115 B12	F047 G12	
3116 B4	F048 H5	
3117 B5	F049 H6	
3118 B8	F050 E10	
3119 B7	F051 E10	
3120 F12	F052 E10	
3121 B12	F053 F4	
3122 B12	F054 E11	
3123 B5	F055 E11	
3124 B12	F056 E4	
3125 C4	F101 A10	
3126 C4	F102 A7	
3127 C12	F103 A4	
3128 C2	F104 A8	
3129 C5	F105 A1	
3130 C12	F106 A6	
3131 C13	F107 A4	
3132 D12	F108 A12	
3133 D13	F109 A7	
3134 D7	F110 A2	
3135 D5	F111 A2	
3136 D6	F112 A6	
3137 D6	F113 A7	
3138 G10	F114 A8	
3139 E4	F115 B12	
3140 E6	F116 A2	
3141 E3	F117 B3	
3142 E5	F118 B9	
3143 G10	F119 B10	
3144 E2	F120 B12	
3145 E7	F121 B2	
3146 E8	F122 B5	
3147 E8	F123 B12	
3148 G10	F124 B2	
3149 E8	F125 B7	
3150 E4	F126 B10	
3151 E3	F127 B2	
3152 E8	F128 C2	
3153 H9	F129 C5	
3154 F4	F130 C1	
3155 F8	F131 C4	
3156 F3	F132 C4	
3157 F8	F133 C12	
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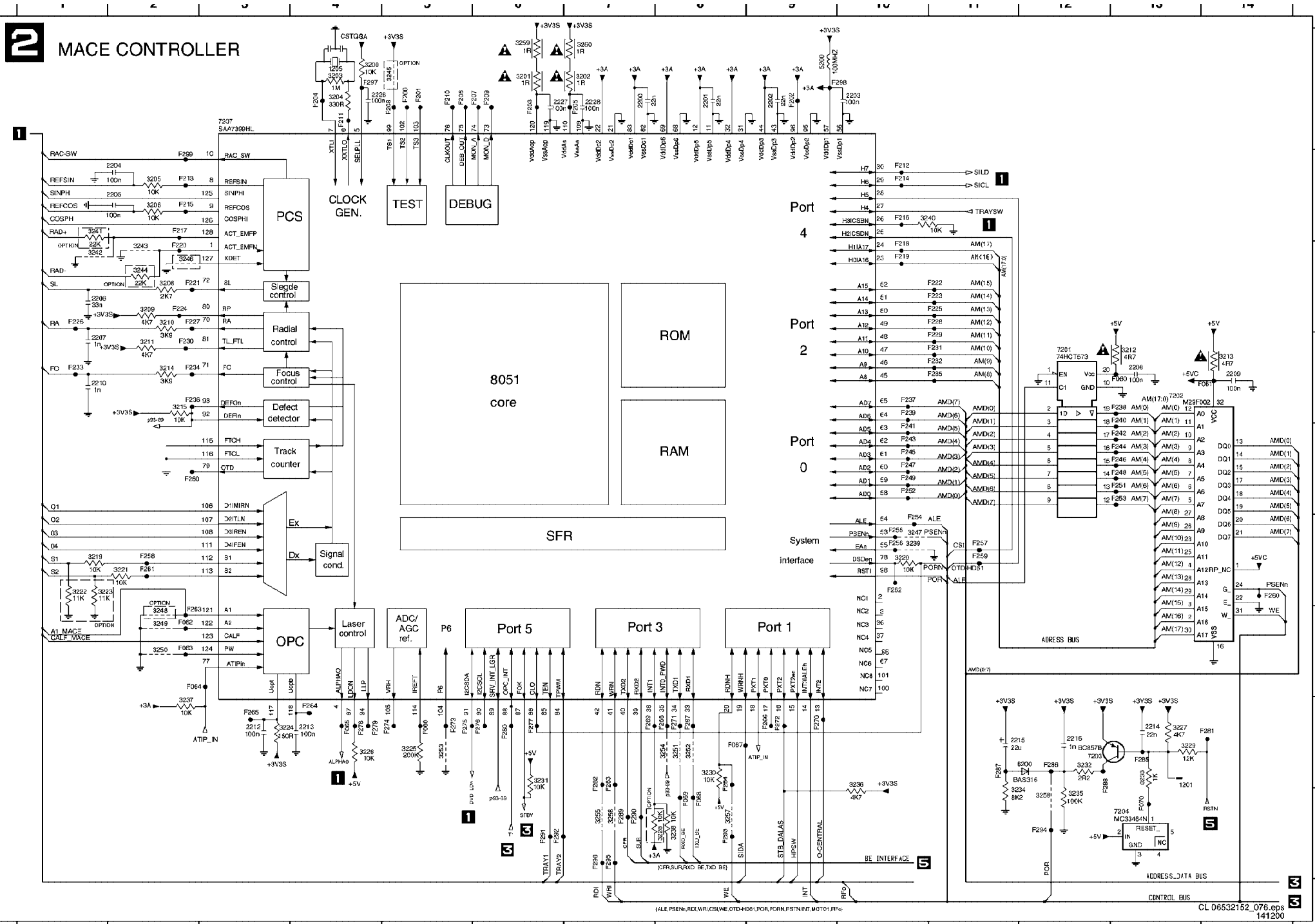
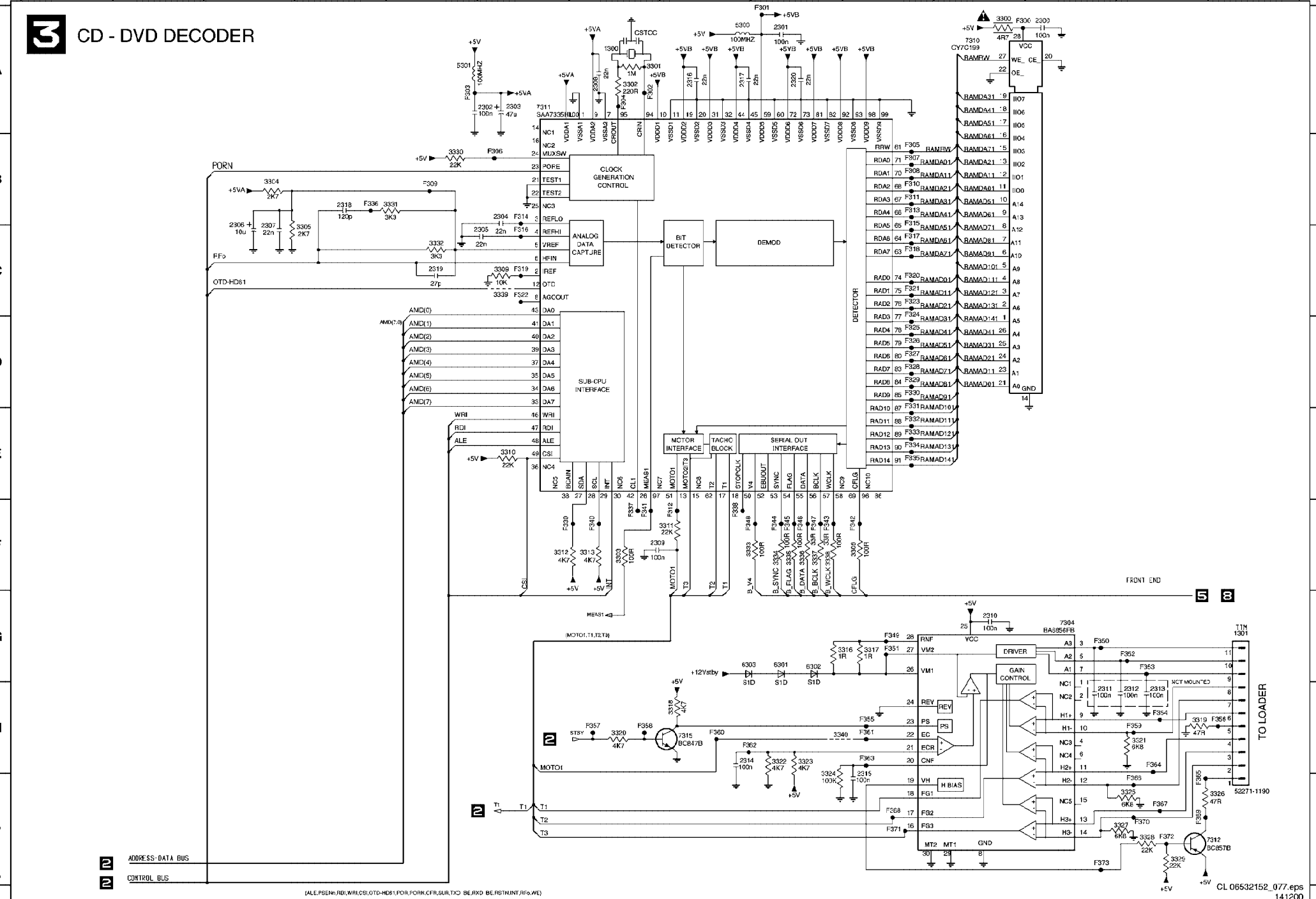
3160 F3	F136 C2	
3161 F8	F137 C12	

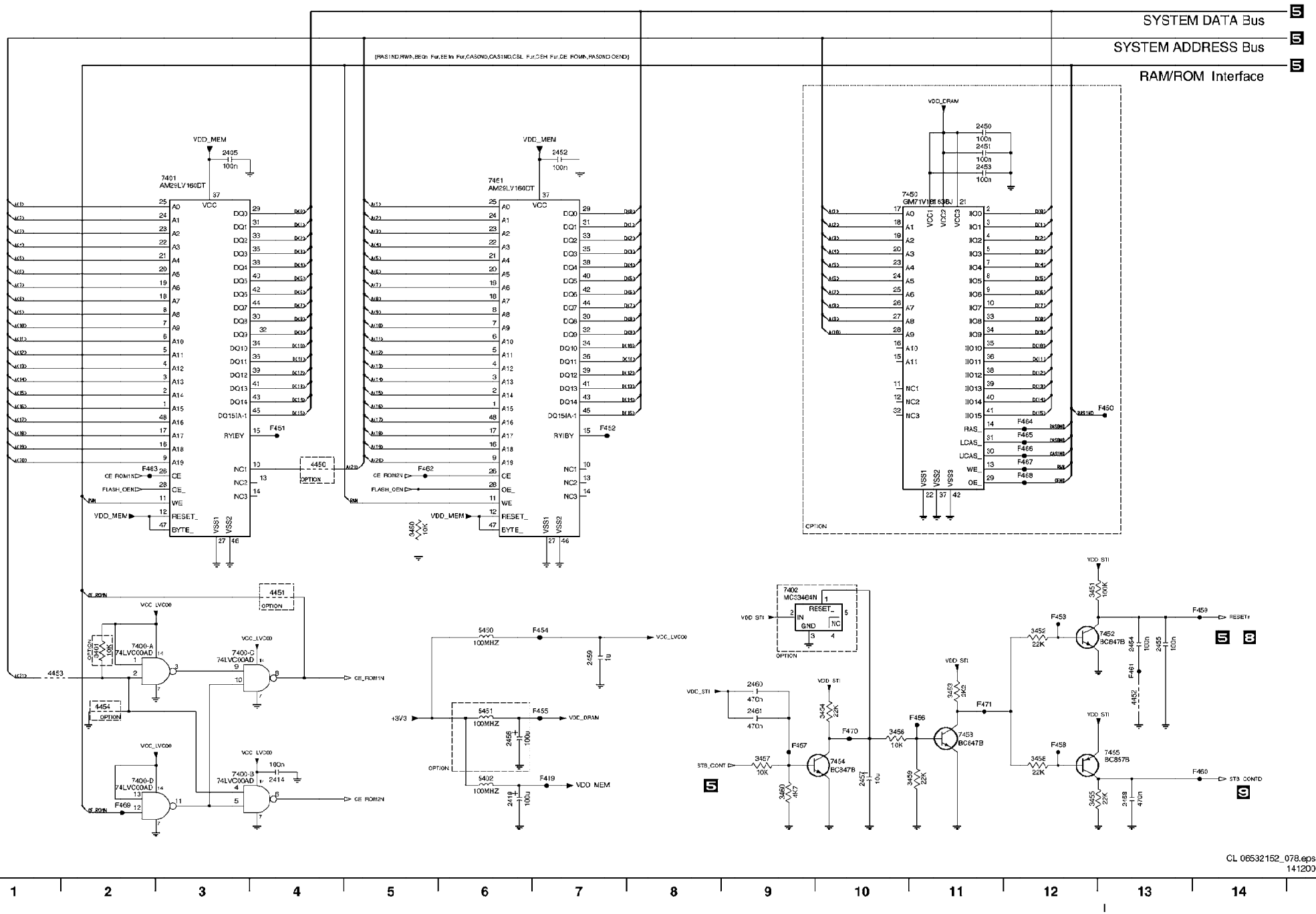
2 MACE CONTROLLER

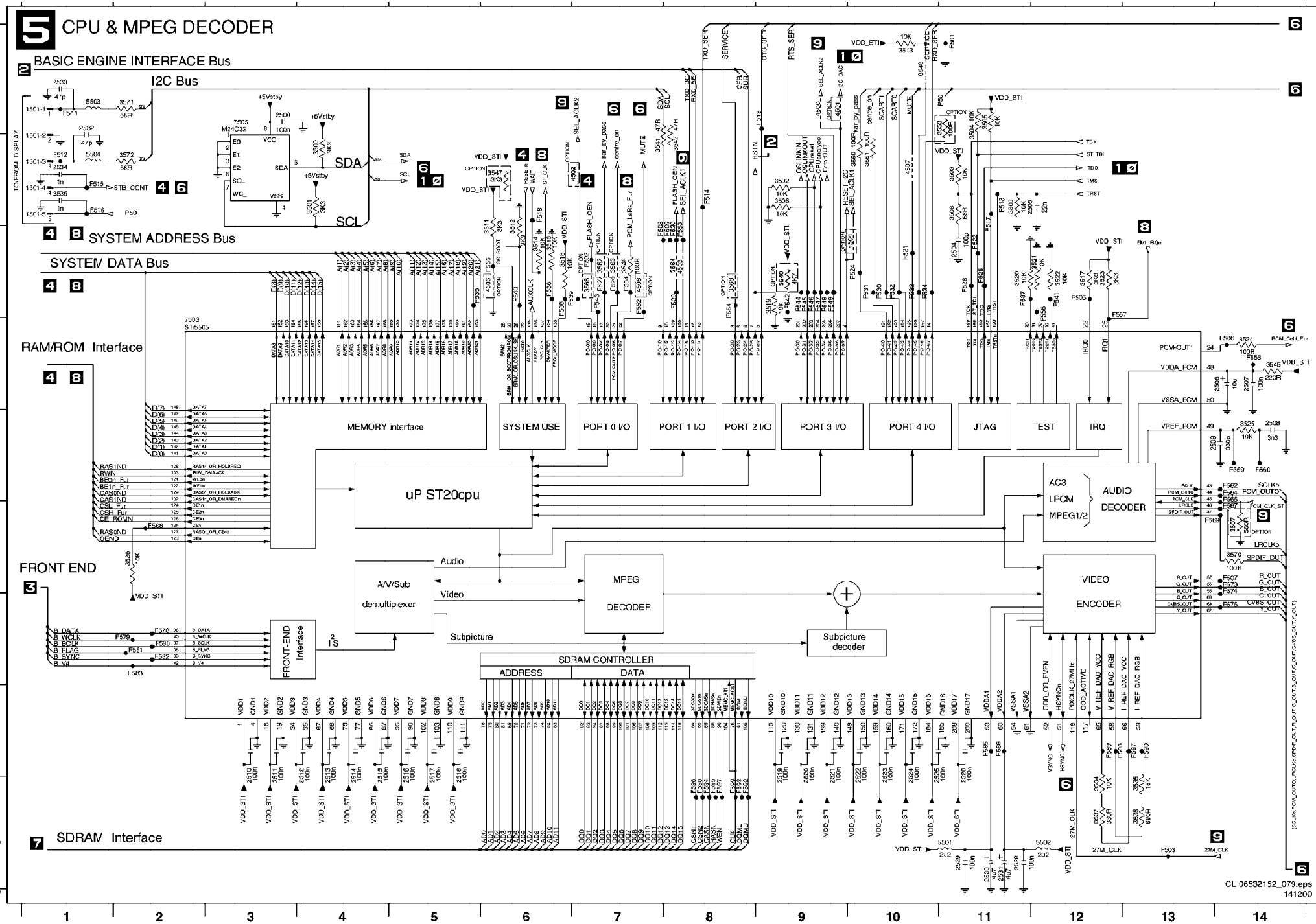


3 CD - DVD DECODER



4 PROGRAM MEMORIES

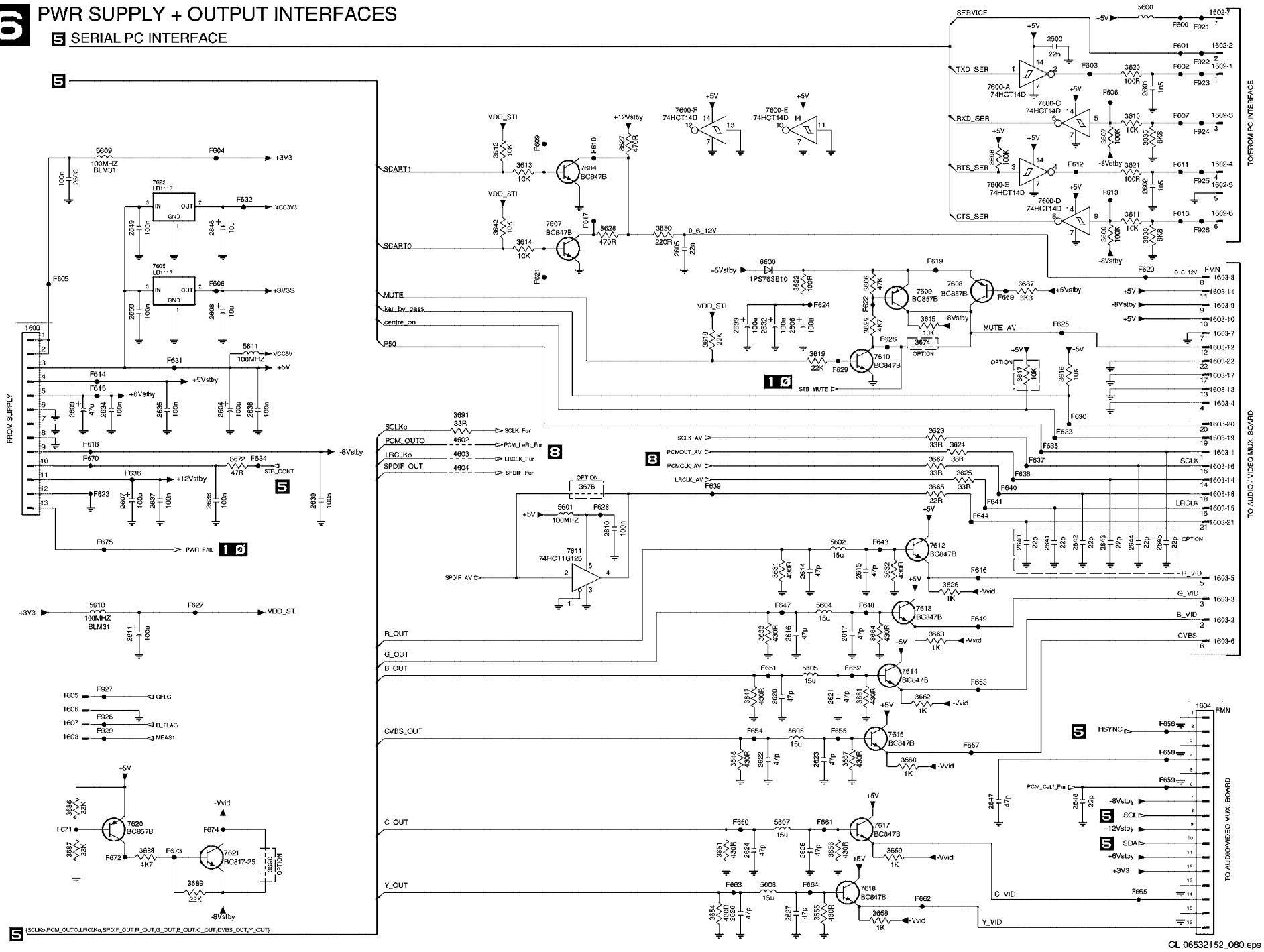




DVD962SA(2020)_- MONO SCHEMATIC DIAGRAM 5 : CPU_AND_MPEG DECODER

6 PWR SUPPLY + OUTPUT INTERFACES

5 SERIAL PC INTERFACE



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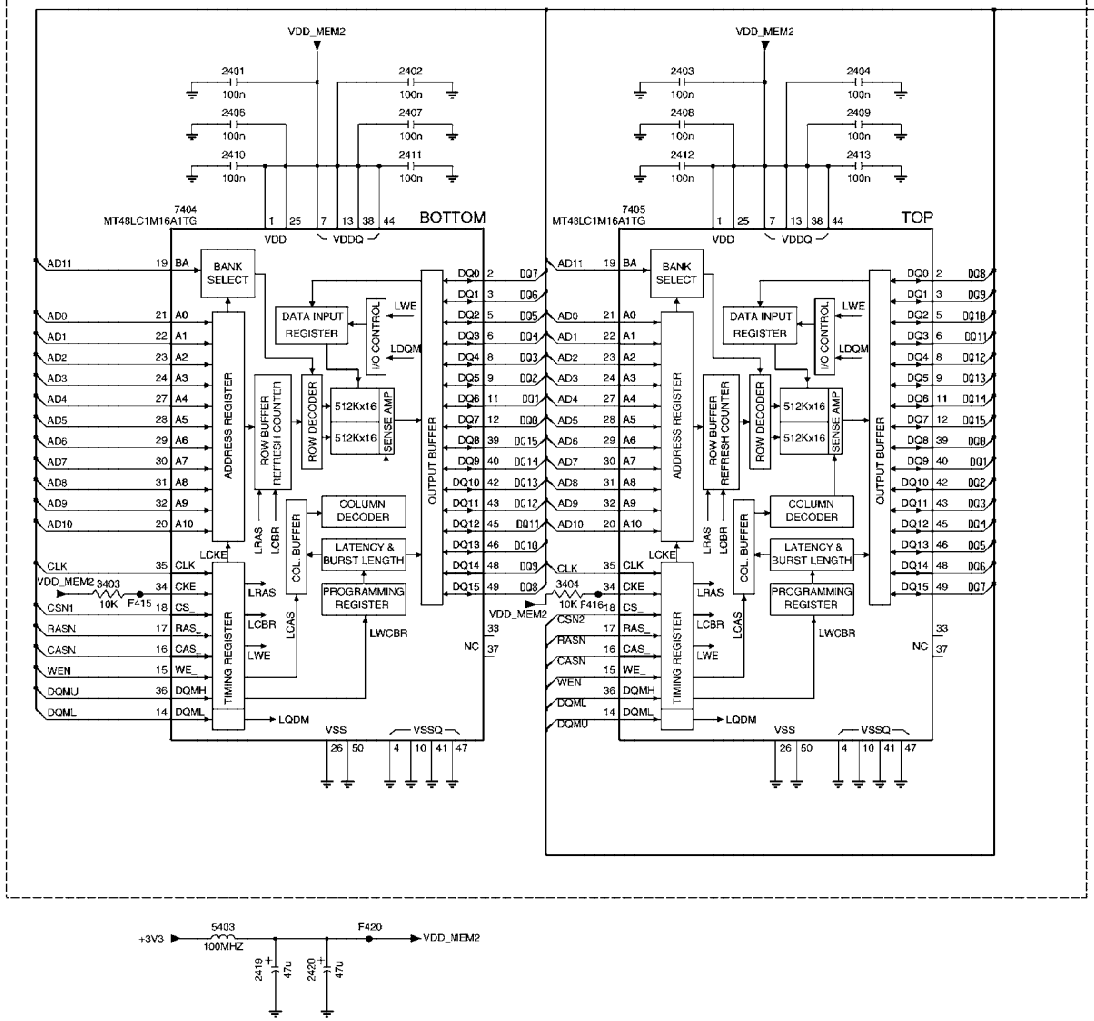
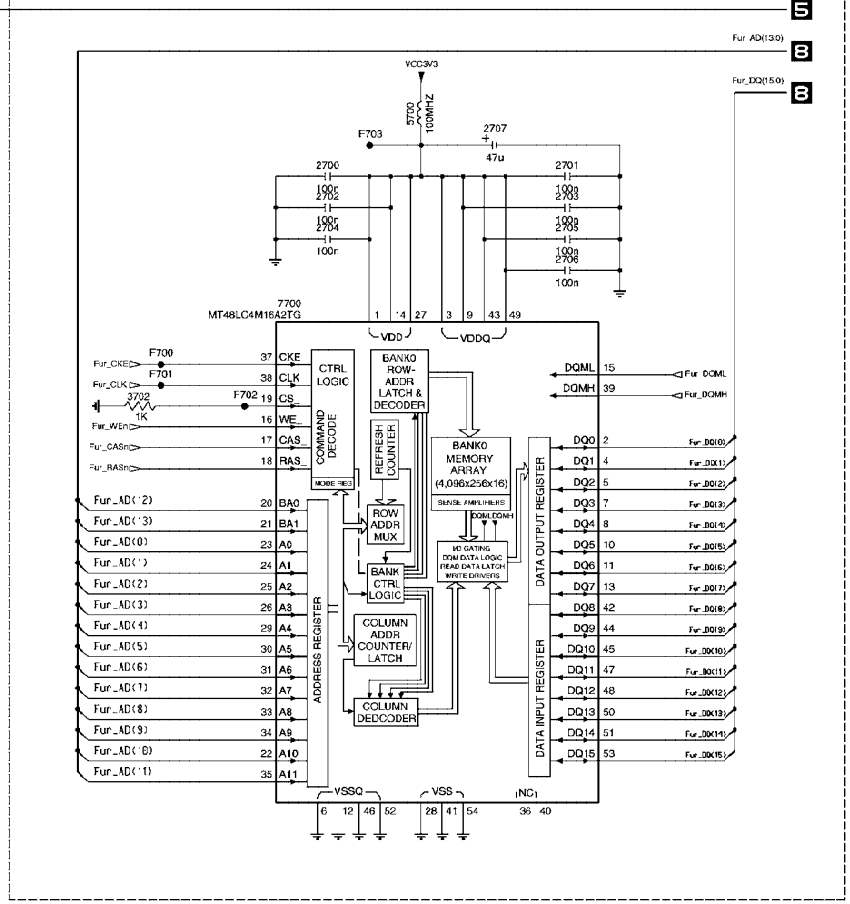
1602-3 A13	3661 G9	F671 I1
1602-4 B13	3662 G10	F672 I2
1602-5 B13	3663 G10	F673 I2
1602-6 B13	3664 G10	F674 I3
1602-7 A13	3665 E10	F675 F2
1603-1 E13	3667 E10	F921 A13
1603-10 C13	3672 E3	F922 A13
1603-11 C13	3674 D10	F923 A13
1603-12 D13	3676 E7	F924 A13
1603-13 D13	3686 H1	F925 B13
1603-14 E13	3687 I1	F926 B13
1603-15 E13	3688 I2	F927 G2
1603-16 E13	3689 I3	F928 G2
1603-17 D13	3690 I3	F929 H2
1603-18 E13	3691 D5	
1603-19 E13	4602 E5	
1603-2 F13	4603 E5	
1603-20 D13	4604 E5	
1603-21 E13	5600 A12	
1603-22 D13	5601 E6	
1603-3 F13	5602 F9	
1603-4 D13	5604 F9	
1603-5 F13	5605 G9	
1603-6 G13	5606 H9	
1603-7 D13	5607 I9	
1603-8 C13	5608 I9	
1603-9 C13	5609 B2	
1604 G13	5610 F2	
1605 G1	5611 D3	
1606 G1	6600 C9	
1607 G1	7600-A A11	
1608 H1	7600-B B11	
2600 A11	7600-C A11	
2601 A12	7600-D B11	
2602 B12	7600-E A9	
2603 B1	7600-F A8	
2604 D3	7604 B7	
2605 C8	7605 C2	
2606 C9	7607 B6	
2607 E2	7608 C10	
2608 C3	7609 C10	
2609 D1	7610 D10	
2610 E7	7611 F6	
2611 G2	7612 F10	
2614 F9	7613 F10	
2615 F9	7614 G10	
2616 G9	7615 H10	
2617 G9	7617 I10	
2620 G9	7618 I9	
2621 G9	7620 H2	
2622 H8	7621 I3	
2623 H9	7622 B2	
2624 I8	F600 A13	
2625 I9	F601 A13	
2626 I8	F602 A13	
2627 I9	F603 A12	
2632 C8	F604 B3	
2633 C8	F605 C1	
2634 D2	F606 A12	
2635 D2	F607 A13	
2636 D3	F608 C3	
2637 E2	F609 B6	
2638 E3	F610 B7	
2639 E4	F611 B13	
2640 F11	F612 B12	
2641 F11	F613 B12	
2642 F12	F614 D2	
2643 F12	F615 D2	
2644 F12	F616 B13	
2645 F13	F617 B7	
2646 B3	F618 E2	
2647 H11	F619 C10	
2648 H12	F620 C12	
2649 B2	F621 C6	
2650 C2	F622 C10	
3606 C10	F623 E2	
3607 A12	F624 C9	
3608 B11	F625 C12	
3609 B12	F626 D10	
3610 A12	F627 F3	
3611 B12	F628 E7	
3612 B6	F629 D9	
3613 B6	F630 D12	
3614 C6	F631 D2	
3615 C10	F632 B3	
3616 D12	F633 E12	
3617 D11	F634 E3	
3618 D8	F635 E11	
3619 D9	F636 E2	
3620 A12	F637 E11	
3621 B12	F638 E11	
3622 C9	F639 E8	
3623 E10	F640 E11	
3624 E10	F641 E11	
3625 E11	F643 F10	
3626 F10	F644 E11	
3627 B7	F646 F11	
3628 B7	F647 F9	
3629 C10	F648 F10	
3630 B7	F649 F11	
3631 F9	F651 G9	
3632 F10	F652 G9	
3633 G8	F653 G11	
3635 A12	F654 H8	
3636 B12	F655 H9	
3637 C11	F656 H13	
3642 B6	F657 H11	
3647 G8	F658 H13	
3648 H8	F659 H13	
3651 I8	F660 I8	
3654 I8	F661 I9	
3655 I9	F662 I10	
3656 I9	F663 I8	
3657 H9	F664 I9	

7 SDRAMs

ST SDRAM



FURORE SDRAM



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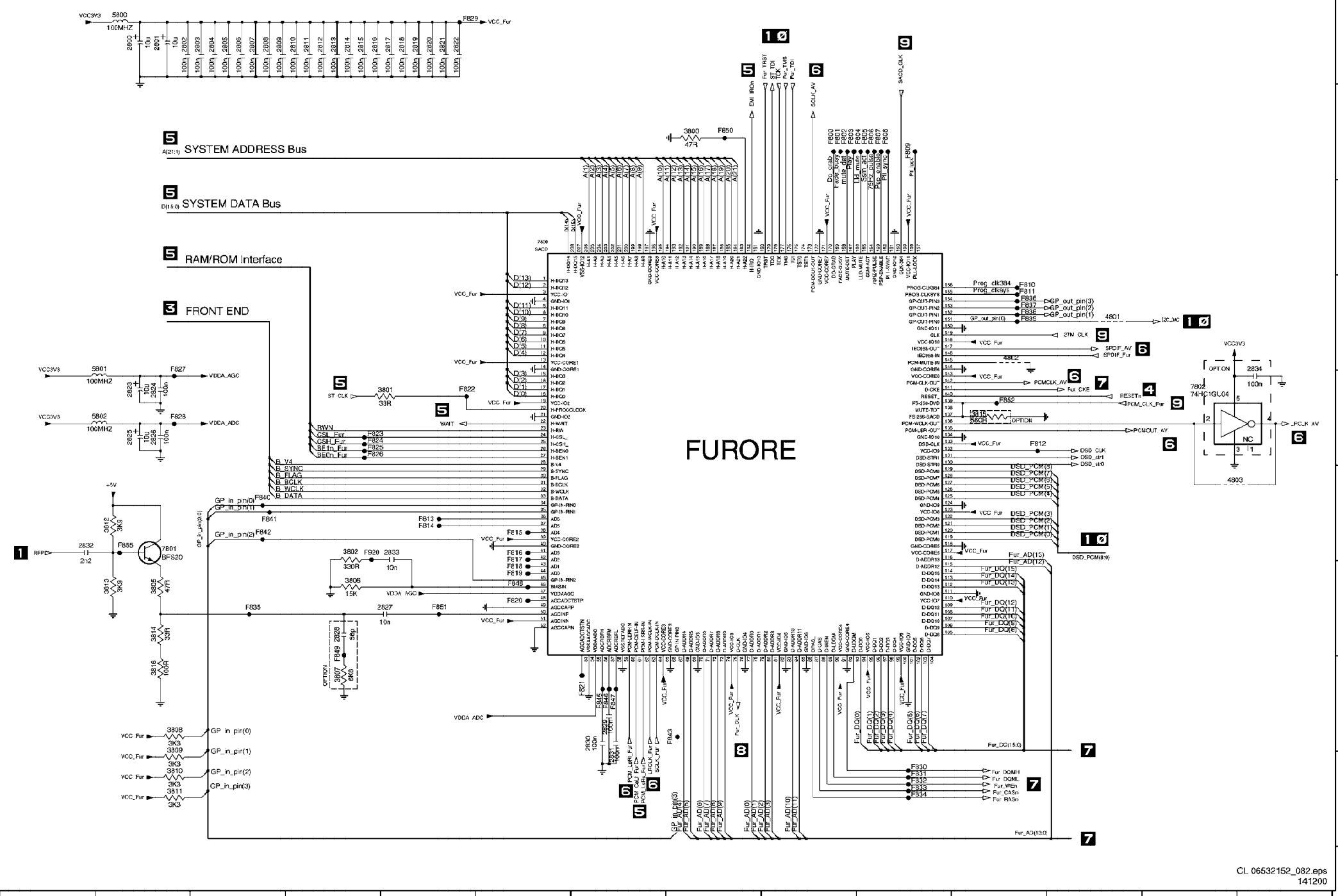
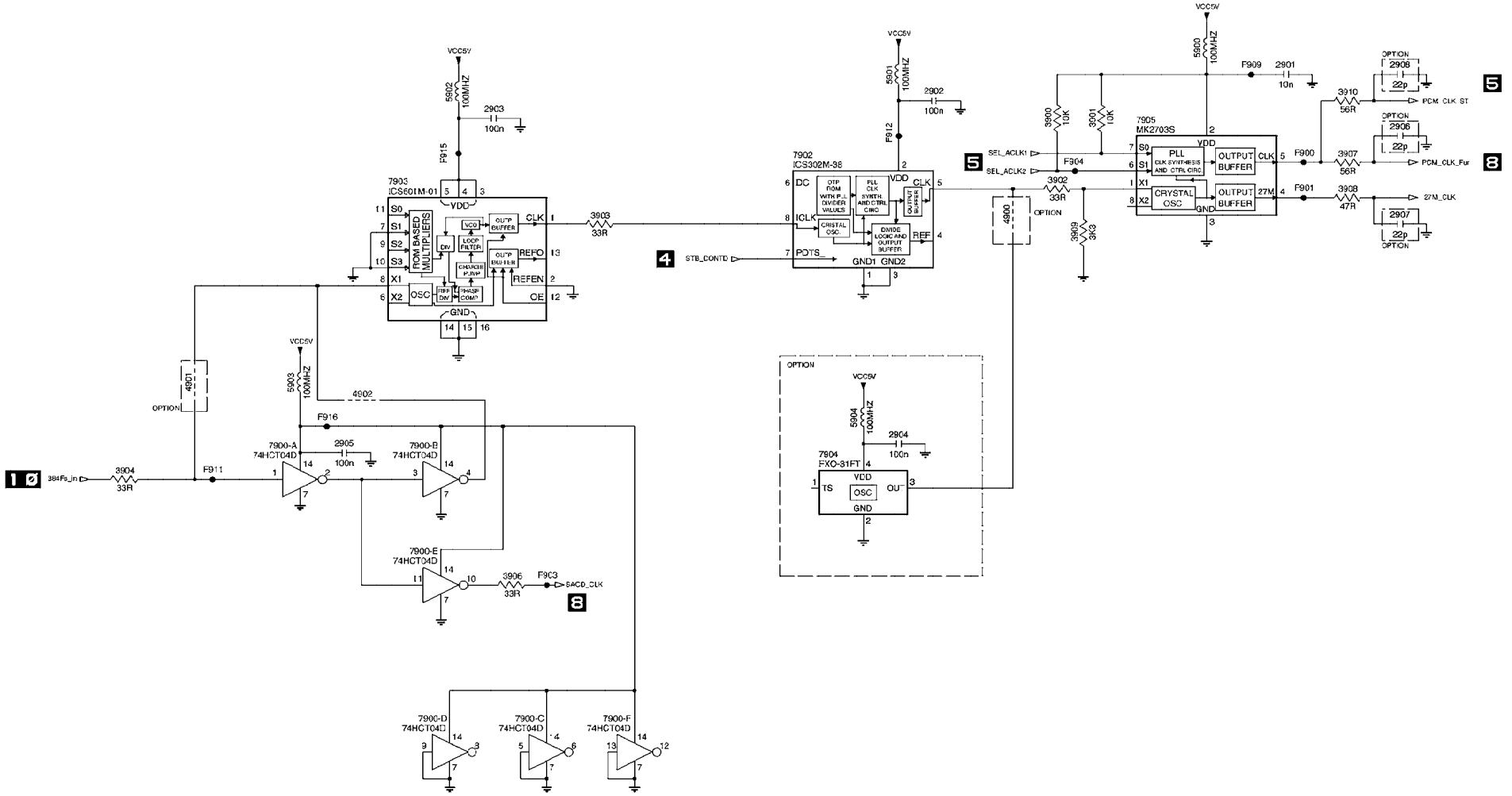
141200

8 SACD DECODER



9 SYSTEM CLOCKS



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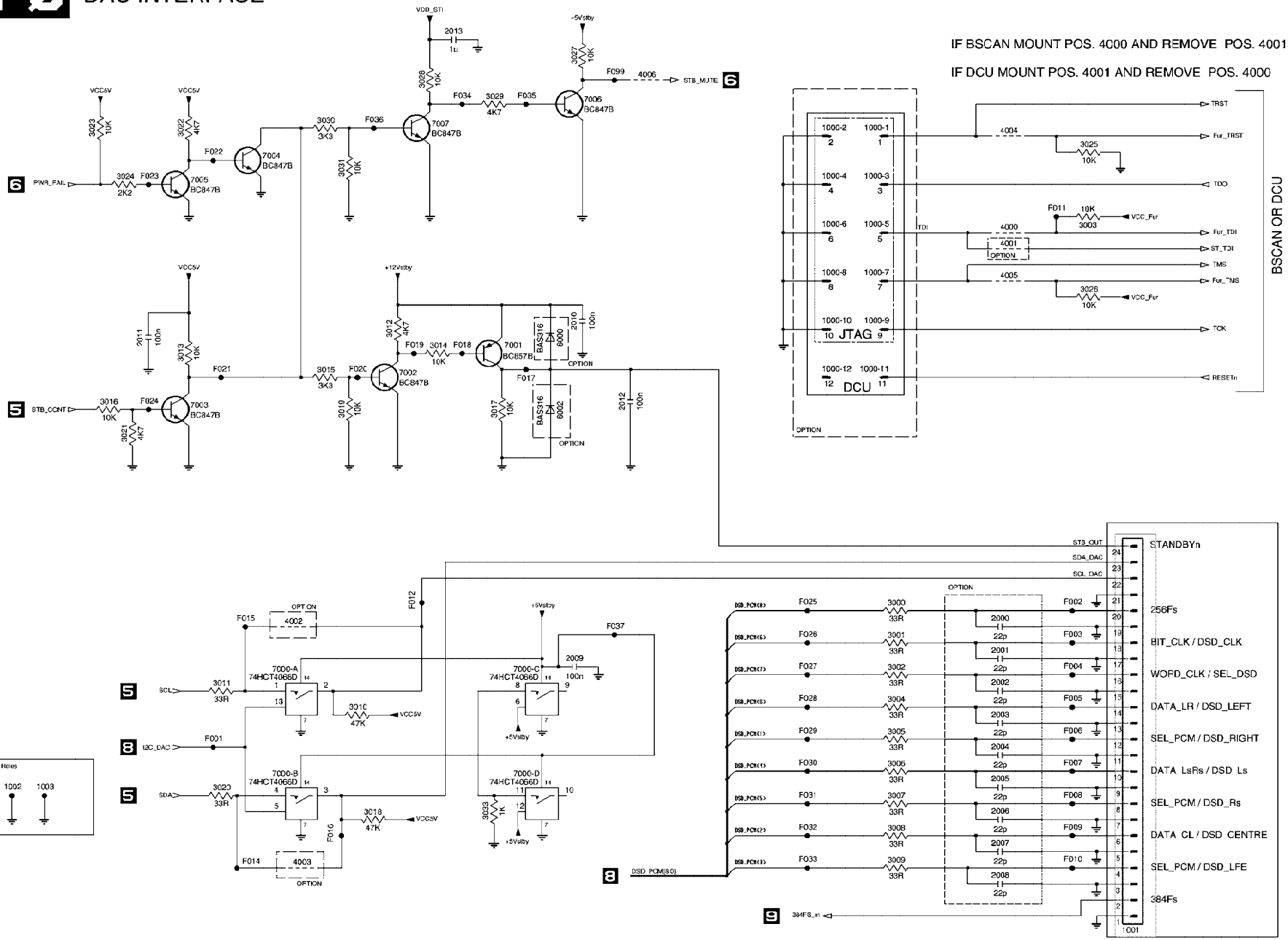
141200

2902 C9
2903 C5
2904 E8
2905 E4
2906 C12
2907 D12
2908 B12
3900 C10
3901 C10
3902 C10
3903 D6
3904 F2
3906 F5
3907 C12
3908 C12
3909 D10
3910 C12
4900 C9
4901 E3
4902 E4
5900 B11
5901 B8
5902 B5
5903 E3
5904 E8
7900-A E3
7900-B E4
7900-C H5
7900-D H4
7900-E F4
7900-F H6
7902 C7
7903 C4
7904 E8
7905 C10
F900 C12
F901 C12
F903 F5
F904 C10
F909 B11
F911 F3
F912 C8
F915 C5
F916 E4

DVD962SA(2020) - MONO SCHEMATIC DIAGRAM 9: SYSTEM CLOCKS

10 DAC INTERFACE



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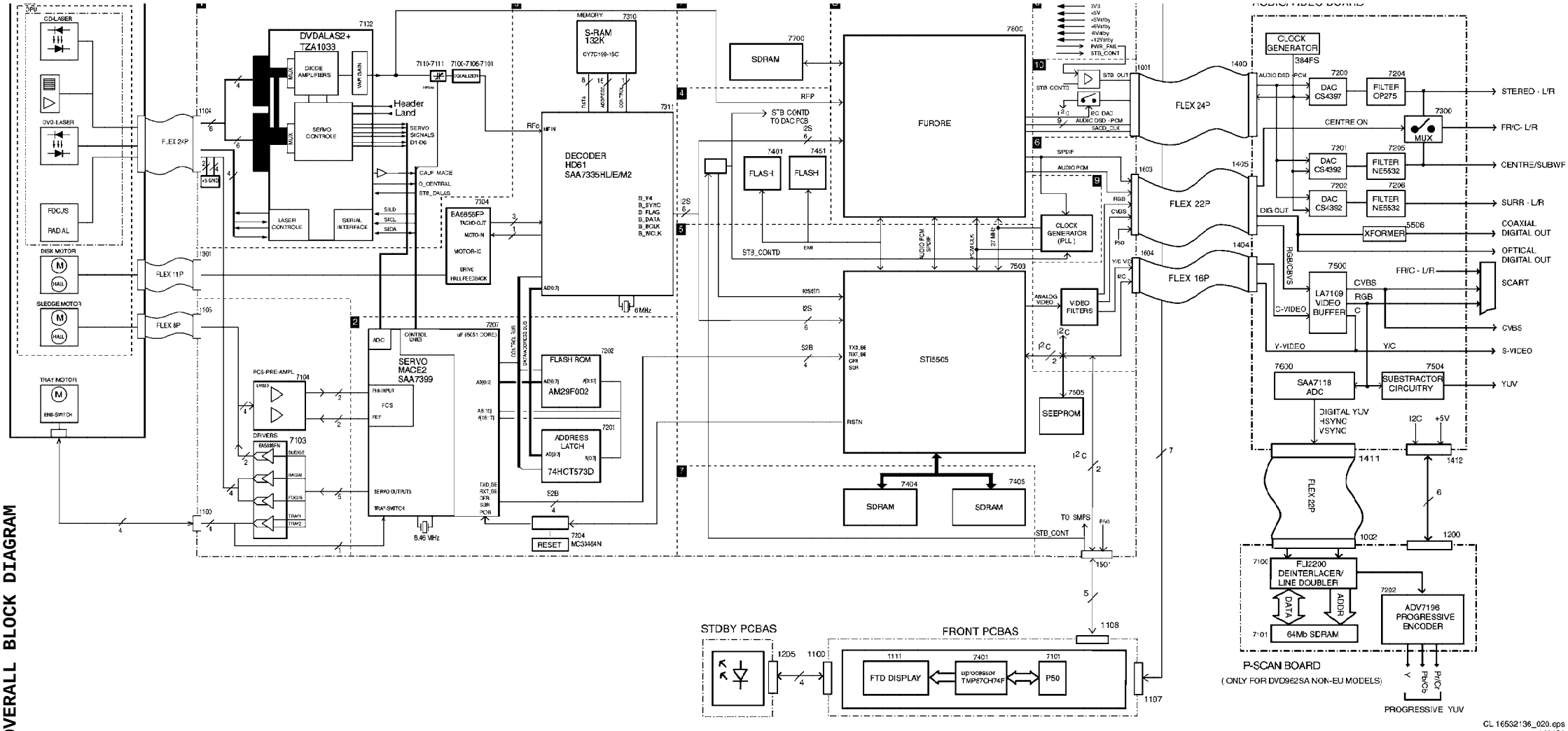
DVD962SA(2020) - MONO SCHEMATIC DIAGRAM 10: DAC INTERFACE



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