DVDR3355/02/05/19/51 & DVDR3365/02/05/19/51

Service
Service
Service

Back End Repair

Service Manual

CLASS 1 LASER PRODUCT

DVD + ReWritable

DVD VIDEO

COMPACT disc DIGITAL VIDEO

COMPACT disc DIGITAL AUDIO

Contents **Page**

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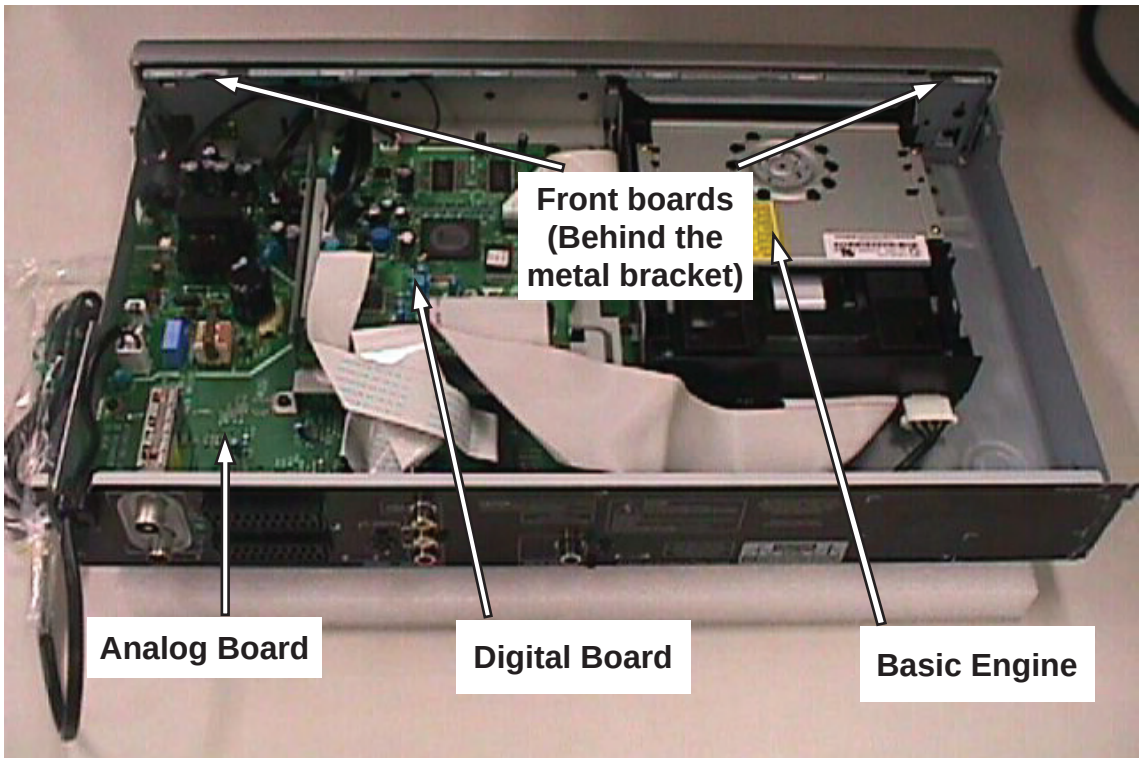
Version 1.1

PHILIPS

1. Technical Specifications and Connection Facilities

1.1 PCB Locations



1.2 General:

Mains voltage	:	220V – 240V
Mains frequency	:	50 Hz
Power consumption (typical)	:	25 W
Standby Power Consumption	:	< 4 W

1.3 RF Tuner

Test equipment: Fluke 54200 TV Signal generator
Test streams: PAL BG Philips Standard test pattern

1.3.1 System

PAL B/G, PAL D/K, SECAM L/L', PAL I

1.3.2 RF - Loop Through:

Frequency range	:	45 MHz – 860 MHz
Gain: (ANT IN - ANT OUT)	:	-6dB to 0dB

1.3.3 Receiver:

PLL tuning with AFC for optimum reception

Frequency range	:	45.25 MHz – 857 MHz
Sensitivity at 40dB S/N	:	≥ 60dBµV at 75 Ω (video unweighted)

1.3.4 Video Performance:

Channel 25 / 503,25 MHz,
Test pattern: PAL BG PHILIPS standard test pattern,
RF Level 74dBV
Measured on SCART 1

Frequency response	:	0.1 – 4.00 MHz ± 3dB
Group delay (0.1 MHz - 4.4 MHz)	:	0 nsec ± 150 nsec

1.3.5 Audio Performance:

Audio Performance Analogue - HiFi:

Frequency response at SCART 1 (L+R) output	:	100 Hz – 12 kHz / 0 ± 3dB
S/N according to DIN 45405, 7, 1967 and PHILIPS standard test pattern video signal	:	≥ 50dB, unweighted
Harmonic distortion (1 kHz, ± 25 kHz deviation)	:	≤ 1.5%

Audio Performance NICAM:

Frequency response at SCART 1 (L+R) output	:	40 Hz – 15 kHz / 0 ± 3dB
S/N according to DIN 45405,7,1967 and PHILIPS standard test pattern video signal	:	≥ 60dB, unweighted
Harmonic distortion (1kHz)	:	≤ 0.5%

1.3.6 Tuning

Automatic Search Tuning

Scanning time without antenna	:	typ. 3 min.
Stop level (vision carrier)	:	≥ 37dBµV
Maximum tuning error of a recalled program	:	± 62.5 kHz
Maximum tuning error during operation	:	± 100 kHz

Tuning Principle

Automatic B, G, I, DK and L/L' detection
Manual selection in "STORE" mode

1.4 Analogue Inputs / Outputs

1.4.1 SCART 1 (Connected to TV)

Pin Signals:

1	- Audio R	1.8V RMS
2	- Audio R	
3	- Audio L	1.8V RMS
4	- Audio GND	
5	- Blue / GND	
6	- Audio L	
7	- Blue out	
8	- Function switch	< 2V = TV > 4.5V / < 7V = asp. Ratio 16:9 DVD > 9.5V / < 12V = asp. Ratio 4:3 DVD
9	- Green GND	
10	- NC	
11	- Green	0.7Vpp ± 0.1V into 75Ω (*)
12	- NC	
13	- Red GND	
14	- Fast switch GND	
15	- Red out	0.7Vpp ± 0.1V into 75Ω (*)
16	- Fast switch RGB / CVBS	< 0.4V into 75Ω = CVBS >1V / < 3V into 75Ω = RGB
17	- CVBS GND OUT	
18	- CVBS GND IN	
19	- CVBS out	1Vpp ± 0.1V into 75Ω (*)
20	- CVBS in	
21	- Shield	

1.4.2 SCART 2 (Connected to AUX)

Pin Signals:

1	- Audio R	1.8V RMS
2	- Audio R	
3	- Audio L	1.8V RMS
4	- Audio GND	
5	- Blue GND	
6	- Audio L	
7	- Blue in	
8	- Function switch	
9	- Green GND	
10	- NC	
11	- Green in	
12	- NC	
13	- Red GND	
14	- Fast switch GND	
15	- Red in	
16	- Fast switch RGB / CVBS	
17	- CVBS GND OUT	
18	- CVBS GND IN	
19	- CVBS / RGB out sync	1Vpp ± 0.1V into 75Ω (*)
20	- CVBS in	
21	- Shield	

(*) for 100% white

1.4.3 Audio/Video Front Input Connectors

Audio - Cinch

Input voltage	:	2.2Vrms
Input impedance	:	> 10kΩ

Video - Cinch

Input voltage	:	1Vpp ± 3dB
Input impedance	:	75Ω

Video - YC (Hosiden)

According to IEC 933-5
Superimposed DC-level on pin 4 (load > 100kΩ)
< 2.4V is detected as 4:3 aspect ratio
> 3.5V is detected as 16:9 aspect ratio

Input voltage Y	:	1Vpp ± 3dB
Input impedance Y	:	75Ω
Input voltage C	:	burst 300mVpp ± 3dB
Input impedance C	:	75Ω

1.4.4 Audio/Video Output rear Connectors

Audio - Cinch

Output voltage	:	2Vrms max.
Output impedance	:	> 10kΩ

Video - Cinch

Output voltage	:	1Vpp ± 3dB
Output impedance	:	75Ω

Video - YC (Hosiden)

According to IEC 933-5
Superimposed DC-level on pin 4 (load > 100kΩ)
< 2.4V is detected as 4:3 aspect ratio
> 3.5V is detected as 16:9 aspect ratio

Output voltage Y	:	1Vpp ± 10/-15%
Output voltage C	:	300mVpp ± 1/-4dB

1.5 Video Performance

All outputs loaded with 75 Ω
SNR measurements over full bandwidth without weighting.

1.5.1 SCART (RGB)

SNR	:	> -65dB on all output
Bandwidth	:	4.8MHz ± 2dB

1.6 Audio Performance CD

1.6.1 Cinch Output Rear

Output voltage 2 channel mode	:	2Vrms ± 2dB
Channel unbalance (1kHz)	:	< 1dB
Crosstalk 1kHz	:	> 95dB
Crosstalk 16Hz-20kHz	:	> 87dB
Frequency response 20Hz-20kHz	:	± 0.2dB max
Signal to noise ratio	:	> 85dB
Dynamic range 1kHz	:	> 83dB
Distortion and noise 1kHz	:	> 83dB
Distortion and noise 16Hz-20kHz	:	> 75dB
Intermodulation distortion	:	> 70dB
Mute	:	> 95dB
Outband attenuation:	:	> 40dB above 30kHz

1.6.2 Scart Audio

Output voltage 2 channel mode	:	1.6Vrms ± 2dB
Channel unbalance (1kHz)	:	< 1dB
Crosstalk 1kHz	:	> 85dB
Crosstalk 16Hz-20kHz	:	> 70dB
Frequency response 20Hz-20kHz	:	± 0.2dB max
Signal to noise ratio	:	> 80dB
Dynamic range 1kHz	:	> 75dB
Distortion and noise 1kHz	:	> 75dB
Distortion and noise 16Hz-20kHz	:	> 50dB
Intermodulation distortion	:	> 70dB
Mute	:	> 80dB
Outband attenuation:	:	> 40dB above 25kHz

1.7 Digital Output

1.7.1 Coaxial

CDDA / LPCM (incl MPEG1)	:	according IEC958, IEC60958-1,-3
MPEG2, AC3 audio	:	according IEC1937, IEC61937
DTS	:	according IEC1937, IEC 61937 amendment 1

1.8 Digital Video Input (IEEE 1394)

1.8.1 Applicable Standards

Implementation according:
IEEE Std 1394-1995
IEC 61883 - Part 1
IEC 61883 - Part 2 SD-DVCR (02-01-1997)

Specification of consumer use digital VCR's using 6.3 mm magnetic tape - dec. 1994
Annex A of 61883-1

1.9 Dimensions and Weight

Height of feet	:	5.5mm
Apparatus tray closed	:	WxDxH:435x285x65mm
Apparatus tray open	:	WxDxH:435x422x65mm
Weight without packaging	:	app. 4.0kg ± 0.5kg
Weight with packaging	:	app. 6kg

1.10 Laser Output Power & Wavelength

1.10.1 DVD

Output power during reading	:	0.8mW
Output power during writing	:	20mW
Wavelength	:	660nm

1.10.2 CD

Output power	:	0.3mW
Wavelength	:	780nm

2. Safety Information, General Notes & Lead Free Requirements

2.1 Safety Instructions

2.1.1 General Safety

Safety regulations require that during a repair:
- Connect the unit to the mains via an isolation transformer.
- Replace safety components, indicated by the symbol ⚠, only by components identical to the original ones. Any other component substitution (other than original type) may increase risk of fire or electrical shock hazard.

Safety regulations require that after a repair, you must return the unit in its original condition. Pay, in particular, attention to the following points:
- Route the wires/cables correctly, and fix them with the mounted cable clamps.
- Check the insulation of the mains lead for external damage.
- Check the electrical DC resistance between the mains plug and the secondary side:
  1. Unplug the mains cord, and connect a wire between the two pins of the mains plug.
  2. Set the mains switch to the 'on' position (keep the mains cord unplugged!).
  3. Measure the resistance value between the mains plug and the front panel, controls, and chassis bottom.
  4. Repair or correct unit when the resistance measurement is less than 1 MΩ.
  5. Verify this, before you return the unit to the customer/ user (ref. UL-standard no. 1492).
  6. Switch the unit 'off', and remove the wire between the two pins of the mains plug.

2.1.2 Laser Safety

This unit employs a laser. Only qualified service personnel may remove the cover, or attempt to service this device (due to possible eye injury).

Laser Device Unit

Type	:	Semiconductor laser GaAlAs
Wavelength	:	650 nm (DVD)
	:	780 nm (VCD/CD)
Output Power	:	20 mW (DVD+RW writing)
	:	0.8 mW (DVD reading)
	:	0.3 mW (VCD/CD reading)
Beam divergence	:	60 degree

Figure 2-1

Note: Use of controls or adjustments or performance of procedure other than those specified herein, may result in hazardous radiation exposure. Avoid direct exposure to beam.

2.2 Warnings

2.2.1 General

- All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD, ⚠). Careless handling during repair can reduce life drastically. Make sure that, during repair, you are at the same potential as the mass of the set by a wristband with resistance. Keep components and tools at this same potential.
  Available ESD protection equipment:
  – Complete kit ESD3 (small tablemat, wristband, connection box, extension cable and earth cable) 4822 310 10671.
  – Wristband tester 4822 344 13999.
- Be careful during measurements in the live voltage section. The primary side of the power supply, including the heatsink, carries live mains voltage when you connect the player to the mains (even when the player is 'off'!). It is possible to touch copper tracks and/ or components in this unshielded primary area, when you service the player. Service personnel must take precautions to prevent touching this area or components in this area. A 'lightning stroke' and a stripe-marked printing on the printed wiring board, indicate the primary side of the power supply.
- Never replace modules, or components, while the unit is 'on'.

2.2.2 Laser

- The use of optical instruments with this product, will increase eye hazard.
- Only qualified service personnel may remove the cover or attempt to service this device, due to possible eye injury.
- Repair handling should take place as much as possible with a disc loaded inside the player.
- Text below is placed inside the unit, on the laser cover shield:

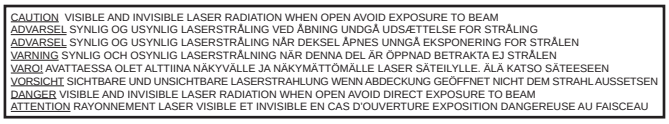


Figure 2-2

2.2.3 Notes

Dolby

Manufactured under licence from Dolby Laboratories. "Dolby", "Pro Logic" and the double-D symbol are trademarks of Dolby Laboratories. Confidential Unpublished Works.

Figure 2-3

Trusurround

TRUSURROUND, **SRS** and symbol (fig 2-4) are trademarks of SRS Labs, Inc. TRUSURROUND technology is manufactured under licence frm SRS labs, Inc.

Figure 2-4

Video Plus
"Video Plus+" and "PlusCode" are registered trademarks of the Gemstar Development Corporation. The "Video Plus+" system is manufactured under licence from the Gemstar Development Corporation.

Figure 2-5

Macrovision
This product incorporates copyright protection technology that is protected by method claims of certain U.S. patents and other intellectual property rights owned by Macrovision Corporation and other rights owners.
Use of this copyright protection technology must be authorized by Macrovision Corporation, and is intended for home and other limited viewing uses only unless otherwise authorized by Macrovision Corporation. Reverse engineering or disassembly is prohibited.

2.3 Lead Free Requirement

Information about Lead-free produced sets

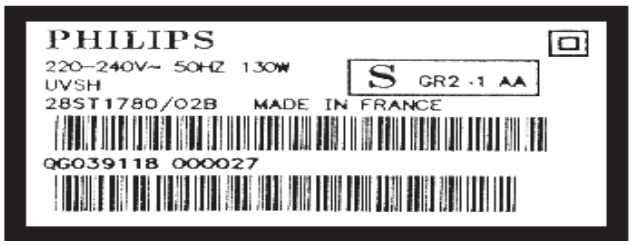
Philips CE is starting production of lead-free sets from 1.1.2005 onwards.

INDENTIFICATION:

Regardless of special logo (not always indicated)

One must treat all sets from **1 Jan 2005** onwards, according next rules.

Example S/N:



Bottom line of typeplate gives a 14-digit S/N. Digit 5&6 is the year, digit 7&8 is the week number, so in this case 1991 wk 18

So from 0501 onwards = from 1 Jan 2005 onwards

Important note: In fact also products of year 2004 must be treated in this way as long as you avoid mixing solder-alloys (leaded/ lead-free). So best to always use SAC305 and the higher temperatures belong to this.

Due to lead-free technology some rules have to be respected by the workshop during a repair:

- Use only lead-free solder alloy Philips SAC305 with order code 0622 149 00106. If lead-free solder-pate is required, please contact the manufacturer of your solder-equipment. In general use of solder-paste within workshops should be avoided because paste is not easy to store and to handle.
- Use only adequate solder tools applicable for lead-free solder alloy. The solder tool must be able
  - o To reach at least a solder-temperature of 400°C,
  - o To stabilize the adjusted temperature at the solder-tip
  - o To exchange solder-tips for different applications.
- Adjust your solder tool so that a temperature around 360°C – 380°C is reached and stabilized at the solder joint. Heating-time of the solder-joint should not exceed ~ 4 sec. Avoid temperatures above 400°C otherwise wear-out of tips will rise drastically and flux-fluid will be destroyed. To avoid wear-out of tips switch off un-used equipment, or reduce heat.
- Mix of lead-free solder alloy / parts with leaded solder alloy / parts is possible but PHILIPS recommends strongly to avoid mixed solder alloy types (leaded and lead-free). If one cannot avoid or does not know whether product is lead-free, clean carefully the solder-joint from old solder alloy and re-solder with new solder alloy (SAC305).
- Use only original spare-parts listed in the Service-Manuals. Not listed standard-material (commodities) has to be purchased at external companies.
- Special information for BGA-ICs:
  - always use the 12nc-recognizable soldering temperature profile of the specific BGA (for de-soldering always use the lead-free temperature profile, in case of doubt)
  - lead free BGA-ICs will be delivered in so-called 'dry-packaging' (sealed pack including a silica gel pack) to protect the IC against moisture. After opening, dependent of MSL-level seen on indicator-label in the bag, the BGA-IC possibly still has to be baked dry. (MSL=Moisture Sensitivity Level). This will be communicated via AYS-website.
  Do not re-use BGAs at all.

- For sets produced before 1.1.2005 (except products of 2004), containing leaded solder-alloy and components, all needed spare-parts will be available till the end of the service-period. For repair of such sets nothing changes.

- On our website **www.atyourservice.ce.Philips.com** you find more information to:

  - BGA-de-/soldering (+ baking instructions)
  - Heating-profiles of BGAs and other ICs used in Philips-sets

  You will find this and more technical information within the "magazine", chapter "workshop news".

For additional questions please contact your local repair-helpdesk.

3. Directions For Use

The following except of the Quick Use Guide serves as an introduction to the set.
The Complete Direction for the Use can be downloaded in different languages from the internet site of Philips Customer care Center:
www.p4c.philips.com

QUICK START GUIDE

1 what's in the box

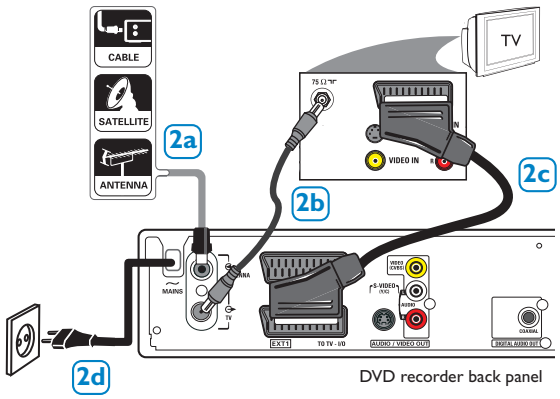
Ⓐ **Main Unit**

Ⓑ **Remote Control**
includes 2x AA batteries

Ⓒ **RF coaxial cable**

Ⓓ **Scart cable**

2 connect DVD recorder



DVD recorder back panel

2a Connect existing antenna cable/satellite signal (or from the Cable/Satellite Box [RF OUT or TO TV]) to the **ANTENNA** input socket at the back of the DVD recorder.

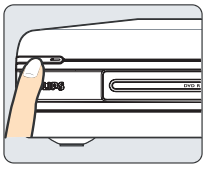
2b Use the supplied RF coaxial cable to connect the DVD recorder's **TV** output socket to your TV's antenna input socket.

2c Use the supplied Scart cable to connect the DVD recorder's **EXT 1 TO TV-I/O** socket to the matching SCART input socket at the back of your TV.

2d Connect the power cable from the DVD recorder's **~ MAINS** to the AC power outlet.

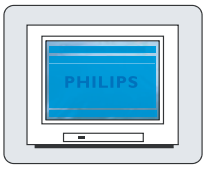
Helpful Hint:
For additional connection diagrams, see User Manual pages 12~19.

3 Start initial setup

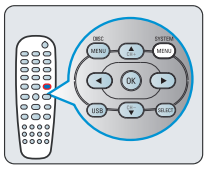


3a Press **STANDBY-ON** ⏻ on the DVD recorder to turn it on.

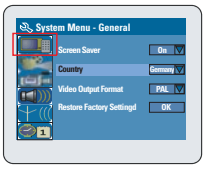
Note: *For successful installation, your cable/satellite box must be turned on.*



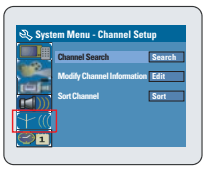
3b Turn on the TV to the correct programme channel for the input socket ('EXT','0','AV').
➜ The blue PHILIPS DVD background screen will appear on the TV.



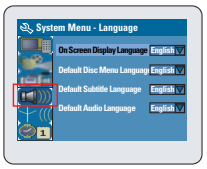
3c Press **SYSTEM MENU** on the remote control.
➜ Use ▲▼ keys to go through the menu. Select an item by pressing ▶, and confirm a setting by pressing **OK**.



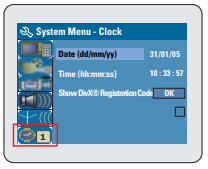
3d Highlight and press ▶.
Select the country of your residence..
Select { **Country** } and press **OK** on the remote control.



3e Highlight and press ▶.
Setup and install TV channels.
Select { **Channel Search** } and press **OK** on the remote control to start automatic TV channel search.



3f Highlight and press ▶.
Select the language.
- select TV On-Screen Display language.
- select default Disc Menu language.
- select default subtitle language.
- select default audio language.



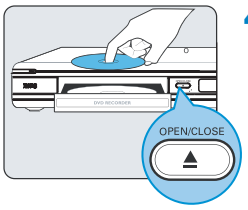
3g Highlight and press ▶.
Set the Date and Time.
Use the **numeric keypad 0-9** to input the date/time, then press **OK** to confirm.

3h Press **SYSTEM MENU** to exit.

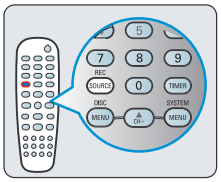
The DVD recorder is ready for use!

See next page for basic recording and playback.

4 start manual recording

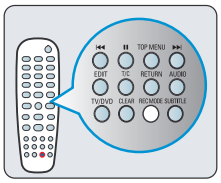


4a Insert a recordable DVD+R/+RW with the label facing up.



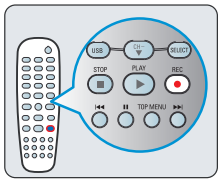
4b To record TV programme, press **REC SOURCE** to select { Tuner }.

To record from an external device connected to this DVD Recorder, press **REC SOURCE** repeatedly to select the corresponding external input channel : { Front CVBS } { Front S-Video }, { DV }, { EXT 2 }.

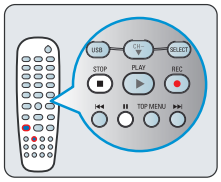


4c Press **REC MODE** to select a desired recording mode.
It defines the picture quality and the maximum recording time for a disc.

Maximum Recording Time per Disc	Picture Quality	Record Mode
1 hour	High quality	1 Hour Mode
2 hours	DVD quality-Standard Play	2 Hour Mode
4 hours	VHS quality-Extended Play	4 Hour Mode
6 hours	VHS quality-Super Long Play	6 Hour Mode



4d Press **REC ●** to start recording.

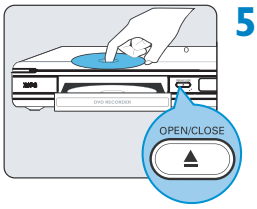


4e To pause the recording, press **II**.
To resume recording, press **REC ●**.

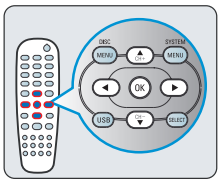
To stop the recording, press **STOP ■**.
➜ Wait until the message disappears from the display panel before you remove the disc.

5 start playback

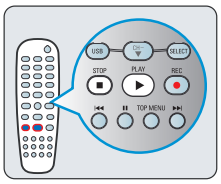
To playback a disc



5a Insert a disc with the label side facing up.

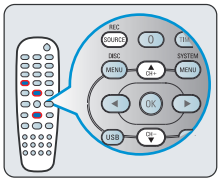


5b Playback may start automatically. If not, press **PLAY ▶**.
➜ If a disc menu appears, use ◀ ▶ ▲ ▼ keys to navigate within the menu, highlight a title and press **OK** to start playback.



5c To stop playback, press **STOP ■**.

To watch the TV programmes



5d Press **REC SOURCE** to select { Tuner }, then use ▲ ▼ keys to select the programme number.

GET PICTURE

- Check the AV mode on TV. It may be called FRONT, A/V IN, or VIDEO. Choose the different modes using TV remote control.
- Or, use the TV remote control to select Channel 1 on TV, then press Channel down button until you get the picture.
- See your TV manual for more details.

GET SOUND

- Use the supplied scart cable to connect the DVD recorder to your TV, the picture and sound will output through the TV.
- Or, connect the AUDIO L/R (red/white) sockets at the back of the DVD recorder to the corresponding AUDIO input sockets on a TV, stereo system or receiver. Turn on the connected system and select the appropriate channel.

Be responsible
Respect copyrights

4. Mechanical Instructions

4.1 Dismantling and Assembly of the Set

For item numbers please see the exploded view in Chapter 9.

4.1.1 Dismantling of the DVD Loader Tray Cover

1) Inserting a minus screw driver and push the lever in the direction as shown in Figure 4-1 to unlock the tray before sliding it out.

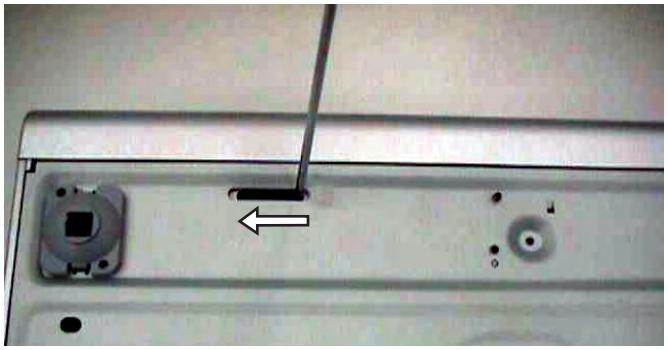


Figure 4-1

2) Remove the Tray Cover as shown in Figure 4-2.

Figure 4-2

4.1.2 Dismantling of the Front Panel Assembly

1) Remove the 3 screws 188 and release the 2 snap hooks on the side before removing the front assembly.

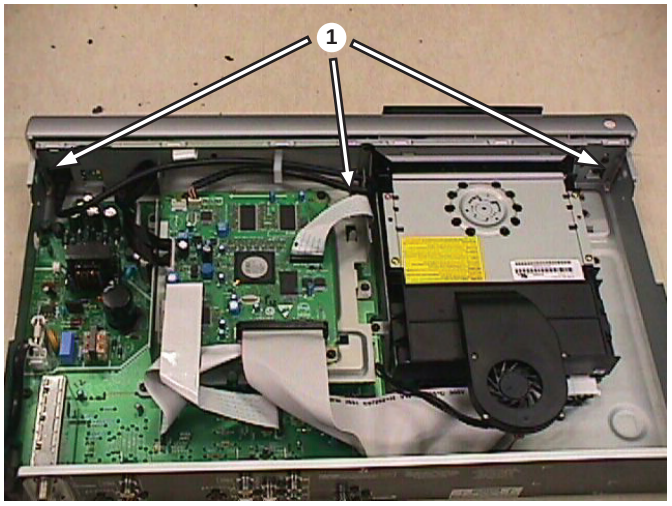


Figure 4-3

2) Remove the 5 screws 186 to remove the front plate 184 as shown in Figure 4-4.

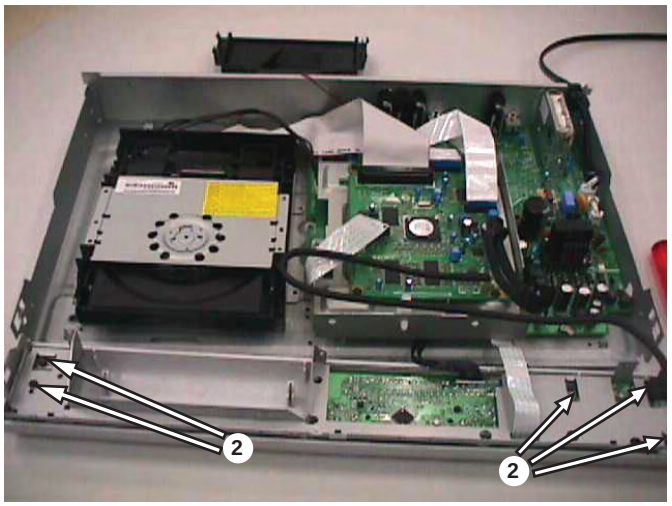


Figure 4-4

4.1.3 Dismantling of the Basic Engine

1) Remove the Cover Tray (See 4.1.1).

2) Remove the 4 screws 260 to free the Basic Engine.

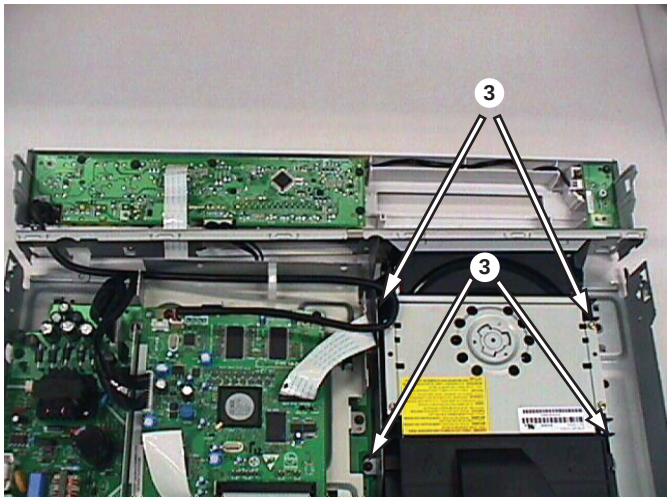


Figure 4-5

3) Place the Basic Engine in the service position by flipping the basic engine to the vertical position

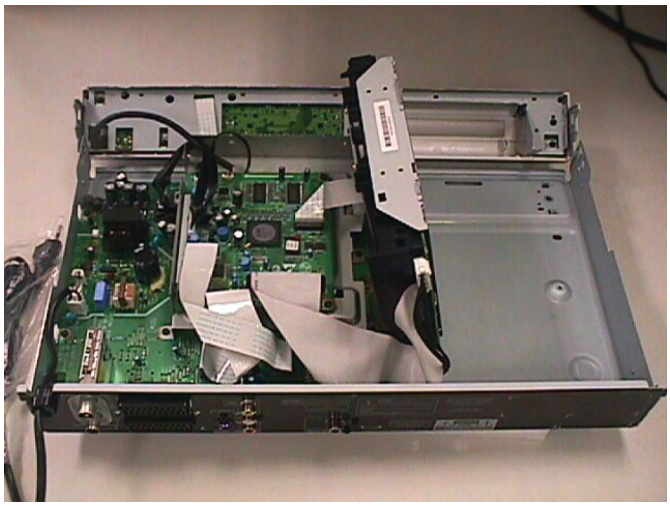


Figure 4-6

4.1.4 Dismantling of the Digital Board

1) Remove the 4 screws 272 to loose the Digital Board as shown in Figure 4-7.

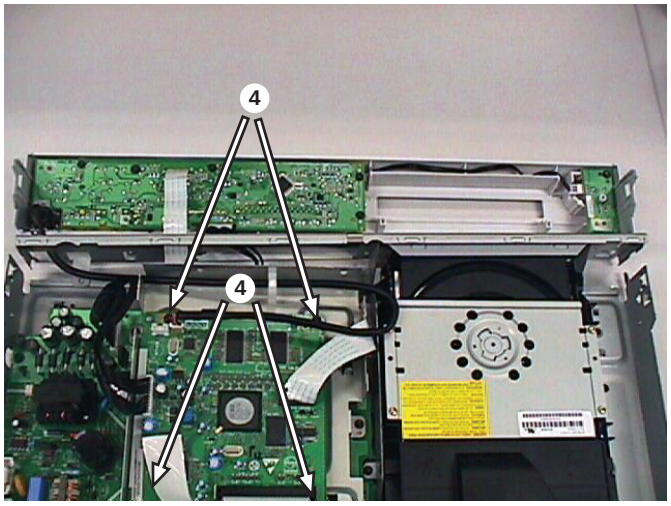


Figure 4-7

2) Service Position can be achieved by flipping the Digital board to the Vertical Position as shown in Figure 4-8.

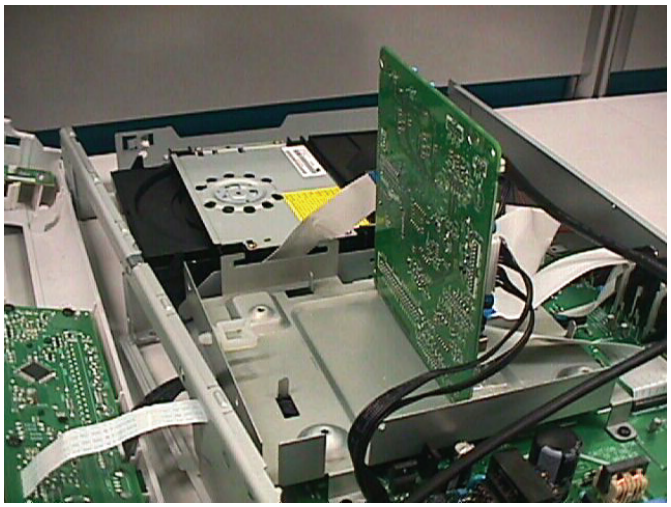


Figure 4-8

Note: The cable (just to transfer the service connection to the analog board) from socket 1101 can be removed and use for hyperterminal connection.

4.1.5 Dismantling of the Analog Board

1) Remove 5 screws 244 and 4 screws 252 and screw 230.

2) Remove 4 screws 270 and 3 screws 268.

3) Service Position can be achieved by flipping the analog board to the Vertical Position as shown in Figure 4-9.

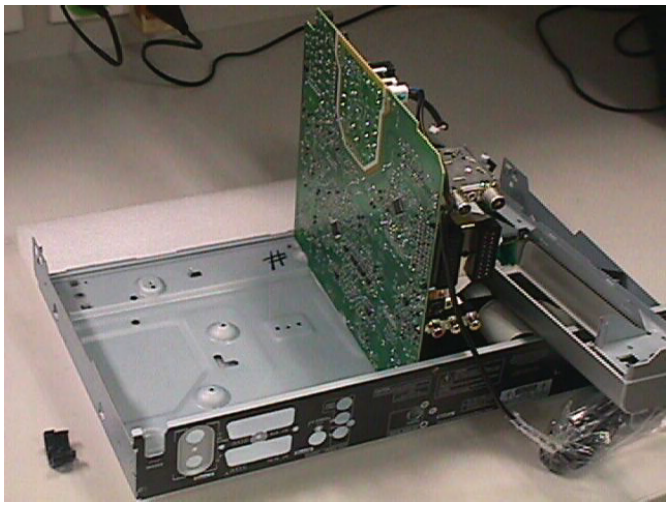


Figure 4-9

Note: Please cover the Live Area during trouble-shooting. (Figure 4-10)

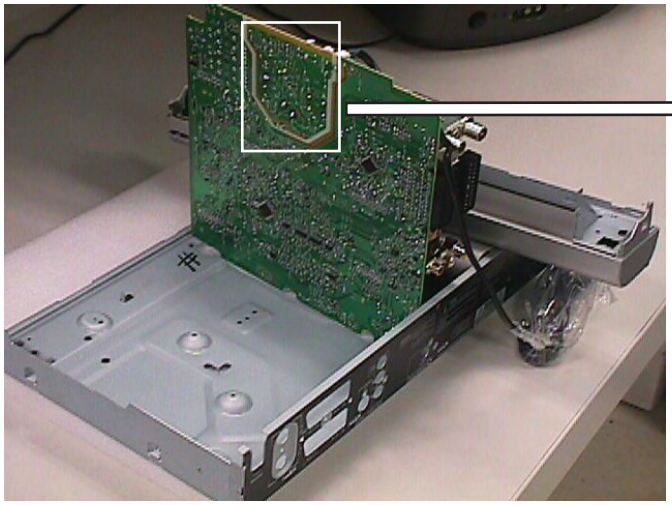


Figure 4-10

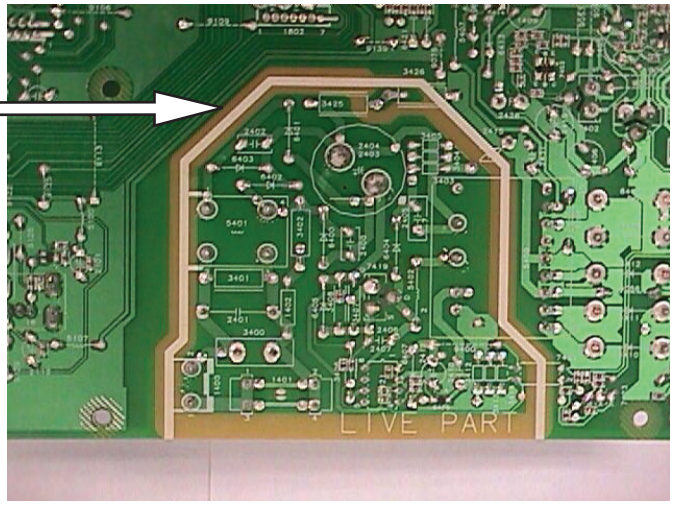


Figure Live Area

5. Upgrade Software & Repair Chart

5.1 Upgrade Software

A. Preparation to upgrade firmware:

1. Unzip the zip-archive file
2. Start the CD Burning software and create a new CD project (data disc) with the following settings:

   File system : Joliet
   Format : MODE 1: CDROM
   Recording mode : SINGLE SESSION (TRACK-AT-ONCE), FINALIZED CD

   Note: Long file name is necessary for the preparation of the upgrade disc

3. Place the content of the zip-archive into the root directory of the new CD project.
4. Burn the data onto a blank CDR or CD-RW

B. Procedure to apply the firmware upgrade:

1. Power up the set and open tray.
2. Insert the prepared Upgrade CDROM and close the tray.
3. The TV connected to the set will display:

   Software Upgrade Disc detected
   Select OK to start or CANCEL to exit

4. Select OK or CANCEL with the <Right> or <Left> button and press <OK> button to confirm.
5. The TV connected to the set will display:

   Upgrading Software, Please wait
   Do not switch off the power

6. When the upgrading process is successful the tray will open and the TV connected to the set will display:

   System is successfully upgraded.
   Remove disc from tray & reset system

7. Remove the Upgrade Disc and press <OK> button on Remote control to confirm
8. The TV screen goes blank and the Philips Logo screen appear again after the tray door has closed.

C. How to Restore Factory setting (Default setting)

1. Power up the set and with no disc in the tray
2. Press <System Menu> <Right> and 4x <Down> buttons on the Remote control to reach the Restore Factory setting option.
3. Press <OK> button and the TV connected to the set will display:

   System will reset to the Factory settings.
   Select OK to confirm or CANCEL to exit.

4. Select OK or CANCEL with the <Right> or <Left> button and press <OK> button to confirm.

   Note: All customers' settings will be lost.

D. How to read out the firmware version to confirm set has been upgraded.

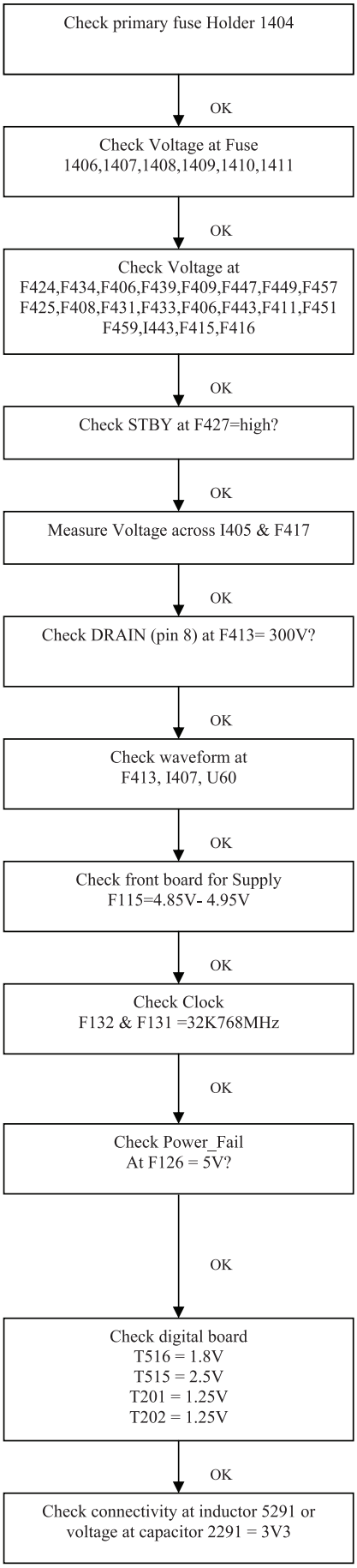
1. Power up the set and with no disc in the tray
2. Press <0009> and <OK> buttons on the Remote control
3. The TV connected to the set will display:

   DVDR3365_75_BT3_2, Drive: 43.02.11 Build: FAE6206 Apr 21 2005, 18:49:43

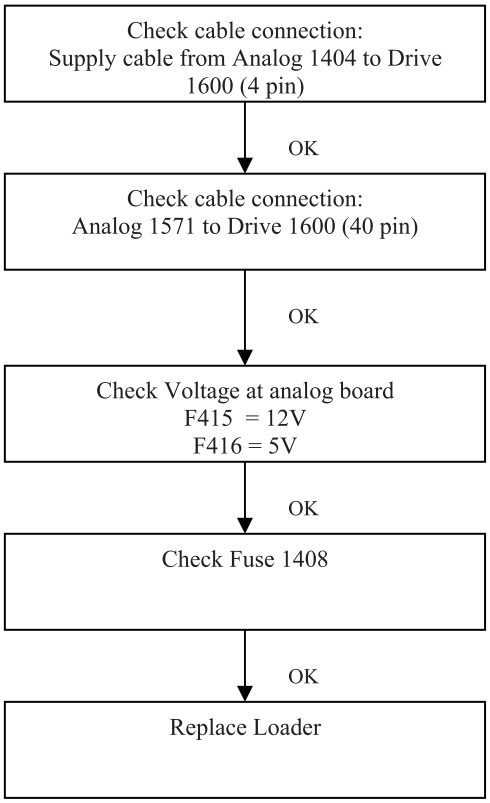
   where DVDR3365_75 = Type/version
   BT3_2 = Application (Backend) firmware version
   43.02.11 = Drive (Basic Engine) firmware version

5.2 Repair Chart

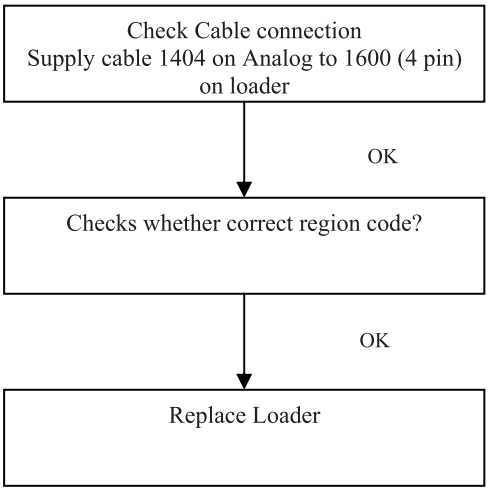
5.2.1 Completely Dead Set



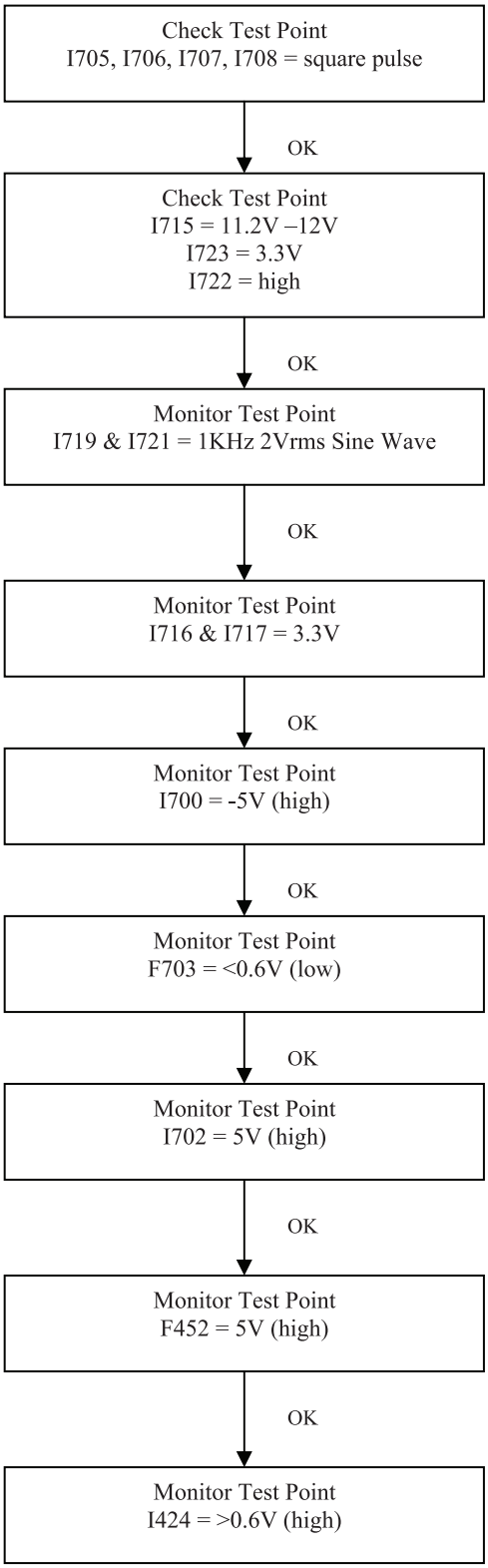
5.2.2 Cannot Read Disk



5.2.3 Disk Unknown

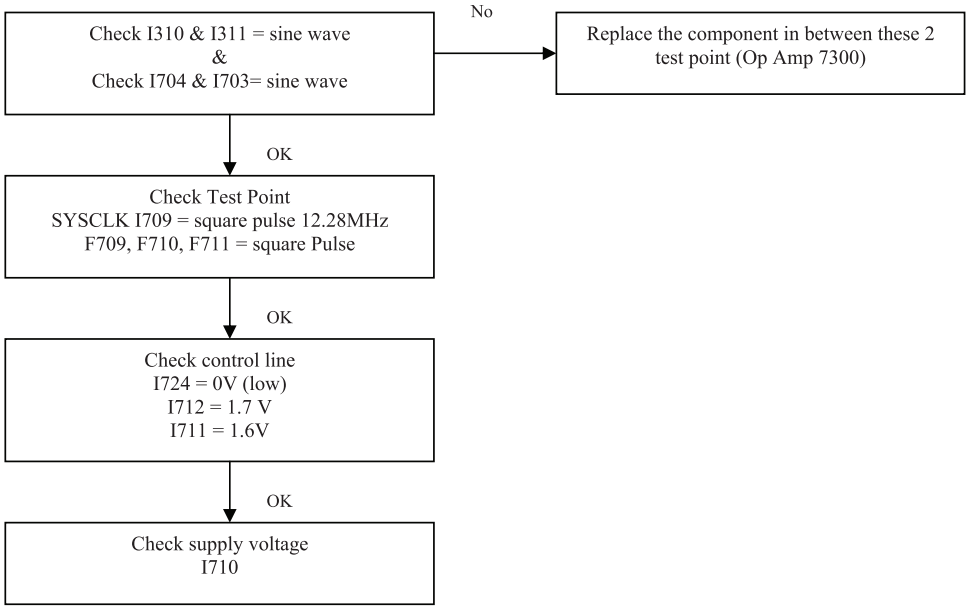


5.2.4 Audio No Sound (Playback)



5.2.5 Audio No Sound (TV & External Source)

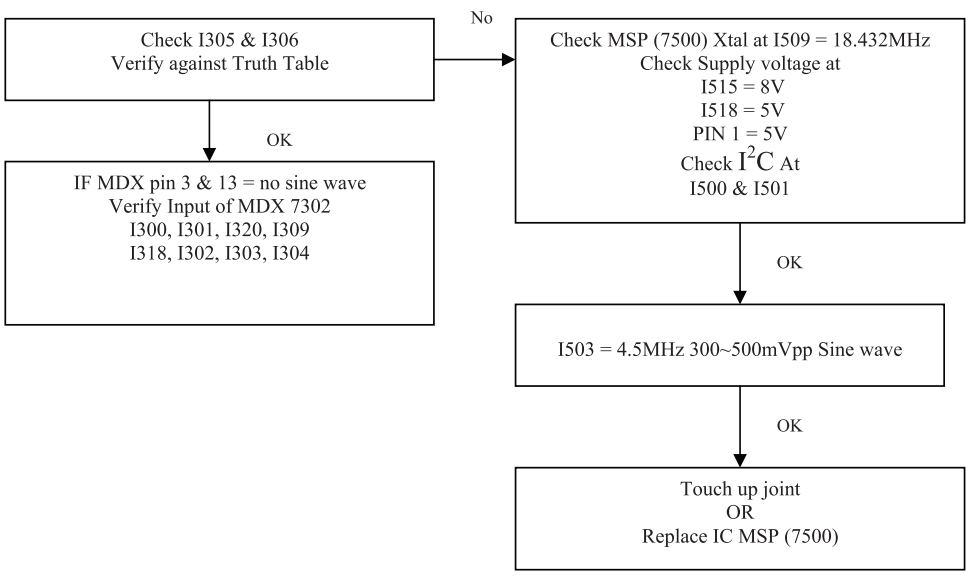
Part 1



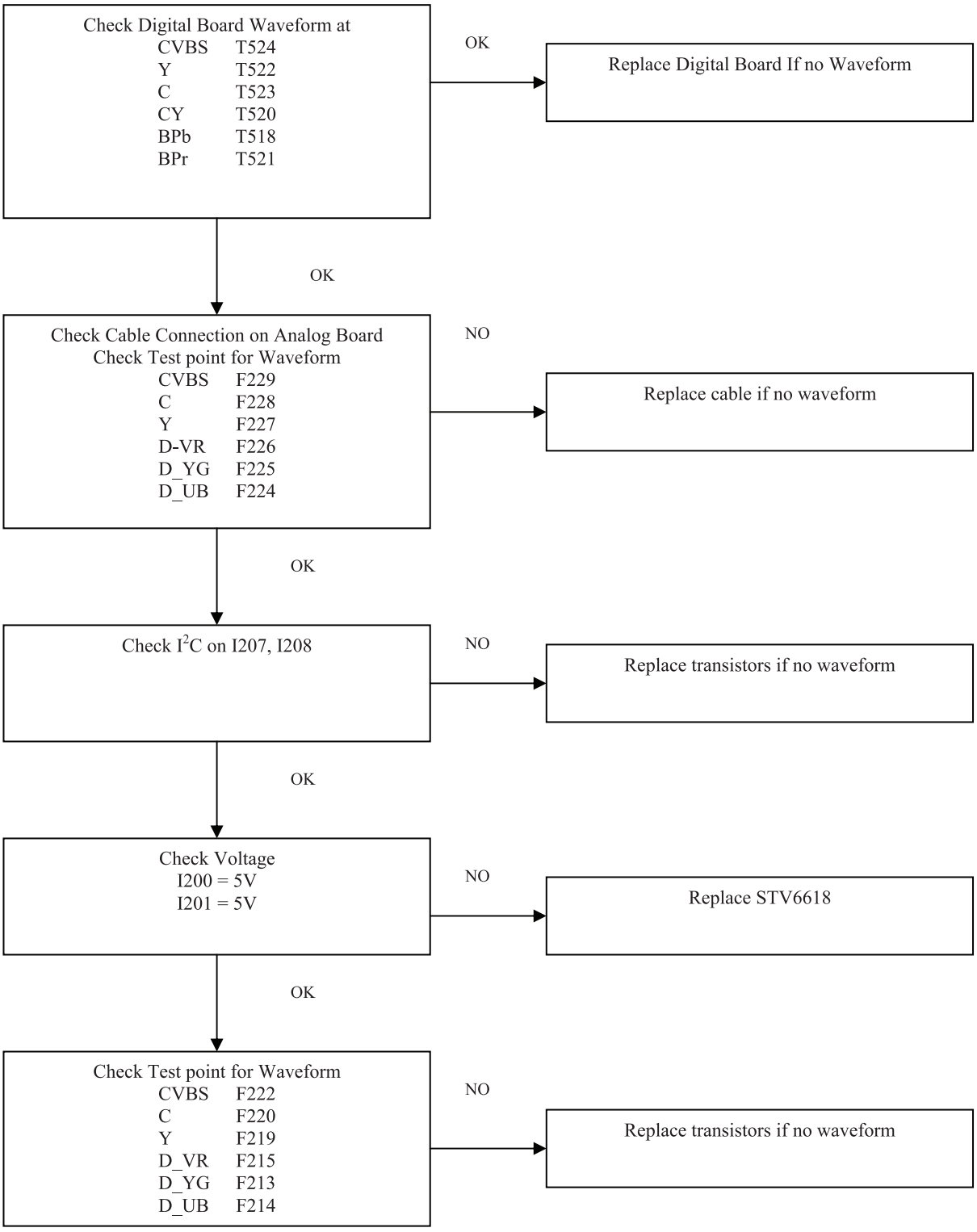
Part 2

Truth Table

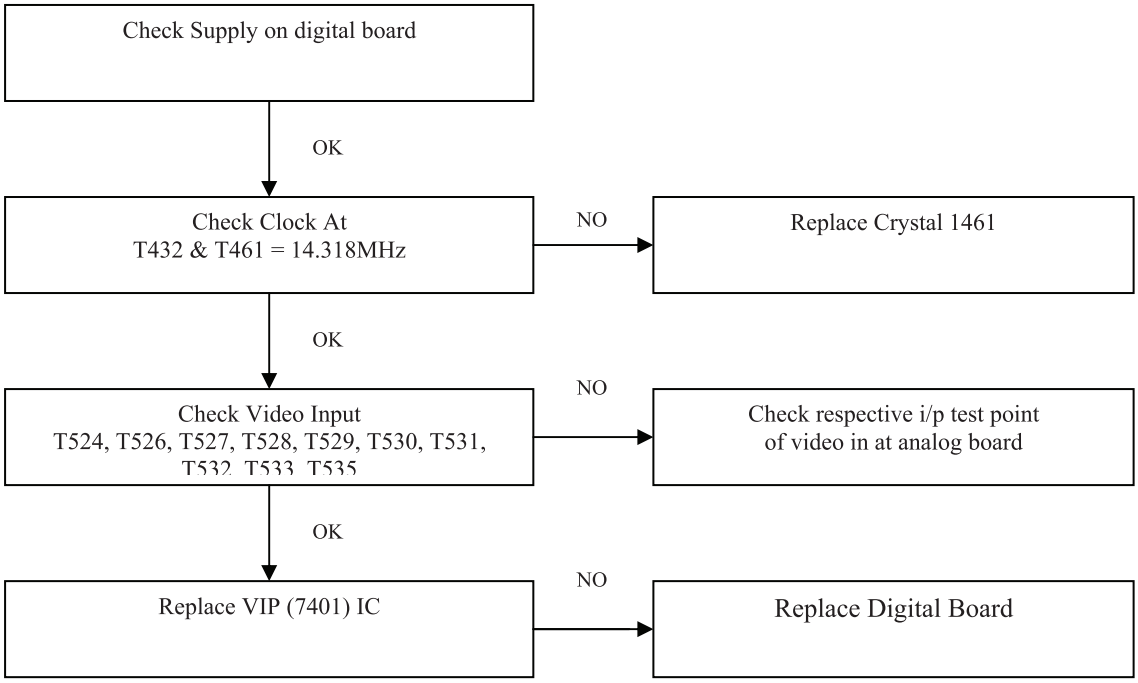
Pin 9	Pin 10	Source
0	0	Tuner
0	1	SCART 2
1	0	SCART 1
1	1	FRONT AV IN



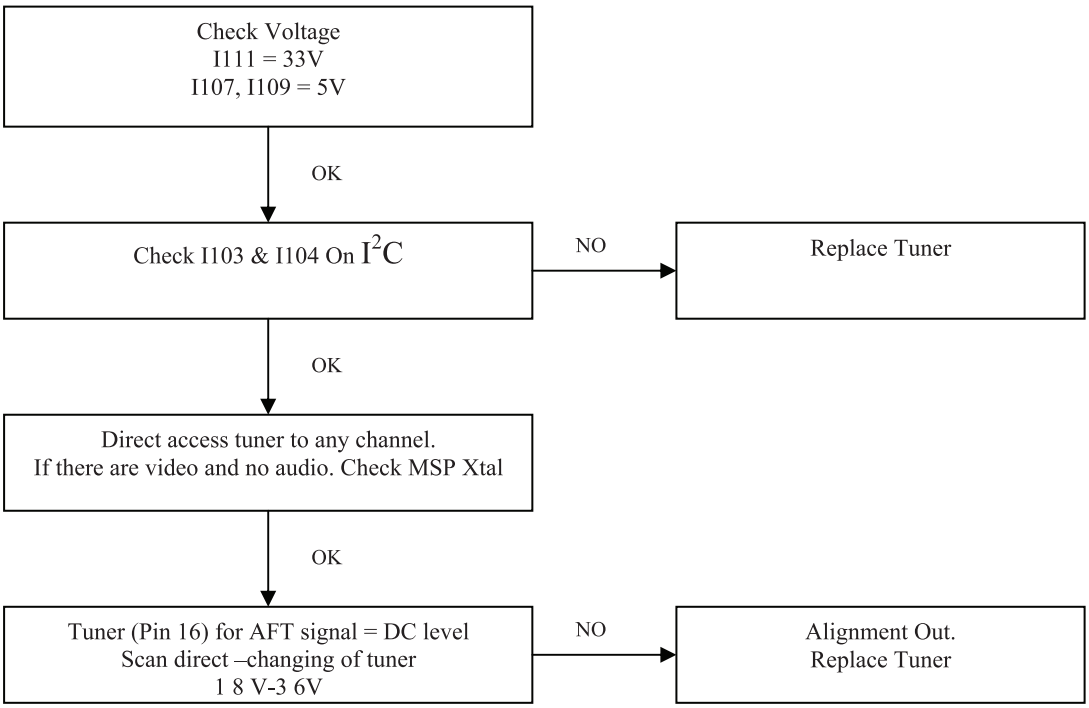
5.2.6 No Video Out Upon Power ON (Assume set is not dead)



5.2.7 No Video In Only

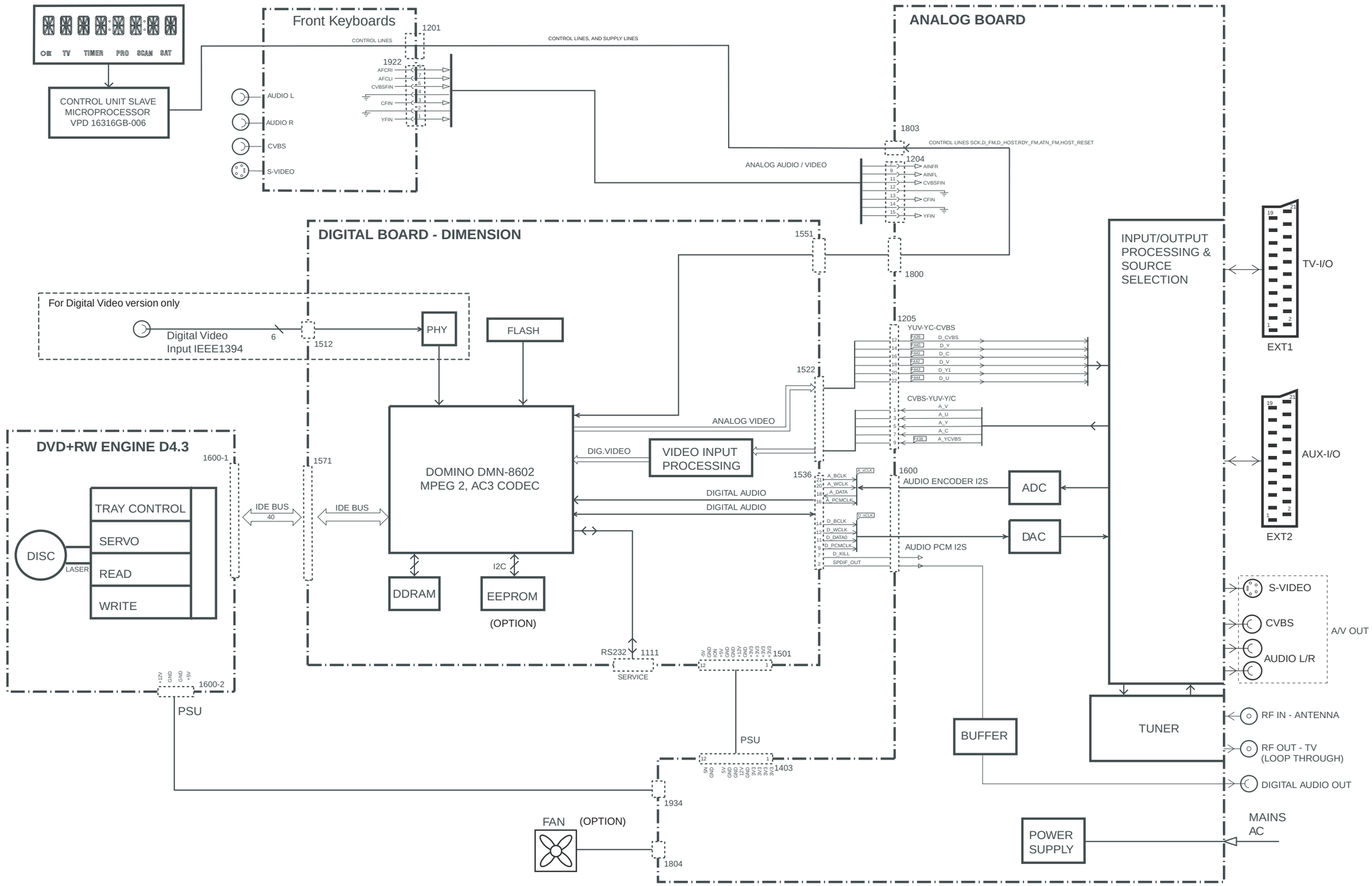


5.2.8 Tuner Not Functioning



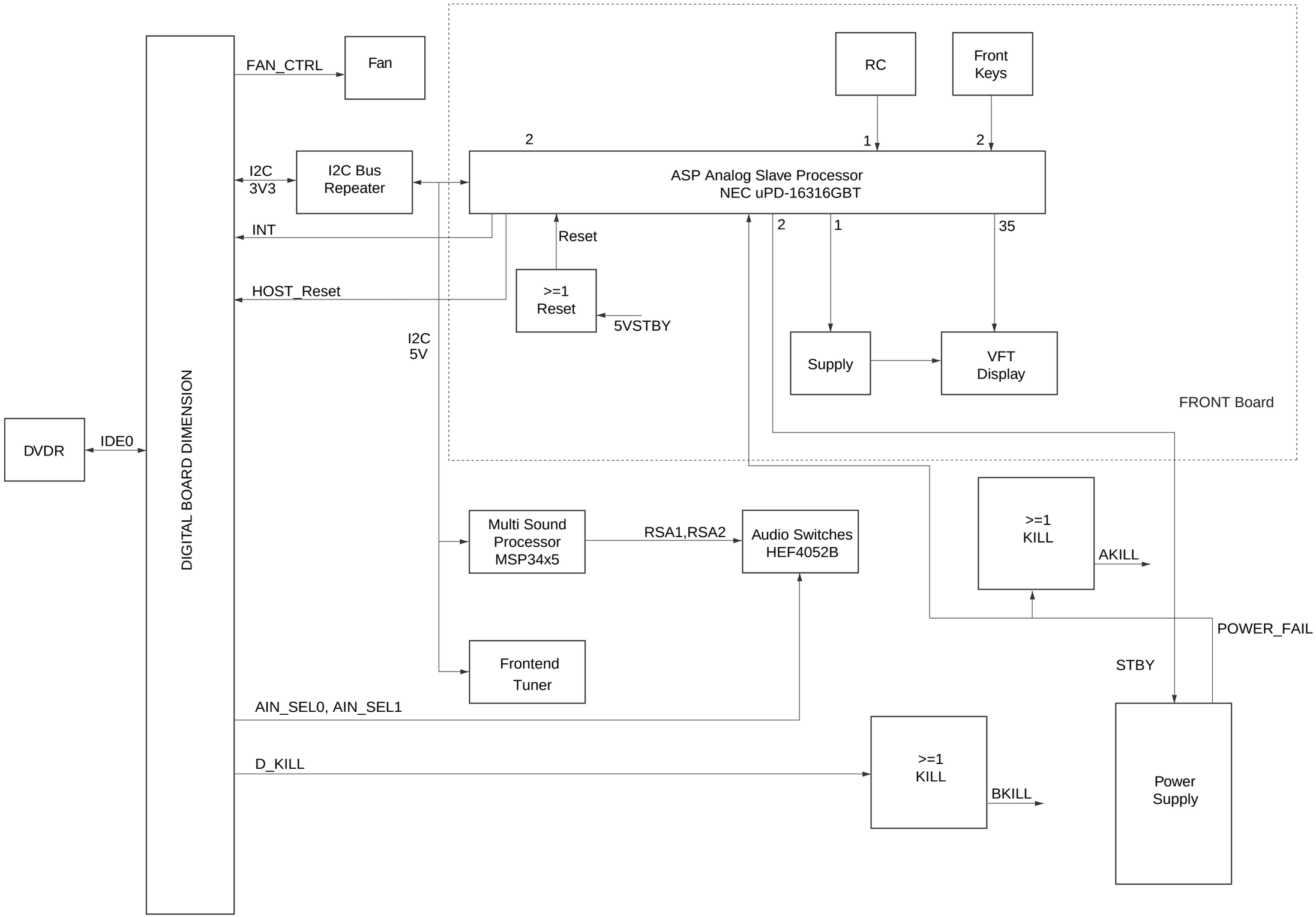
6. Block Diagrams, Waveforms, Wiring Diagram

Overall Block Diagram of the Set



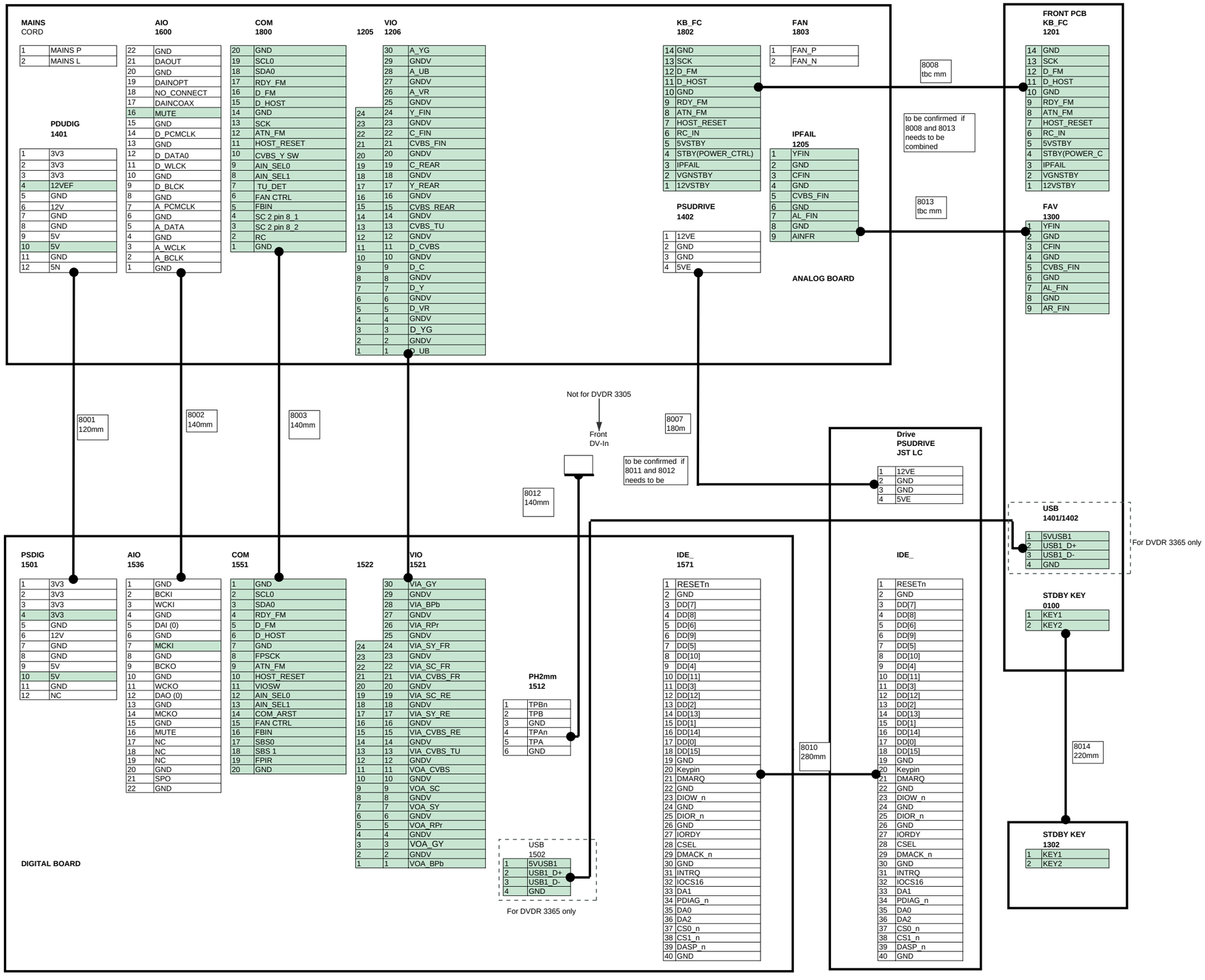
Control Block Diagram

Control Block Diagram Analog Board



Wiring Diagram

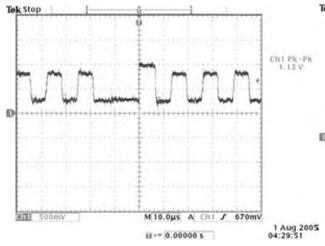
Interconnection Diagram Architecture



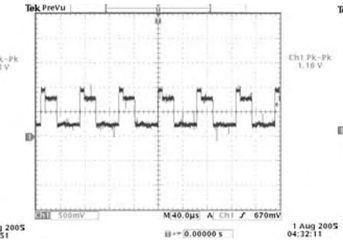
Waveforms

Waveforms of Analog Board

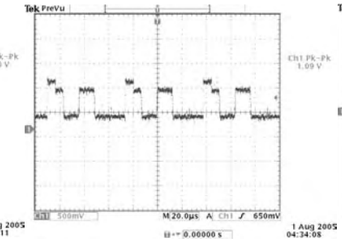
F204 BOUT



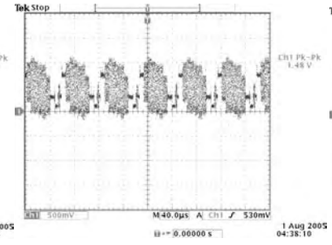
F206 GOUT



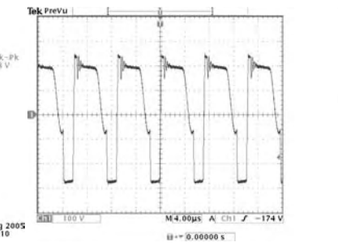
F207 ROUT



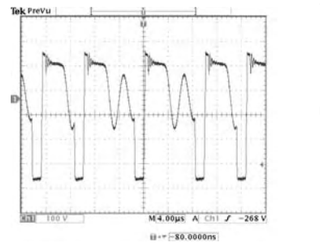
F209 YCVBS_OUT1



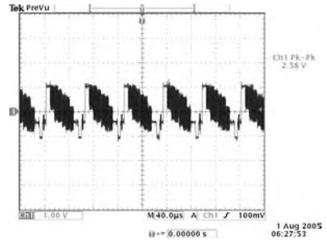
F417 VDrain (No Disc)



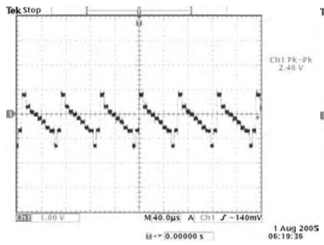
F417 Vdrain(Standby)



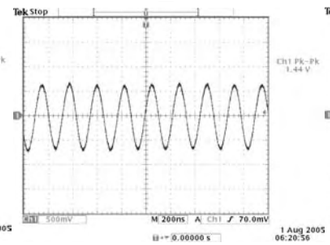
F602 CVBS



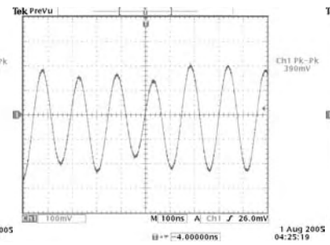
F604 Y_OUT



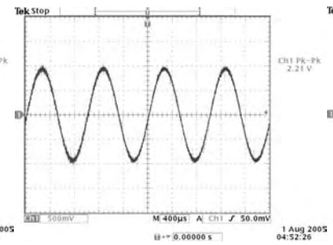
F605 C_OUT



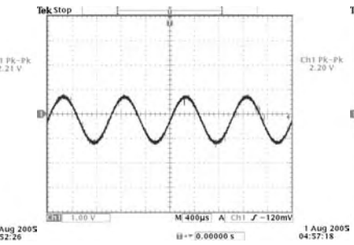
I110 SIFOUT



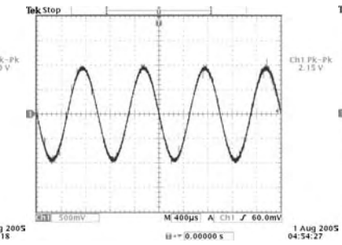
I303 AFER



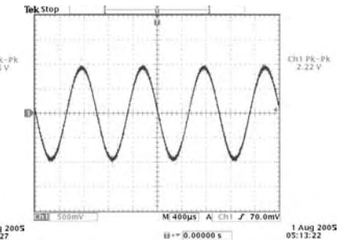
I304 AFEL



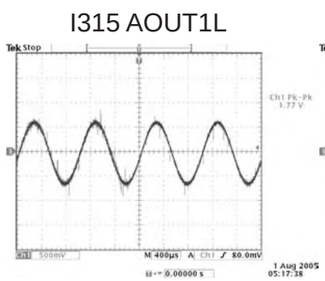
I310 ARADC



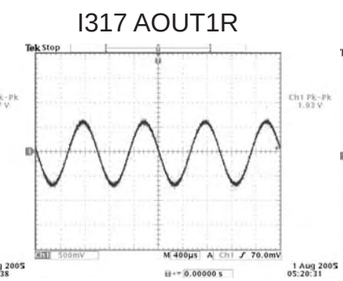
I311 ALADC



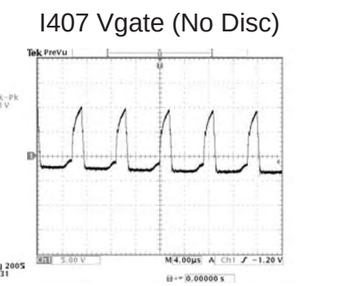
I315 AOUT1L



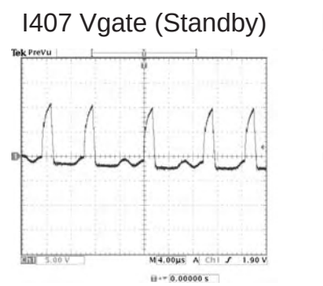
I317 AOUT1R



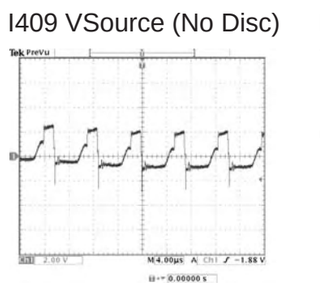
I407 Vgate (No Disc)



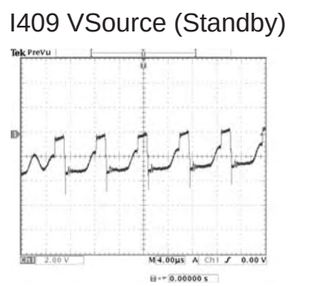
I407 Vgate (Standby)



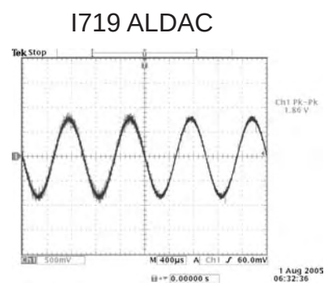
I409 VSource (No Disc)



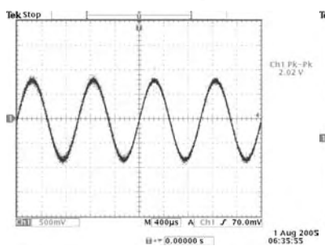
I409 VSource (Standby)



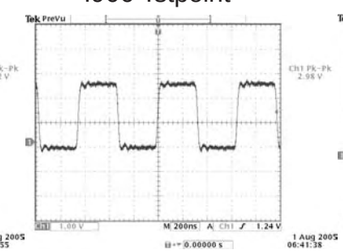
I719 ALDAC



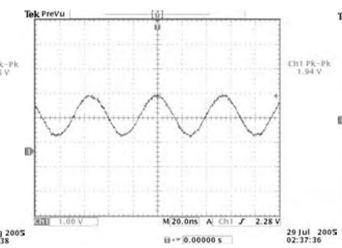
I721 ARDAC



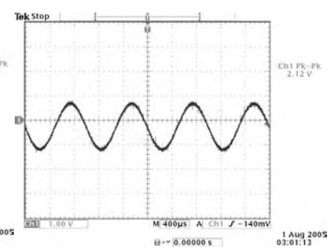
I906 Tstpoint



7500MSP XTAL IN

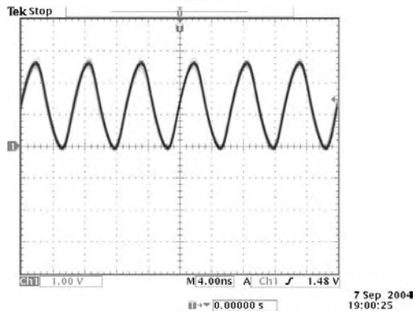


7500MSP XTAL OUT

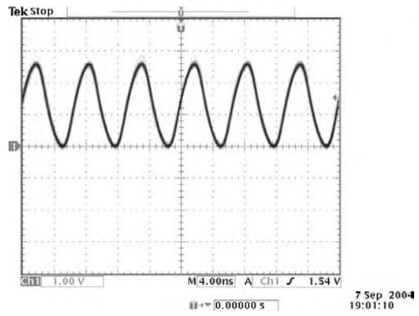


Waveforms of Digital Board

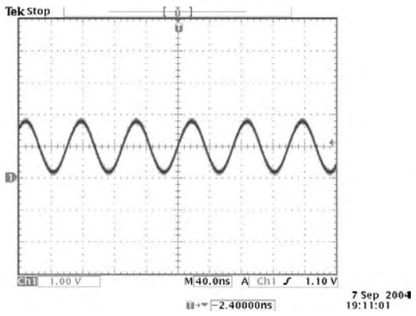
IC 7211 PIN 45



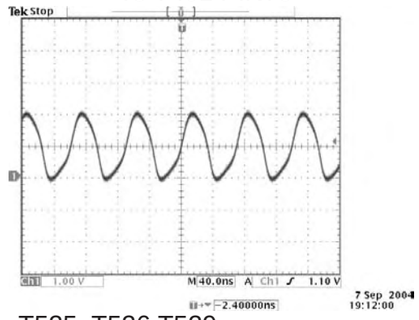
IC 7211 PIN 46



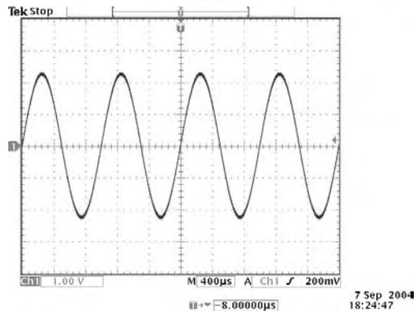
IC 7401 PIN74



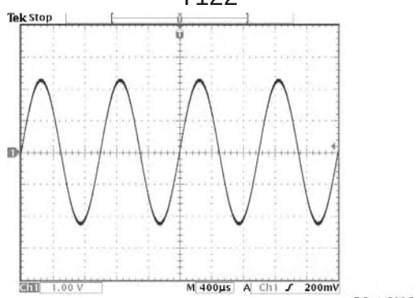
IC 7401 PIN75



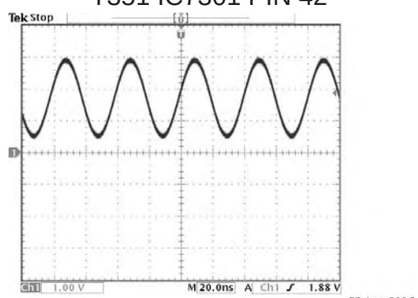
T121



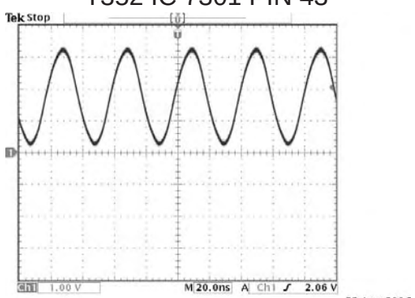
T122



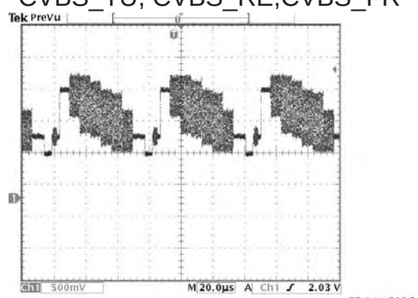
T351 IC7301 PIN 42



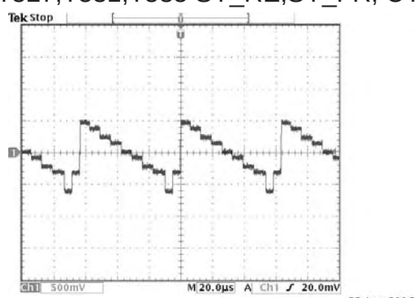
T352 IC 7301 PIN 43



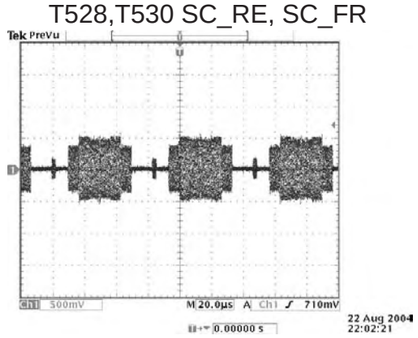
T525, T526,T529
CVBS_TU, CVBS_RE,CVBS_FR



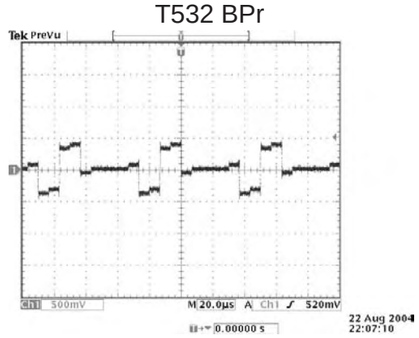
T527,T531,T535 SY_RE,SY_FR, CY



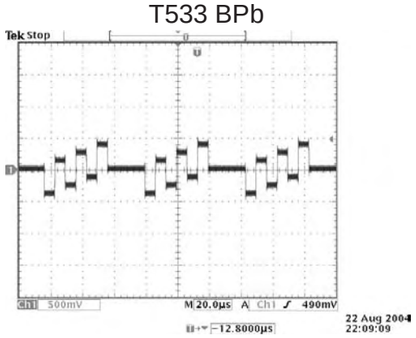
T528,T530 SC_RE, SC_FR



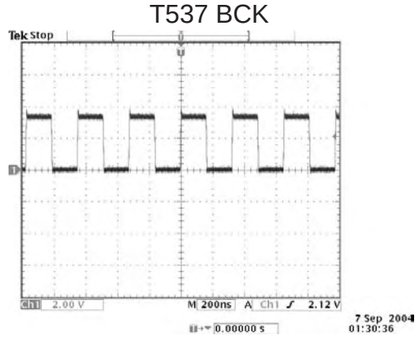
T532 BPr



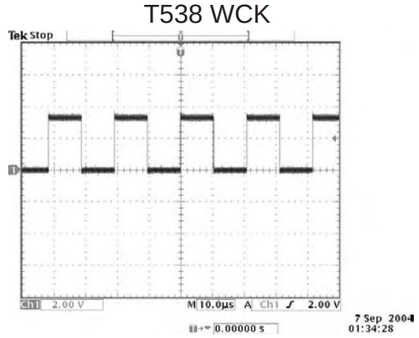
T533 BPb



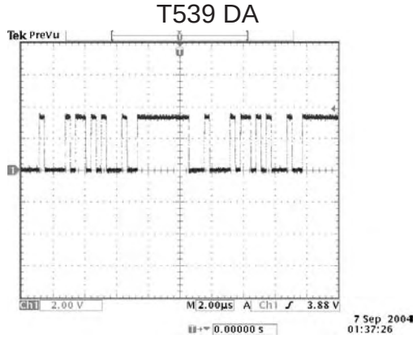
T537 BCK



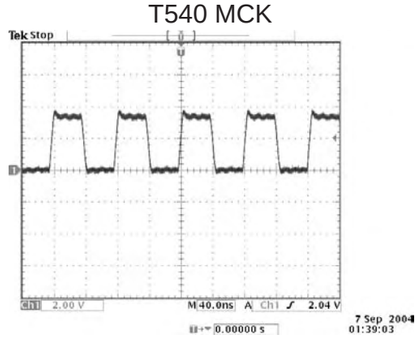
T538 WCK



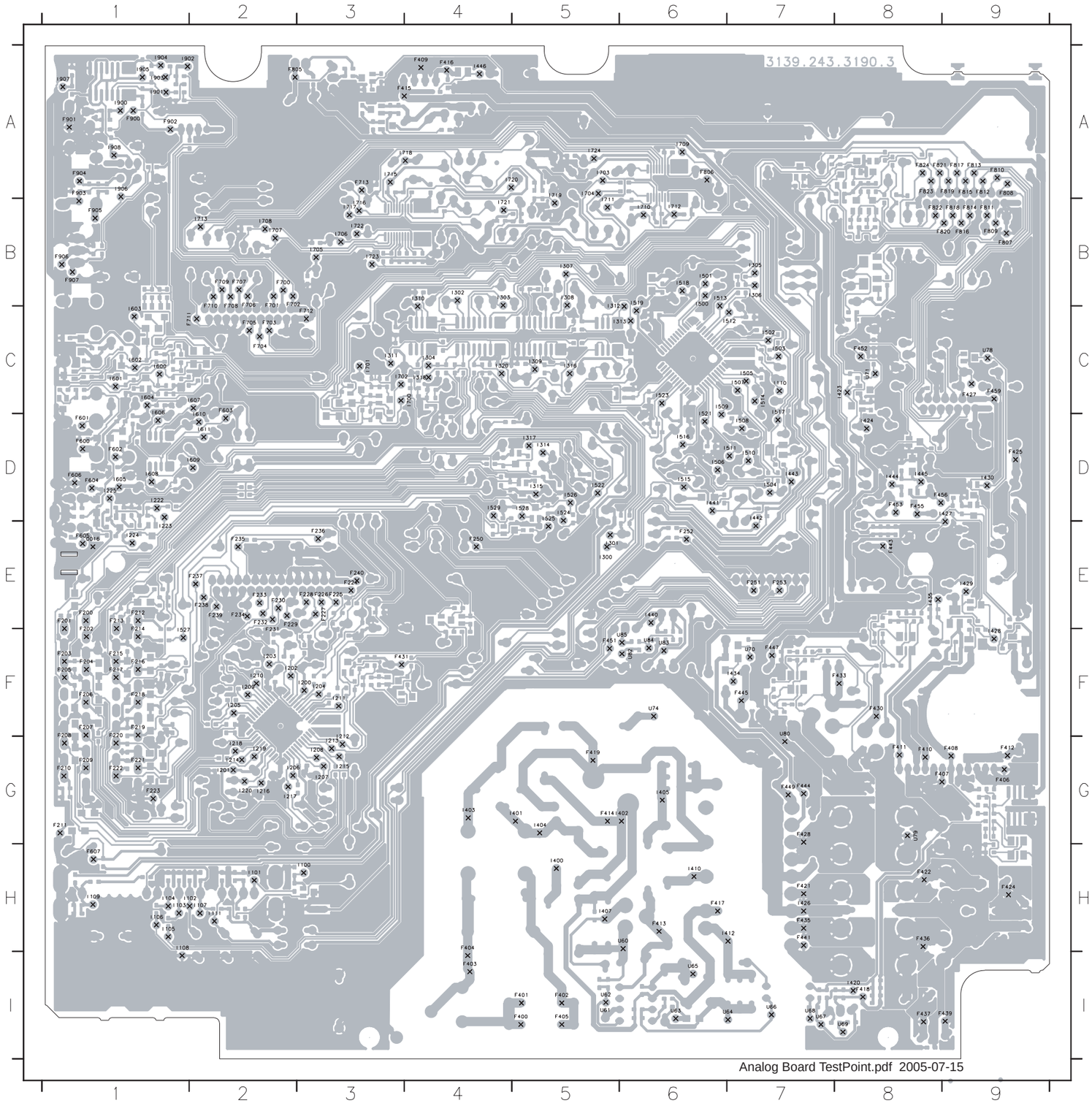
T539 DA



T540 MCK

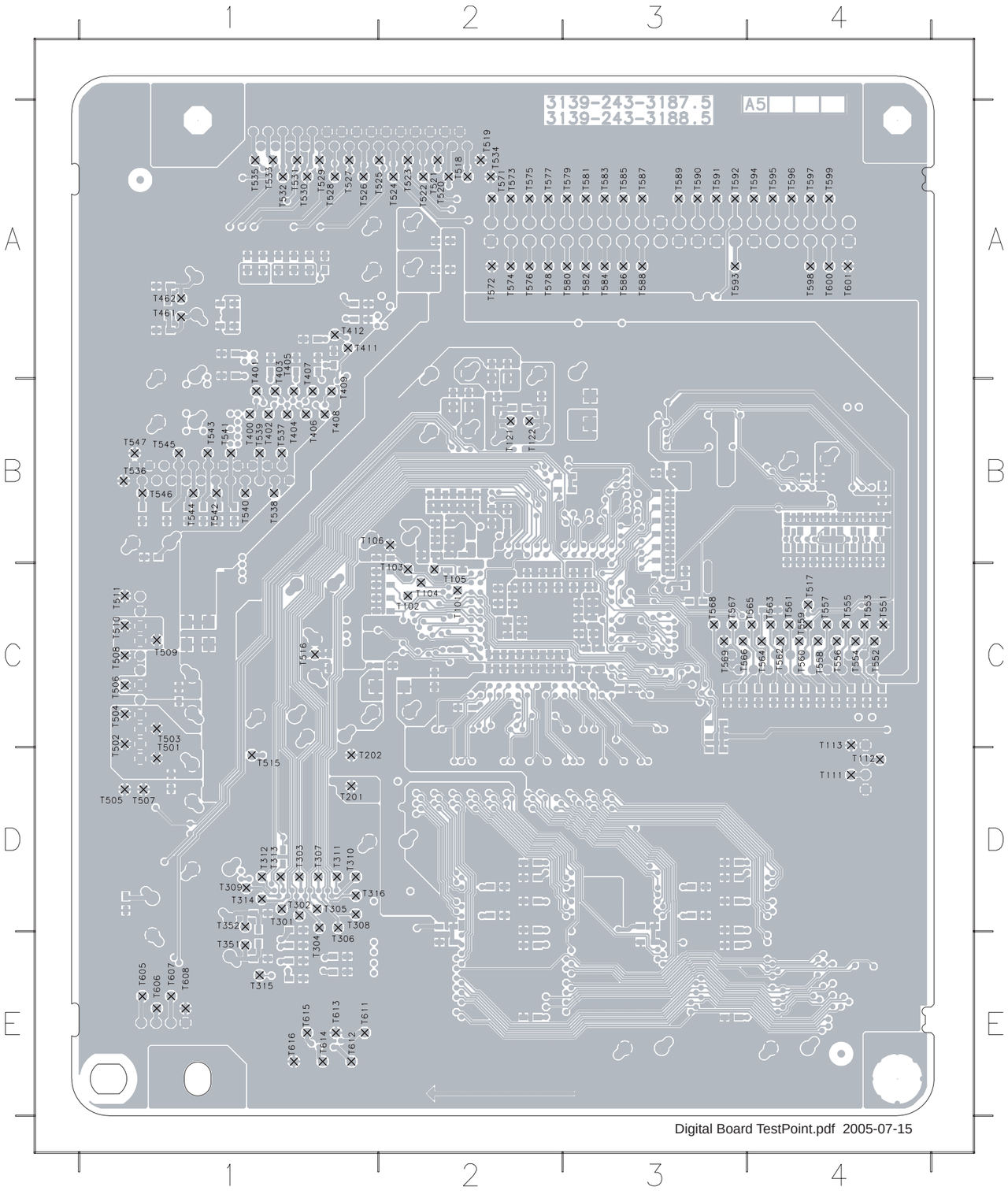


Test Points Overview for Analog Board



U60	H6	F810	A9	I603	C1		
U61	I5	F811	B9	I604	C1		
U62	I5	F812	A9	I605	D1		
U63	I6	F813	A9	I606	D1		
U64	I7	F814	B9	I607	C2		
U65	I6	F815	A9	I608	D1		
U66	I7	F816	B9	I609	D2		
U67	I7	F817	A9	I610	D2		
U68	I7	F818	B9	I611	D2		
U69	I8	F819	A9	I700	C3		
U70	F7	F820	B9	I701	C3		
U71	C8	F821	A8	I702	C3		
U74	F6	F822	B8	I703	A5		
U78	C9	F823	A8	I704	A5		
U79	G8	F824	A8	I705	B3		
U80	G7	F900	A1	I706	B3		
U82	F6	F901	A1	I707	B2		
U83	F6	F902	A1	I708	B2		
U84	F6	F903	B1	I709	A6		
U85	F6	F904	A1	I710	B6		
0016	E1	F905	B1	I711	B5		
F200	E1	F906	B1	I712	B6		
F201	E1	F907	B1	I713	B2		
F202	E1	I100	H3	I715	A3		
F203	E1	I101	H2	I716	B3		
F204	E1	I102	H2	I717	B3		
F205	E1	I103	H1	I718	A4		
F206	E1	I104	H1	I719	B5		
F207	E1	I105	H1	I720	A4		
F208	G1	I106	H1	I721	B4		
F209	G1	I107	H2	I722	B3		
F210	G1	I108	I1	I723	B3		
F211	G1	I109	H1	I724	A5		
F212	E1	I110	C7	I900	A1		
F213	E1	I111	H2	I901	A1		
F214	E1	I200	F3	I902	A1		
F215	E1	I201	G2	I903	A1		
F216	E1	I202	F2	I904	A1		
F217	E1	I203	F2	I905	A1		
F218	E1	I204	F3	I906	A1		
F219	E1	I205	F2	I907	A1		
F220	G1	I206	G2	I908	A1		
F221	G1	I207	G3				
F222	G1	I208	G2				
F223	G1	I209	G2				
F224	E3	I210	F2				
F225	E3	I211	F3				
F226	E3	I212	G3				
F227	E3	I213	G3				
F228	E3	I214	G2				
F229	E2	I215	G3				
F230	E2	I216	G2				
F231	E2	I217	G2				
F232	E2	I218	G2				
F233	E2	I219	G2				
F234	E2	I220	G2				
F235	E2	I222	D1				
F236	E3	I223	D1				
F237	E2	I224	F1				
F238	E2	I225	D1				
F239	E2	I300	F5				
F240	E3	I301	F5				
F241	E3	I302	B4				
F250	E4	I303	B4				
F251	E7	I304	C4				
F252	E6	I305	B7				
F253	E7	I306	B7				
F400	I5	I307	B5				
F401	I5	I308	B5				
F402	I5	I309	C5				
F403	I4	I310	C4				
F404	I4	I311	C3				
F405	I5	I312	C6				
F406	G9	I313	C6				
F407	G8	I314	C6				
F408	G9	I315	D5				
F409	A4	I316	C5				
F410	G8	I317	D5				
F411	G8	I318	C4				
F412	G9	I320	C4				
F413	H6	I400	H5				
F414	G5	I401	G5				
F415	A3	I402	G6				
F416	A4	I403	G4				
F417	H6	I404	G5				
F418	I8	I405	G6				
F419	G5	I407	H5				
F422	H8	I410	H6				
F424	H9	I412	H7				
F425	D9	I420	I8				
F427	C9	I423	C8				
F428	G7	I424	D8				
F430	F8	I426	H7				
F431	F3	I427	F9				
F433	F8	I428	F9				
F435	H7	I429	F9				
F436	H8	I430	D9				
F437	I8	I434	F7				
F439	I9	I435	E8				
F441	H7	I440	E6				
F443	F8	I441	D6				
F444	G7	I442	E7				
F445	F7	I443	D7				
F447	G7	I444	D8				
F449	G7	I445	D8				
F451	F5	I446	A4				
F452	G8	I500	B6				
F453	G8	I501	B6				
F455	D8	I502	C7				
F456	D8	I503	C7				
F459	C9	I504	D7				
F600	D1	I505	C7				
F601	D1	I506	D6				
F602	D1	I507	C7				
F603	D2	I508	D7				
F604	D1	I509	D6				
F605	E1	I510	D7				
F606	D1	I511	D7				
F607	H1	I512	C7				
F700	B2	I513	B6				
F701	B2	I514	C7				
F702	B2	I515	D6				
F703	C2	I516	D6				
F704	C2	I517	D7				
F705	C2	I518	B6				
F706	B2	I519	C6				
F707	B2	I521	D6				
F708	B2	I522	D5				
F709	B2	I523	C6				
F710	B2	I524	D5				
F711	C2	I525	E5				
F712	C3	I526	D5				
F713	A3	I527	F1				
F805	A2	I528	D5				
F806	A6	I529	D4				
F807	B9	I600	C1				
F808	A9	I601	C1				
F809	B9	I602	C1				

Test Points Overview for Digital Board

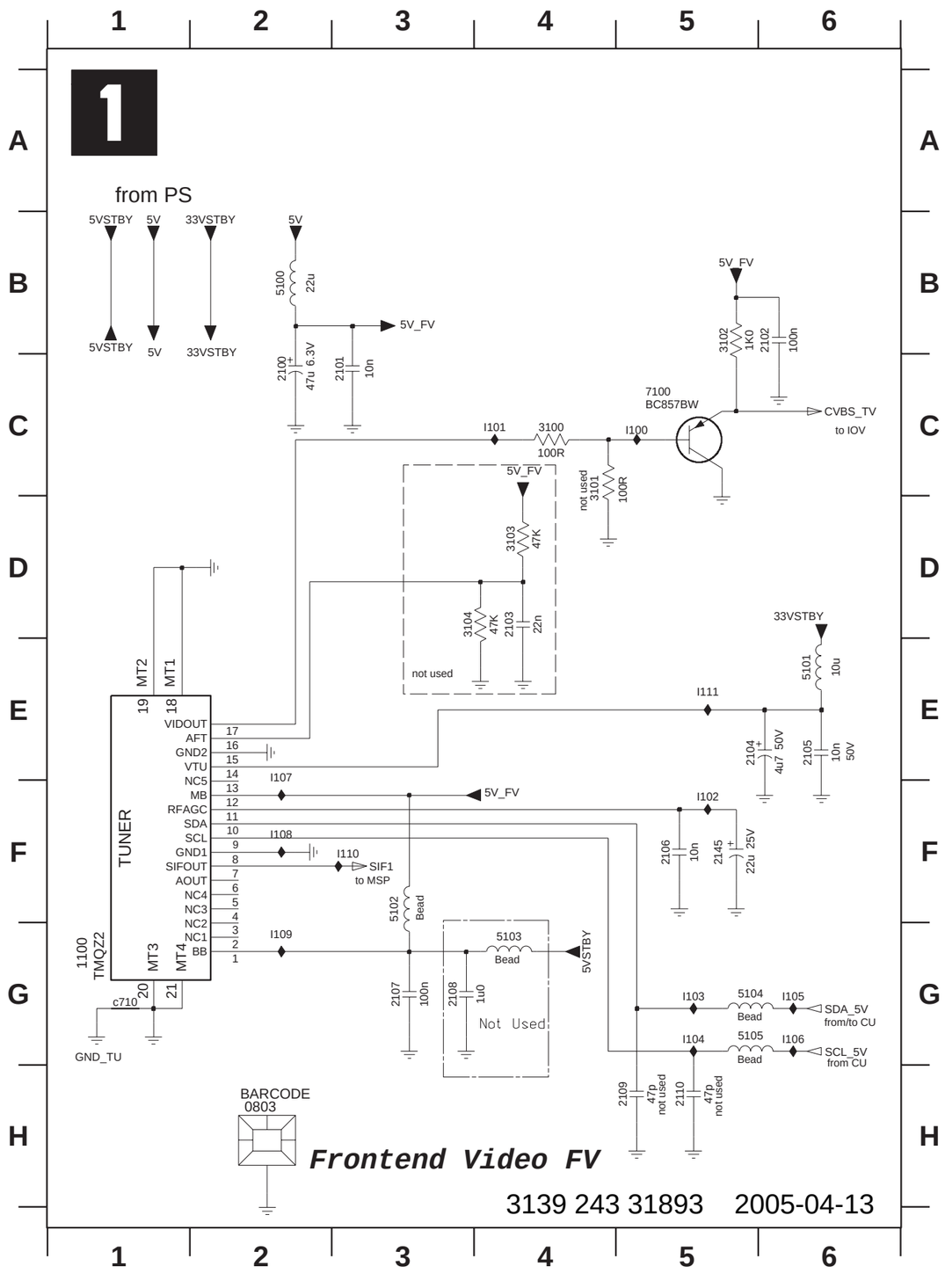


Digital Board TestPoint.pdf 2005-07-15

T101	C2	T545	B1
T102	C2	T546	B1
T103	C2	T547	B1
T104	C2	T551	C4
T105	C2	T552	C4
T106	B2	T553	C4
T111	D4	T554	C4
T112	D4	T555	C4
T113	C4	T556	C4
T121	B2	T557	C4
T122	B2	T558	C4
T201	D1	T559	C4
T202	D1	T560	C4
T301	D1	T561	C4
T302	D1	T562	C4
T303	D1	T563	C4
T304	D1	T564	C4
T305	D1	T565	C4
T306	D1	T566	C3
T307	D1	T567	C3
T308	D1	T568	C3
T309	D1	T569	C3
T310	D1	T571	A2
T311	D1	T572	A2
T312	D1	T573	A2
T313	D1	T574	A2
T314	D1	T575	A2
T315	E1	T576	A2
T316	D1	T577	A2
T351	E1	T578	A2
T352	D1	T579	A3
T400	B1	T580	A3
T401	B1	T581	A3
T402	B1	T582	A3
T403	B1	T583	A3
T404	B1	T584	A3
T405	B1	T585	A3
T406	B1	T586	A3
T407	B1	T587	A3
T408	B1	T588	A3
T409	B1	T589	A3
T411	A1	T590	A3
T412	A1	T591	A3
T461	A1	T592	A3
T462	A1	T593	A3
T501	D1	T594	A4
T502	C1	T595	A4
T503	C1	T596	A4
T504	C1	T597	A4
T505	D1	T598	A4
T506	C1	T599	A4
T507	D1	T600	A4
T508	C1	T601	A4
T509	C1	T605	E1
T510	C1	T606	E1
T511	C1	T607	E1
T515	D1	T608	E1
T516	C1	T611	E1
T517	C4	T612	E1
T518	A2	T613	E1
T519	A2	T614	E1
T520	A2	T615	E1
T521	A2	T616	E1
T522	A2		
T523	A2		
T524	A2		
T525	A2		
T526	A1		
T527	A1		
T528	A1		
T529	A1		
T530	A1		
T531	A1		
T532	A1		
T533	A1		
T534	A2		
T535	A1		
T536	B1		
T537	B1		
T538	B1		
T539	B1		
T540	B1		
T541	B1		
T542	B1		
T543	B1		
T544	B1		

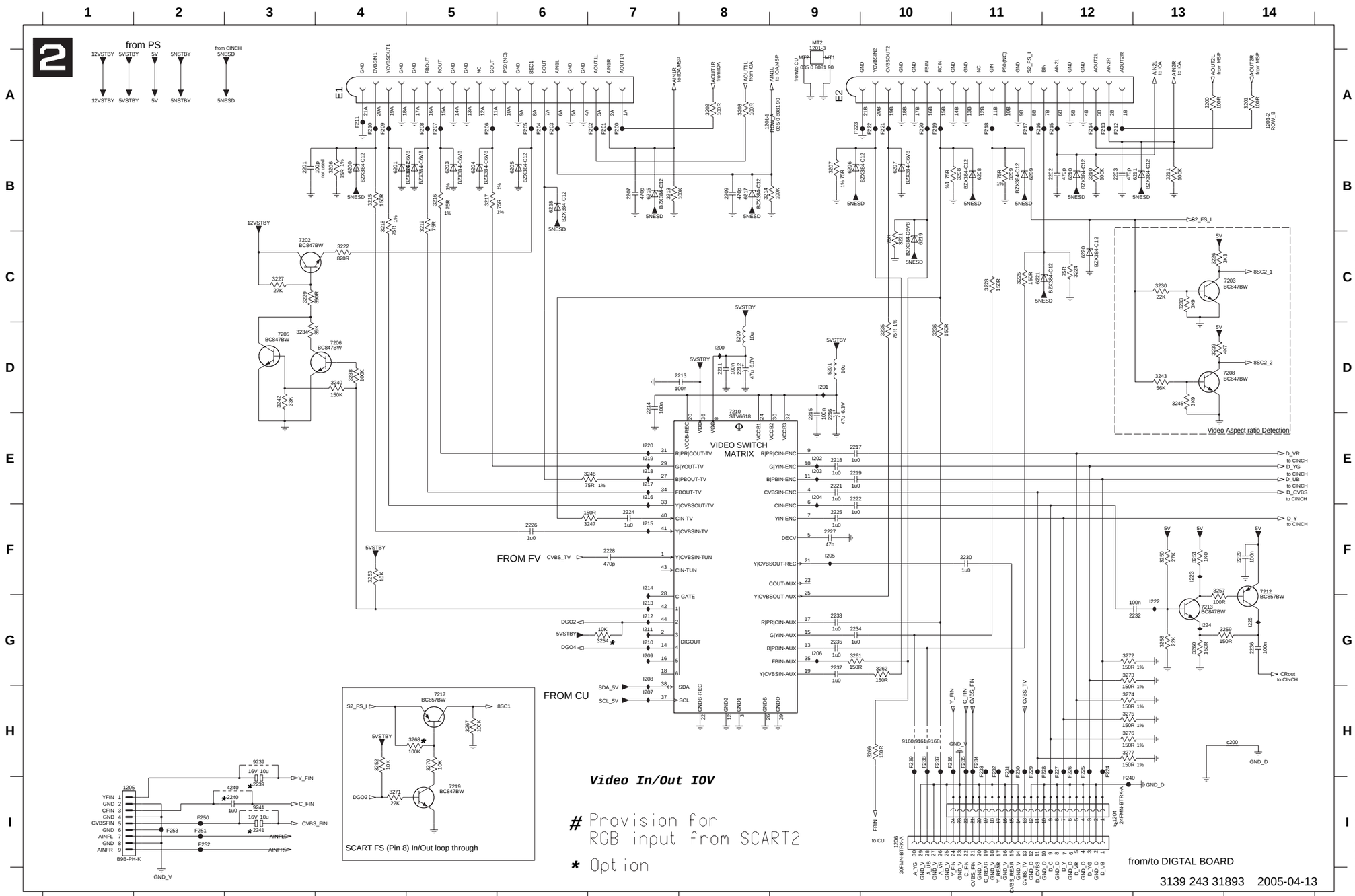
7. Circuit Diagrams and PWB Layouts

Analog: Frontend Video (FV)

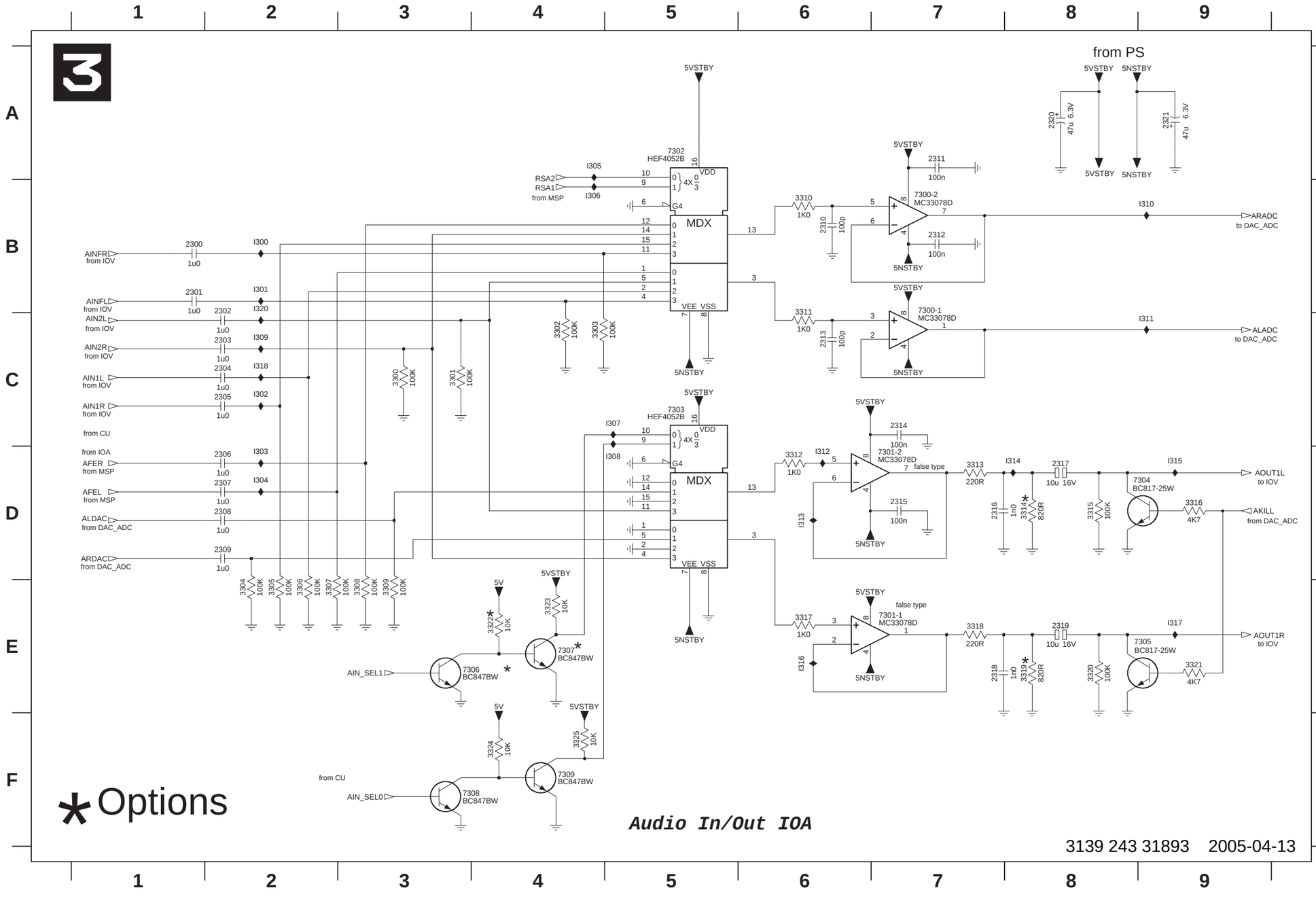


0803 H2
1100 G1
2100 C2
2101 C3
2102 B6
2103 D4
2104 E5
2105 E6
2106 F5
2107 G3
2108 G3
2109 H5
2110 H5
2145 F5
3100 C4
3101 C4
3102 B5
3103 D4
3104 D3
5100 B2
5101 E6
5102 F3
5103 G4
5104 G5
5105 G5
7100 C5
I100 C5
I101 C4
I102 F5
I103 G5
I104 G5
I105 G6
I106 G6
I107 E2
I108 F2
I109 G2
I110 F3
I111 E5
c710 G1

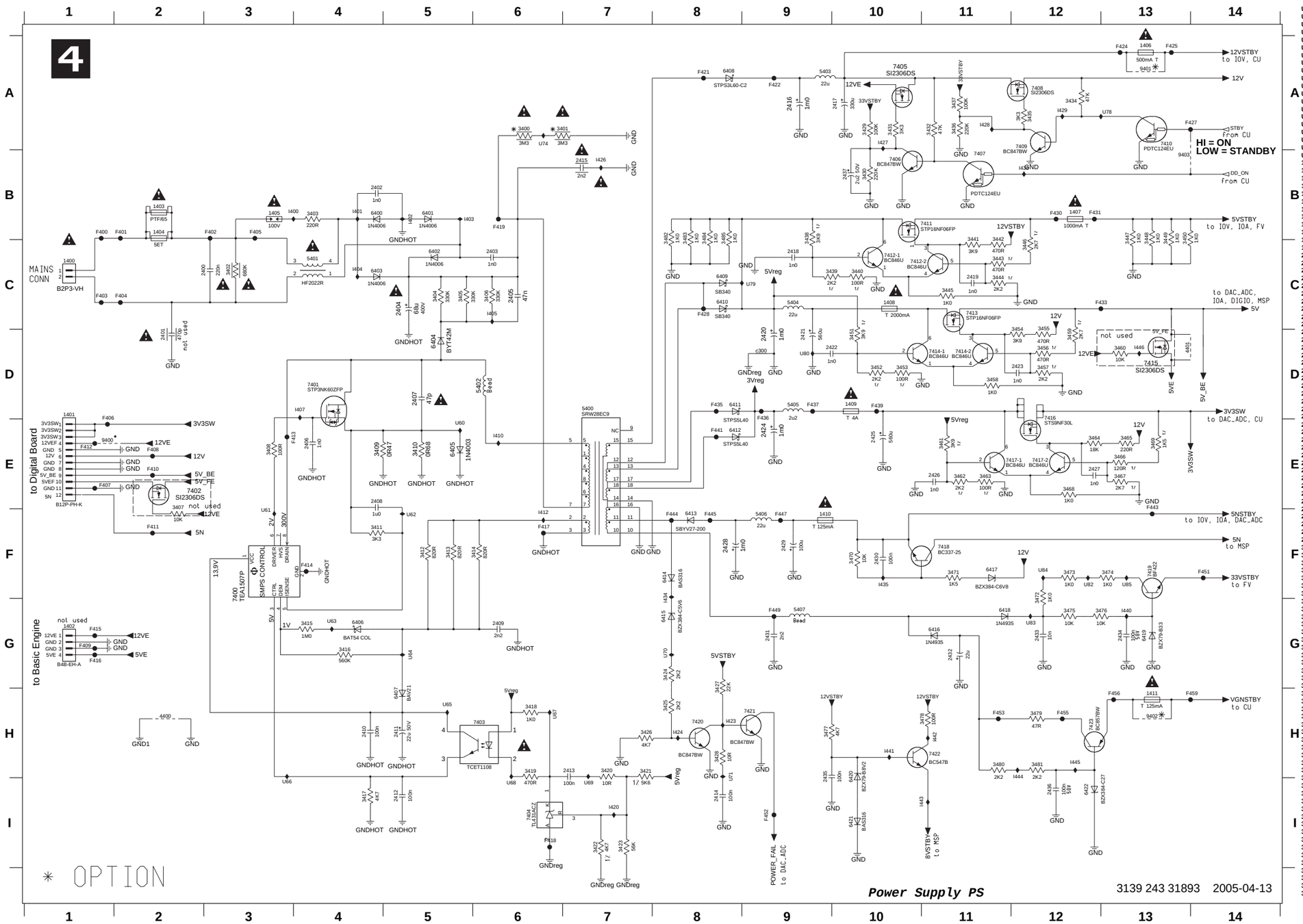
Analog: Video In / Out (IOV)



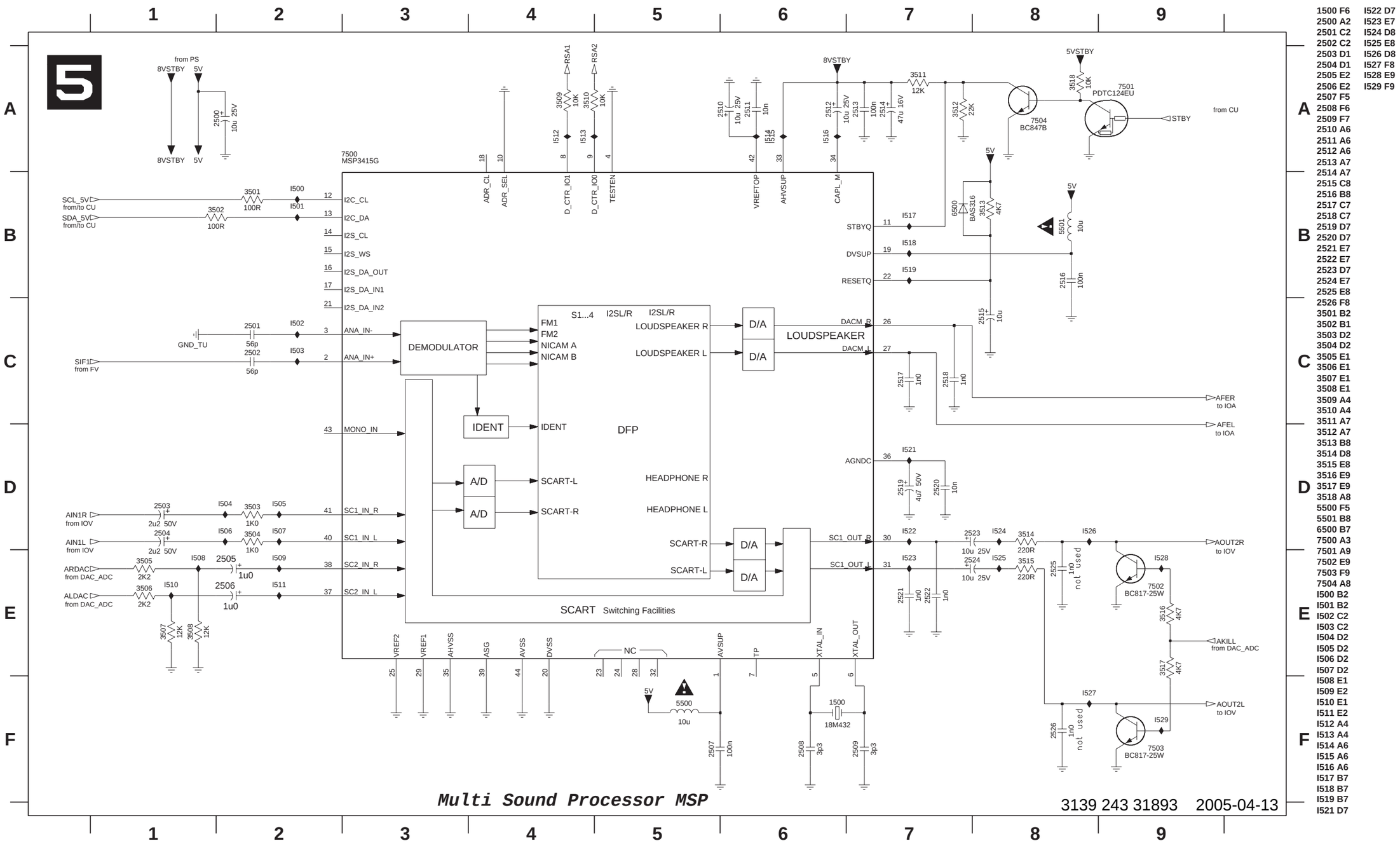
Analog: Audio In / Out (IOA)



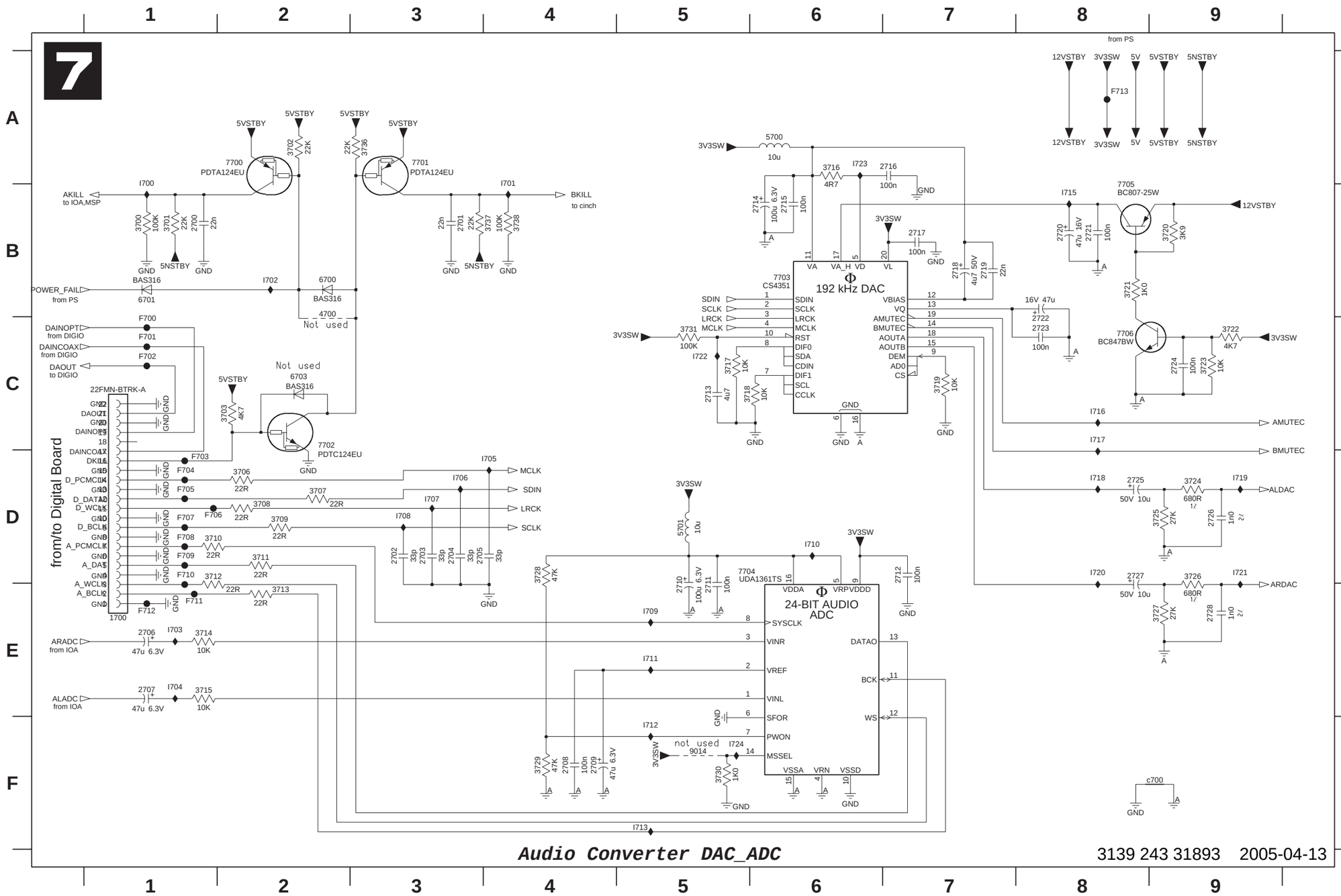
Analog: Power Supply (PS)



Analog: Multi Sound Processing (MSP)

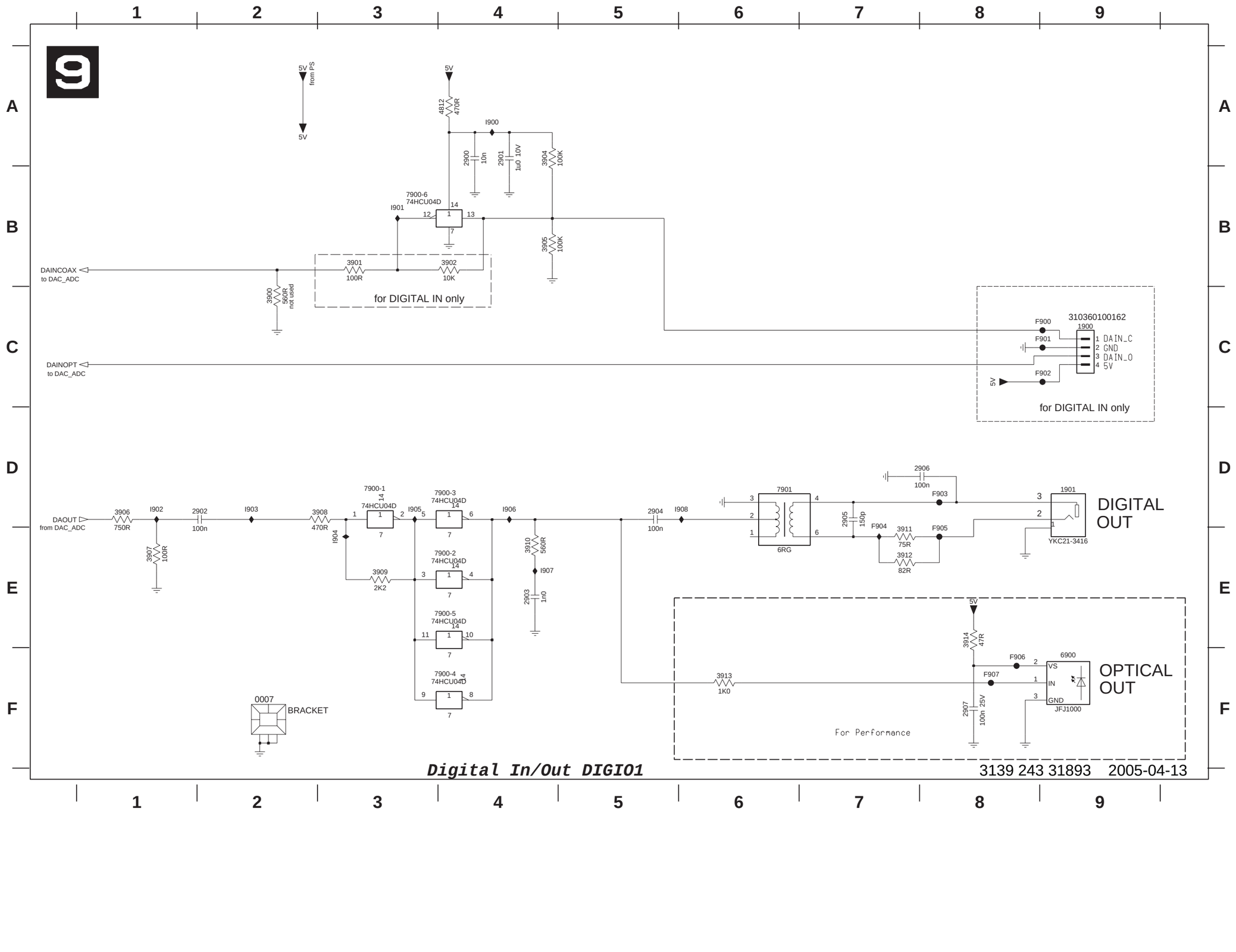


Analog: Audio Converter (DAC_ADC)



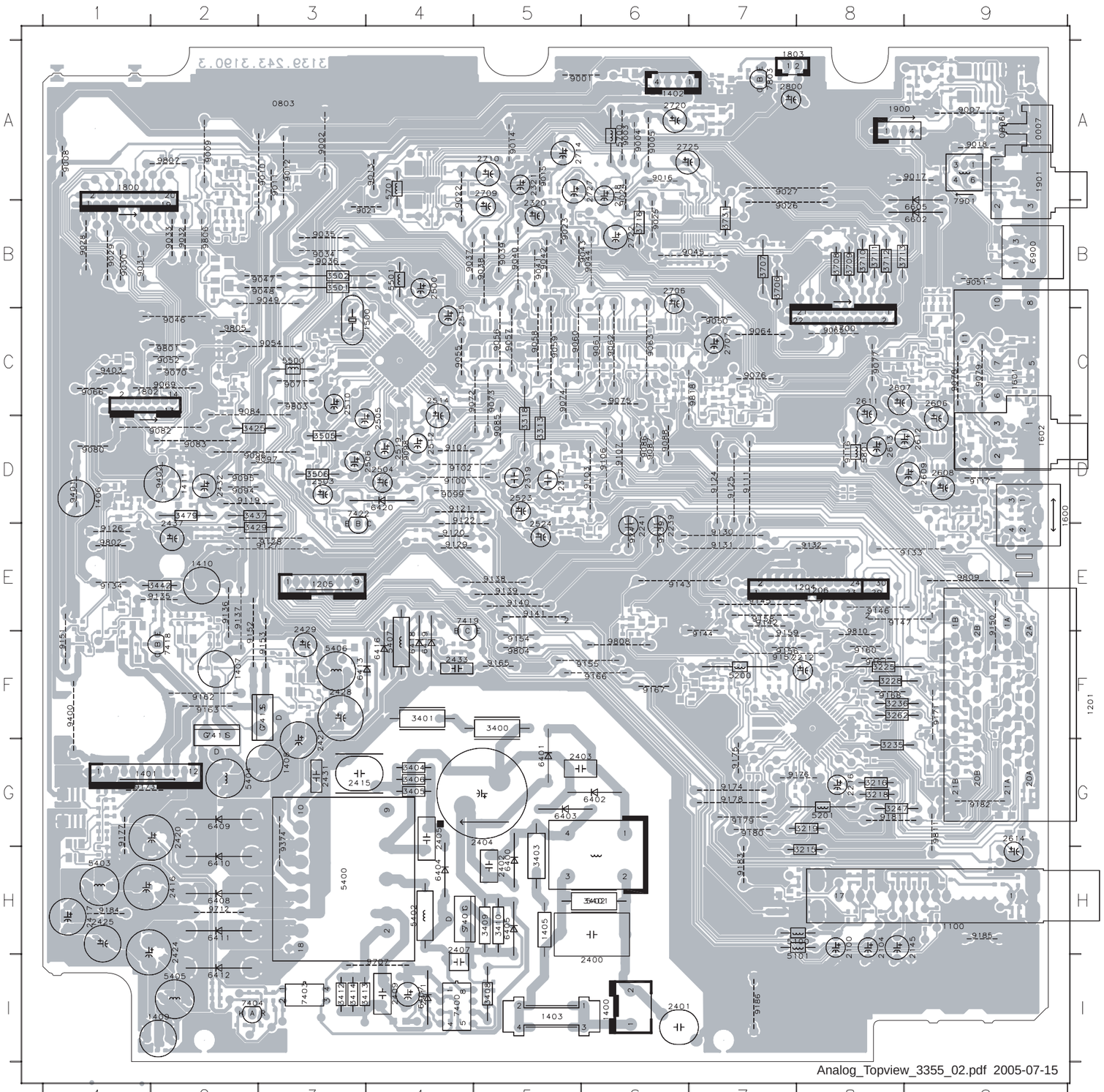
1700 E1	7706 C8
2700 B1	9014 F5
2701 B3	F700 C1
2702 D3	F701 C1
2703 D3	F702 C1
2704 D3	F703 D1
2705 D3	F704 D1
2706 E1	F705 D1
2707 E1	F706 D1
2708 F4	F707 D1
2709 F4	F708 D1
2710 E5	F709 D1
2711 E5	F710 D1
2712 D7	F711 E1
2713 C5	F712 E1
2714 B6	F713 A8
2715 B6	I700 A1
2716 A7	I701 A4
2717 B7	I702 B2
2718 B7	I703 E1
2719 B7	I704 E1
2720 B8	I705 D4
2721 B8	I706 D3
2722 B8	I707 D3
2723 C8	I708 D3
2724 C9	I709 E5
2725 D8	I710 D6
2726 D9	I711 E5
2727 D8	I712 F5
2728 E9	I713 F5
3700 B1	I715 B8
3701 B1	I716 C8
3702 A2	I717 C8
3703 C2	I718 D8
3706 D2	I719 D9
3707 D2	I720 D8
3708 D2	I721 D9
3709 D2	I722 C5
3710 D1	I723 A6
3711 D2	I724 F5
3712 D1	c700 F9
3713 E2	
3714 E1	
3715 E1	
3716 A6	
3717 C5	
3718 C5	
3719 C7	
3720 B9	
3721 B8	
3722 C9	
3723 C9	
3724 D9	
3725 D9	
3726 D9	
3727 E9	
3728 D4	
3729 F4	
3730 F5	
3731 C5	
3736 A3	
3737 B4	
3738 B4	
4700 B2	
5700 A6	
5701 D5	
6700 B2	
6701 B1	
6703 C2	
7700 A2	
7701 A3	
7702 C2	
7703 B6	
7704 D6	
7705 B8	

Analog: Digital In / Out 1 (DIGIO 1)



0007 F2
1900 C9
1901 D9
2900 A4
2901 A4
2902 D2
2903 E4
2904 D5
2905 D7
2906 D8
2907 F8
3900 C2
3901 B3
3902 B4
3904 A4
3905 B4
3906 D1
3907 E1
3908 D3
3909 E3
3910 E4
3911 E7
3912 E7
3913 F6
3914 E8
4812 A4
6900 F9
7900-1 D3
7900-2 E4
7900-3 D4
7900-4 F4
7900-5 E4
7900-6 B3
7901 D6
F900 C9
F901 C9
F902 C9
F903 D8
F904 D7
F905 E8
F906 F8
F907 F8
I900 A4
I901 B3
I902 D1
I903 D2
I904 E3
I905 D3
I906 D4
I907 E4
I908 D6

Layout: Analog-Main Part (Top View)



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0007	A9	5201	G8	9111	D7	2608	D9
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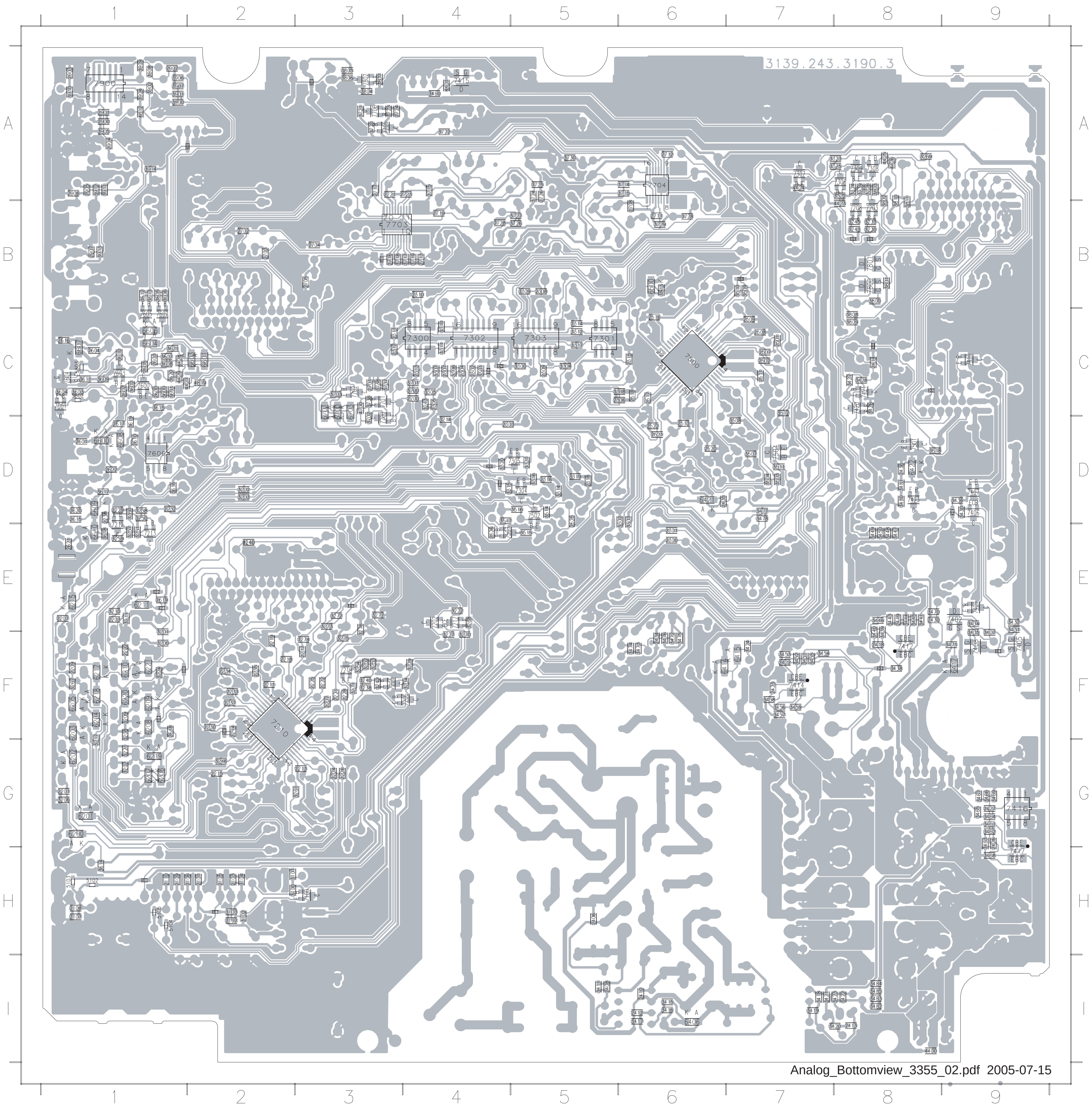
1100	H9	5401	H6	9117	D9	2611	C8
1204	F8	5402	H4	9118	D2	2612	D9
1205	F3	5403	H1	9120	E4	2613	D8
1206	E8	5404	G2	9121	D4	2614	G9
1400	I6	5405	I2	9122	D4	2706	C6
1401	G1	5406	F3	9124	D7	2707	C7
1402	A6	5407	F4	9125	D7	2709	A5
1403	I5	5500	C3	9126	E1	2710	A5
1405	H5	5501	B4	9127	E3	2714	A5
1406	D1	5700	A6	9128	E3	2718	A6
1407	F2	5701	A4	9129	E4	2720	A6
1408	G3	5801	D8	9130	E7	2722	D6
1409	I2	6400	H5	9131	E7	2725	A6
1410	F2	6401	G5	9132	E6	2727	A6
1411	D2	6402	G6	9133	E6	2800	A7
1500	C4	6403	G5	9134	E1	3215	H8
1600	D9	6404	H4	9135	E2	3216	G8
1601	C9	6405	H5	9136	E2	3218	G8
1602	D9	6407	I4	9137	E3	3219	G8
1700	A8	6408	G2	9138	E5	3225	F8
1800	A1	6409	G2	9139	E5	3226	F8
1802	C1	6410	H2	9140	E5	3235	F8
1803	A7	6411	H2	9141	E5	3236	F8
1900	A8	6412	I2	9142	E7	3247	G8
1901	A9	6413	F3	9143	E6	3262	F8
2100	H8	6416	F4	9144	E7	3313	D5
2104	H8	6418	F4	9145	E7	3318	D5
2145	I8	6419	F4	9146	E8	3400	F5
2212	F8	6420	D4	9147	E8	3401	F4
2216	G8	6602	B9	9150	E9	3402	H6
2239	F6	6605	B9	9151	F2	3403	H5
2241	F6	6900	B9	9152	F2	3404	G4
2317	D5	7400	I4	9153	F3	3405	G4
2319	D5	7401	H4	9154	F5	3406	I4
2320	B5	7403	I3	9155	F6	3408	I5
2321	A5	7404	I2	9156	F6	3409	H5
2400	I6	7411	F2	9157	F7	3410	H5
2401	I6	7413	F3	9158	E7	3412	I3
2402	H5	7418	F2	9159	F7	3413	I3
2403	G5	7419	H4	9160	F8	3414	I3
2404	G5	7422	D3	9161	F8	3425	D2
2405	G4	7803	A7	9162	F2	3427	D2
2407	H4	7901	B9	9163	F2	3442	F2
2409	I4	9001	A5	9165	F6	3479	D2
2411	I4	9002	A5	9166	F6	3501	B3
2415	G3	9003	A6	9167	F6	3502	B3
2416	H2	9004	A6	9168	F8	3505	D3
2417	H1	9005	A6	9171	F9	3506	D3
2420	G2	9007	A9	9173	G7	3706	B7
2421	G3	9008	A1	9174	G7	3707	B7
2424	H2	9009	A2	9175	G7	3708	B8
2425	H1	9010	A3	9176	G8	3709	B8
2428	F3	9011	A3	9177	G8	3710	B8
2429	F3	9012	A3	9178	G7	3711	B8
2431	G3	9013	A4	9179	G7	3712	B8
2432	D2	9014	A5	9180	G7	3713	B8
2433	D4	9015	A5	9182	G8	3716	B6
2437	F2	9016	A6	9183	G9	3731	B7
2500	B4	9017	A9	9184	H1	5100	H8
2503	D3	9018	A9	9185	H9	5101	I8
2504	D4	9021	B4	9186	I7		
2505	D4	9022	A4	9239	E6		
2506	D4	9023	B5	9241	E6		
2510	C3	9024	A6	9374	G5		
2514	C4	9025	B6	9400	F1		
2515	C4	9026	B7	9401	D1		
2519	D4	9027	A7	9402	D2		
2523	D5	9028	B1	9403	C1		
2524	E5	9029	B1	9404	I4		
2606	C9	9030	B1	9707	I4		
		9031	B1	9712	H2		
		9032	B2	9801	C2		
		9033	B2	9802	E1		
		9034	B3	9803	K5		
		9035	B3	9804	F5		
		9036	B3	9805	C2		
		9037	B4	9806	B2		
		9038	B5	9807	A2		
		9039	B5	9808	F2		
		9040	B5	9809	E9		
		9041	B5	9810	F8		
		9042	B5	9811	G9		
		9043	B6	9818	C7		
		9044	B6				
		9045	B7				
		9046	C2				
		9047	B3				
		9048	B3				
		9049	B3				
		9050	C7				
		9051	B9				
		9052	C2				
		9054	C3				
		9055	C4				
		9056	C5				
		9057	C5				
		9058	C5				
		9059	C5				
		9060	C5				
		9061	C6				
		9062	C6				
		9063	C7				
		9064	C7				
		9065	C8				
		9066	C1				
		9069	C2				
		9070	C2				
		9071	C3				
		9072	C4				
		9073	C5				
		9074	C5				
		9075	C6				
		9076	C7				
		9077	C8				
		9078	C9				
		9079	C9				
		9080	D1				
		9082	D2				
		9083	D2				
		9084	D3				
		9085	D5				
		9086	D6				
		9087	D6				
		9088	D6				
		9094	D2				
		9095	D2				
		9096	D2				
		9097	D3				
		9098	D4				
		9099	D4				
		9100	D4				
		9101	D4				
		9102	D4				
		9103	D6				
		9106	D6				

Layout: Analog-Main Part (Bottom View)



2101	H2
2102	H2
2103	H2
2105	H2
2106	H2
2107	H1
2108	H1
2109	H1
2110	H1
2201	G1
2202	F1
2203	E1
2207	E1
2209	F1
2211	F2
2213	G3
2214	F2
2215	G2
2217	F3
2218	F2
2219	F2
2221	F3
2222	F3
2224	G3
2225	F3
2226	G3
2227	F3
2228	F3
2229	D1
2230	F2
2232	D1
2233	F2
2234	F2
2235	F2
2236	D1
2237	F2
2240	E2
2300	E6
2301	E6
2302	C4
2303	D4
2304	C4
2305	C4
2306	C6
2307	C4
2308	B5
2309	C5
2310	B4
2311	C3
2312	C3
2313	C4
2314	C5
2315	C6
2316	D5
2318	D5
2406	H5
2408	I5
2410	I6
2412	I6
2413	I8
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2419	E8
2422	F7
2423	F7
2426	G9
2427	G9
2430	E8
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2435	D6
2436	D8
2501	C7
2502	C7
2507	C7
2508	C7
2509	C7
2511	C7
2513	D6
2516	C6
2517	C6
2518	C6
2520	D6
2521	D6
2522	D6
2525	D5
2526	E4
2600	C1
2601	D1
2602	C1
2603	C1
2604	C1
2605	C1
2610	D1
2615	D1
2616	C1
2617	D1
2618	F1
2619	E1
2620	D1
2621	E1
2622	D1
2700	C4
2701	C3
2702	B2
2703	B2
2704	B3
2705	B3
2708	B6
2711	B6
2712	A6
2713	B4
2715	A4
2716	B3
2717	A3
2719	B4
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2723	A4
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2726	A5
2728	B4
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2902	A1
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2904	A1
2905	A1
2906	A1
2907	B1
3100	H2
3101	H2
3102	H2
3103	H2
3104	H2
3200	F1
3201	F1
3202	D2
3203	D2
3206	G1
3207	G1
3208	F1
3209	F1
3210	E1
3211	E1
3213	C4
3214	D4
3217	G1
3221	G1
3222	E4
3224	F1
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3227	F4
3229	F4
3230	B8
3233	B8
3234	F4
3238	F3
3239	A8
3240	F3
3242	F3
3243	B8
3245	B8
3246	G2
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3251	E1
3252	F3
3253	F3
3254	F3
3257	E1
3258	D1
3259	E1
3260	D1
3261	G3
3267	F1
3268	E4
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3270	F4
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3272	E3
3273	E3
3274	F3
3275	F3
3276	E3
3277	E3
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3301	C4
3302	D6
3303	D6
3304	C5
3305	C4
3306	C4
3307	C4
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3309	B5
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3311	C4
3312	C5
3314	D5
3315	D4
3316	D5
3317	C5
3319	D5
3320	D4
3321	D5
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3462	G9
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3464	G9
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3474	F6
3475	F6
3476	F6
3477	D7
3478	D7
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3507	D7
3508	D7
3509	B7
3510	B7
3511	D7
3512	C7
3513	B6
3514	D5
3515	E5
3516	D5
3517	D4
3518	D8
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3601	C1
3602	C1
3603	C1
3604	C1
3605	B1
3606	B1
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3610	C1
3611	C1
3612	B1
3613	B1
3614	H1
3615	C1
3616	D1
3617	D1
3618	E1
3619	D1
3620	C1
3621	C1
3700	C4
3701	C4
3702	D3
3703	C3
3714	A6
3715	A6
3717	B4
3718	B3
3719	B4
3720	A3
3721	A3
3722	A4
3723	A3
3724	A5
3725	A5
3726	B5
3727	B5
3728	B6
3729	B6
3730	A5
3736	C3
3737	C3
3738	C3
3800	B8
3801	B8
3802	B8
3803	A8
3804	A3
3805	A3
3806	A3
3807	A3
3808	C8
3809	C8
3810	B8
3811	B8
3900	A1
3901	A1
3902	A1
3904	A1
3905	A1
3906	A1
3907	A1
3908	A1
3909	A1
3910	A1
3911	A1
3912	A1
3913	B1
3914	A1
4001	C8
4002	C8
4003	F8
4004	B8
4005	B8
4006	D4
4007	D4
4010	F1
4011	E1
4012	E1
4013	F1
4014	D9
4240	E2
4400	I8
4401	A4
4407	E3
4418	C4
4422	C4
4423	B8
4424	A7
4425	A8
4426	A8
4427	C1
4428	C1
4429	C1
4700	C3
4804	A2
4809	B7
4810	F9
4811	H1
4812	A1
4815	B3
4816	A3
4817	H2
4818	F2
4819	C2
5102	H1
5103	H1
5104	H1
5105	H1
5802	C1
5803	C1
6200	G1
6201	G1
6202	G1
6203	F1
6204	F1
6205	F1
6206	G1
6207	G1
6208	F1
6209	F1
6210	F1
6211	E1
6215	E1
6217	F1
6218	F1
6219	G1
6220	F1
6221	F1
6406	I6
6414	F6
6415	F7
6417	F9
6421	D6
6422	D8
6500	B6
6600	D1
6601	C2
6603	C2
6604	C1
6606	C1
6607	C1
6608	D1
6609	D1
6610	E1
6700	C3
6701	C3
6703	C3
7100	H3
7202	E4
7203	B8
7205	F3
7206	F4
7208	B8
7210	F2
7212	E1
7213	E1
7217	E4
7219	F3
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7301	C5
7302	C4
7303	C5
7304	D5
7305	D5
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7307	A7
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7309	A8
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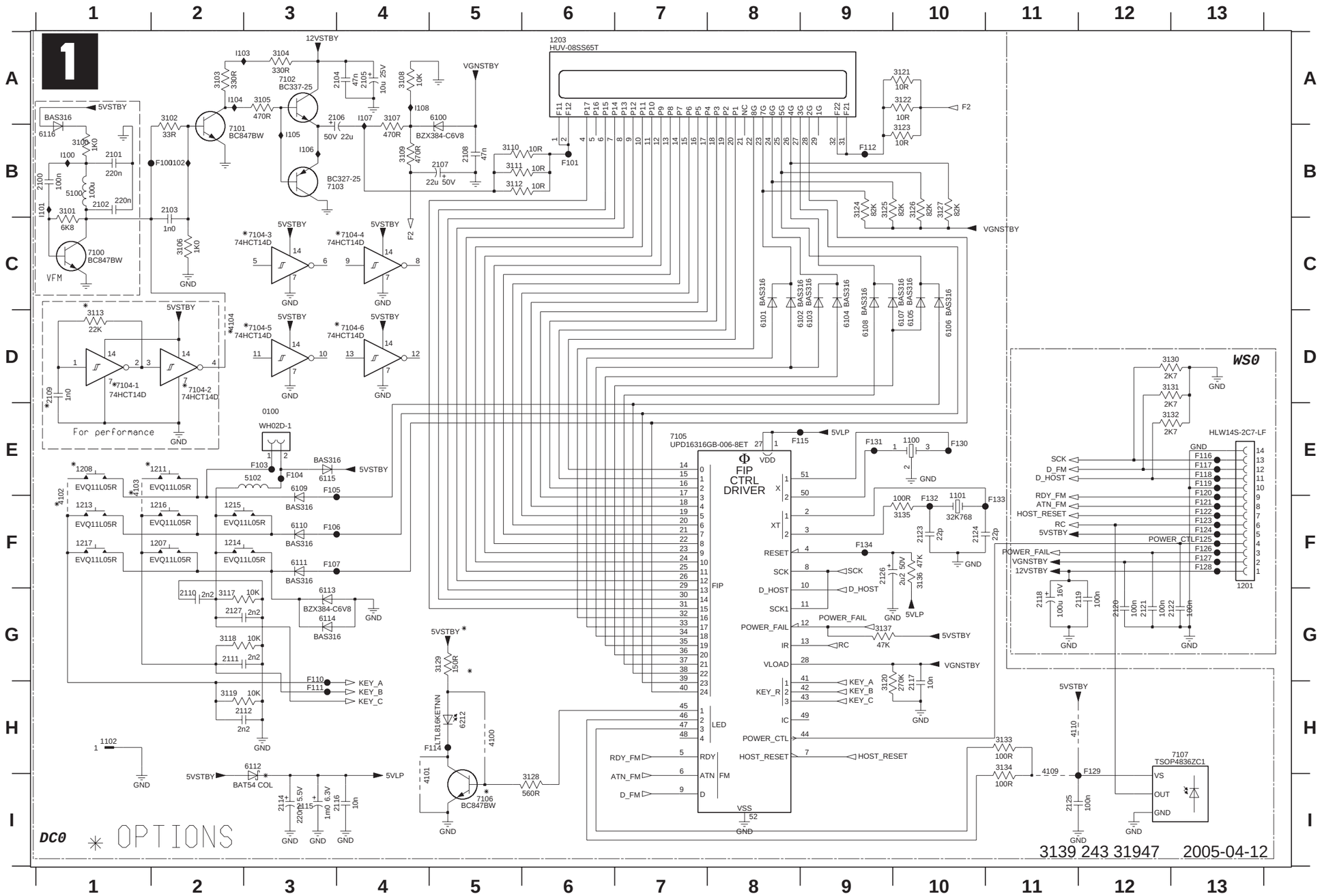
7405	F9
7406	D9
7407	D9
7408	F9
7409	E9
7410	C9
7412	F8
7414	F7
7415	A4
7416	G9
7417	H9
7420	C8
7421	C8
7423	D8
7500	C6
7501	D8
7502	D5
7503	E4
7504	D7
7600	C1
7601	C1
7602	C1
7603	C1
7604	C1
7605	C1
7606	D1
7700	D3
7701	C3
7702	C3
7703	B3
7704	A6
7705	A3
7706	A3
7800	B8
7801	B8
7802	A3
7900	A1

Front: Front Panel



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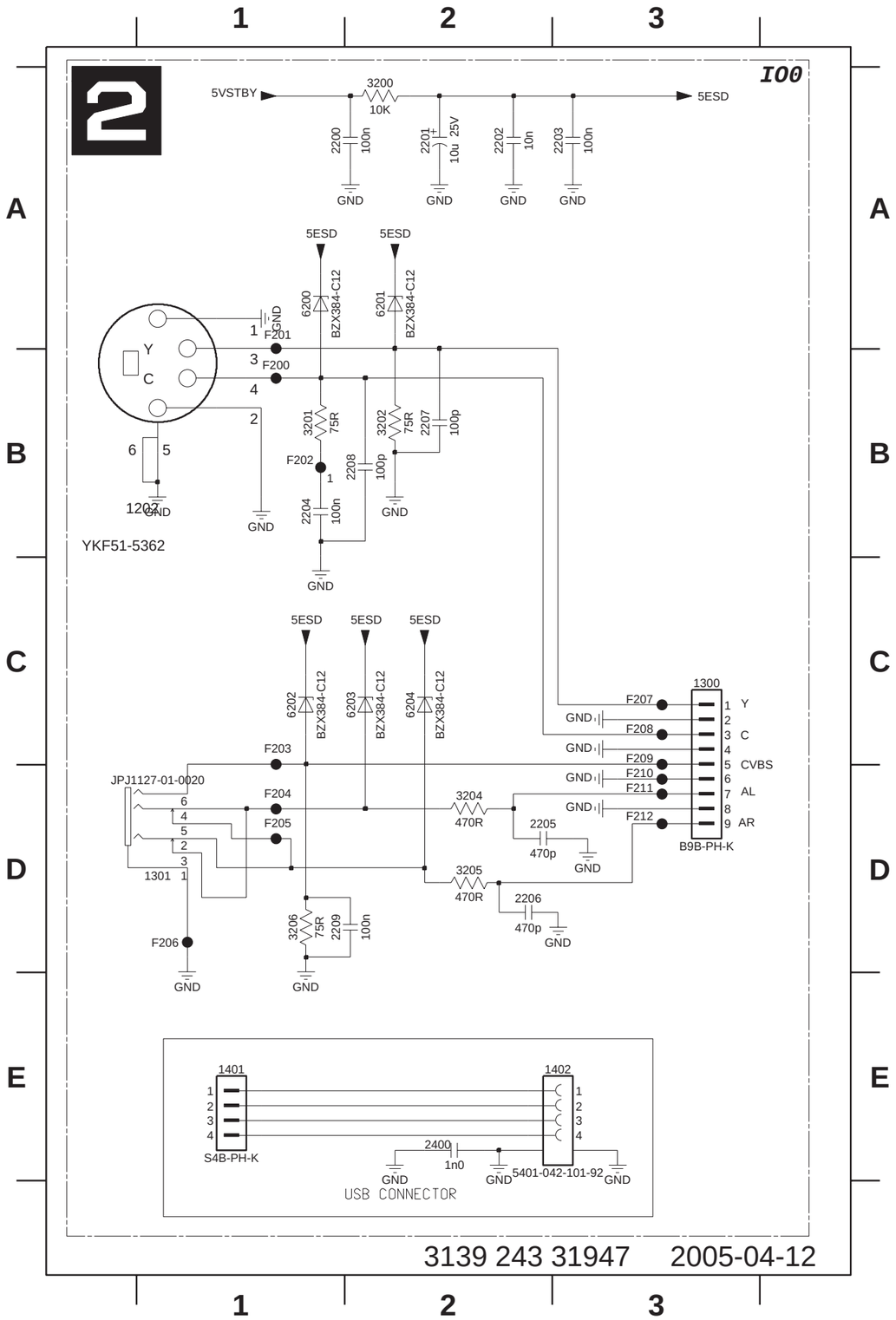
1100 E10	4102 F1	I108 A4
1101 F10	4103 E1	
1102 H1	4104 D2	
1201 F13	4109 H11	
1203 A6	4110 H11	
1207 F2	5100 B1	
1208 E1	5102 E3	
1211 E2	6100 A5	
1213 F1	6101 D8	
1214 F2	6102 D9	
1215 F2	6103 D9	
1216 F2	6104 D9	
1217 F1	6105 D10	
2100 B1	6106 D10	
2101 B1	6107 D10	
2102 B1	6108 D9	
2103 B2	6109 E3	
2104 A4	6110 F3	
2105 A4	6111 F3	
2106 A3	6112 H3	
2107 B5	6113 G3	
2108 B5	6114 G3	
2109 D1	6115 E3	
2110 G2	6116 B1	
2111 G2	6212 H5	
2112 H2	7100 C1	
2114 I3	7101 B2	
2115 I3	7102 A3	
2116 I4	7103 B3	
2117 H10	7104-1 D1	
2118 G11	7104-2 D2	
2119 G12	7104-3 C3	
2120 G12	7104-4 C4	
2121 G12	7104-5 D3	
2122 G13	7104-6 D4	
2123 F10	7105 E7	
2124 F10	7106 I5	
2125 I11	7107 H13	
2126 F9	F100 B2	
2127 G2	F101 B6	
3100 B1	F103 E3	
3101 B1	F104 E3	
3102 A2	F105 E3	
3103 A2	F106 F3	
3104 A3	F107 F3	
3105 A3	F110 H3	
3106 C2	F111 H3	
3107 A4	F112 B9	
3108 A4	F114 H5	
3109 B4	F115 E8	
3110 B5	F116 E13	
3111 B5	F117 E13	
3112 B5	F118 E13	
3113 D1	F119 E13	
3117 G2	F120 E13	
3118 G2	F121 F13	
3119 H2	F122 F13	
3120 H9	F123 F13	
3121 A10	F124 F13	
3122 A10	F125 F13	
3123 B10	F126 F13	
3124 B9	F127 F13	
3125 B9	F128 F13	
3126 B10	F129 H12	
3127 B10	F130 E10	
3128 I6	F131 E9	
3129 G5	F132 F10	
3130 D12	F133 F11	
3131 D12	F134 F9	
3132 E12	I100 B1	
3133 H11	I101 B1	
3134 H11	I102 B2	
3135 F10	I103 A2	
3136 F10	I104 A2	
3137 G9	I105 B3	
4100 H5	I106 B3	

Front: Front Panel



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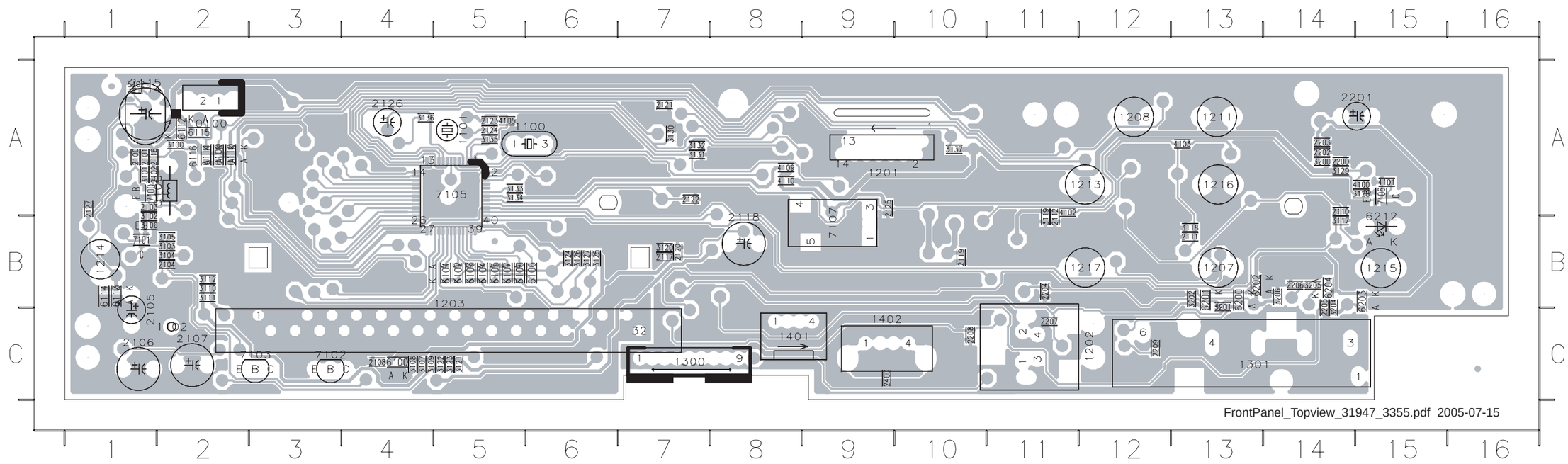
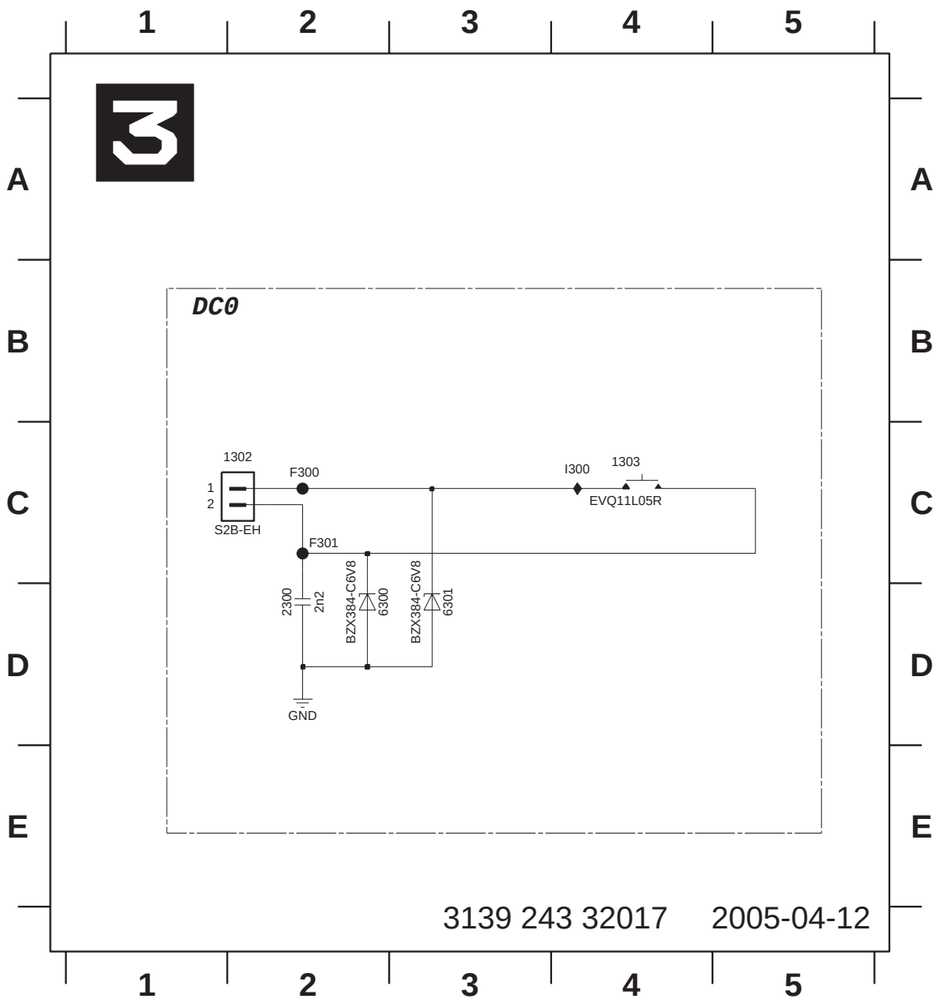
1300 C3
1301 D1
1401 E1
1402 E3
2200 A1
2201 A2
2202 A2
2203 A3
2204 B1
2205 D2
2206 D2
2207 B2
2208 B2
2209 D1
2400 E2
3200 A2
3201 B1
3202 B2
3204 D2
3205 D2
3206 D1
6200 A1
6201 A2
6202 C1
6203 C2
6204 C2
F200 B1
F201 A1
F202 B1
F203 C1
F204 D1
F205 D1
F206 D1
F207 C3
F208 C3
F209 C3
F210 D3
F211 D3
F212 D3

Layout: Front Panel (Top View)

0100 A2	1211 A13	1402 C9	2108 C4	2119 B10	2200 A14	2209 C12	3107 C4	3120 B7	3129 A14	3200 A14	4103 A13	6103 B5	6112 A2	6204 B14
1100 A6	1213 A12	2100 A1	2110 A14	2120 B7	2201 A15	2400 C9	3108 C4	3121 C5	3130 A7	3201 B13	4105 A5	6104 B5	6113 B1	6212 B15
1101 A5	1214 B1	2101 A1	2111 B13	2121 A7	2202 A14	3100 A2	3109 C4	3122 C5	3131 A7	3202 B13	4109 A8	6105 B5	6114 B1	7100 A1
1102 C2	1215 B15	2102 A1	2112 B11	2122 A7	2203 A14	3101 A1	3110 B2	3123 C5	3132 A7	3204 B14	4110 A8	6106 B6	6115 A2	7101 B1
1201 A9	1216 A13	2103 A1	2114 A1	2123 A5	2204 B11	3102 B1	3111 B2	3124 B6	3133 A5	3205 B14	5100 A2	6107 B5	6116 A2	7102 C3
1202 C12	1217 B12	2104 B2	2115 A1	2124 A5	2205 B14	3103 B2	3112 B2	3125 B6	3134 A5	3206 B14	5102 A1	6108 B5	6200 B13	7103 C3
1203 B5	1300 C7	2105 C1	2116 A1	2125 A9	2206 B14	3104 B2	3117 B14	3126 B6	3135 A5	4100 A15	6100 C4	6109 A2	6201 B13	7105 A5
1207 B13	1301 C13	2106 C1	2117 B7	2126 A4	2207 C11	3105 B2	3118 B13	3127 B6	3136 A4	4101 A15	6101 B5	6110 A2	6202 B13	7106 A15
1208 A12	1401 C8	2107 C2	2118 B8	2127 A1	2208 C10	3106 B1	3119 B11	3128 A15	3137 A10	4102 A11	6102 B5	6111 A2	6203 B15	7107 B9

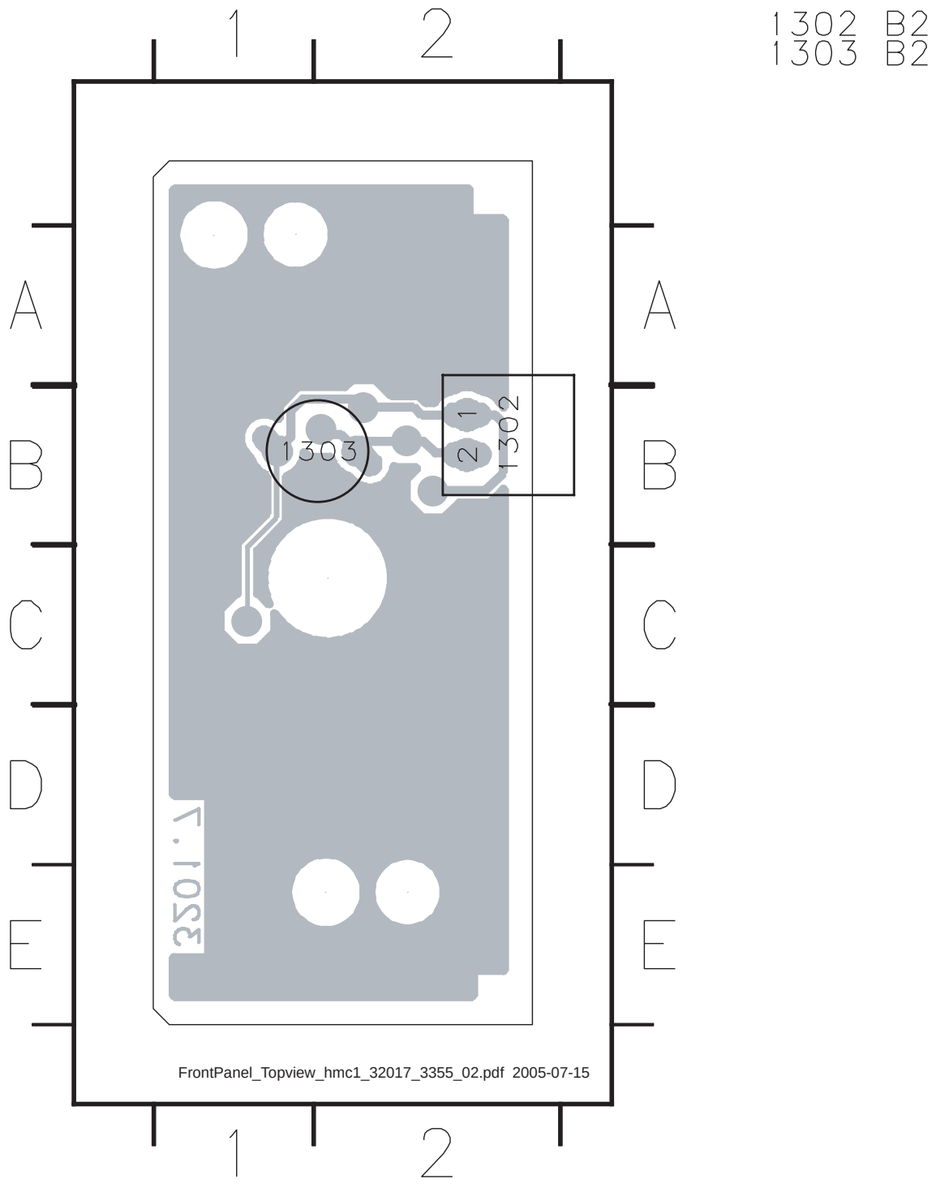


Front: Standby



1302 C2
1303 C4
2300 D2
6300 D2
6301 D3
F300 C2
F301 C2
I300 C4

Layout: Standby (Top View)



1302 B2
1303 B2

Digital: Back-End Processor

1 Back-end Processor

2 Back-end Flash (BEF)

5 Communication (COM)

5 Audio (AUD)

5 Back-end Front-end Interface (IDE)

4 Video Input Digital (VID)

2 Back-end SDRAM (BES)

3 IEEE1394 Link - Physical (LNK)

FC: DM3

FC: DA0

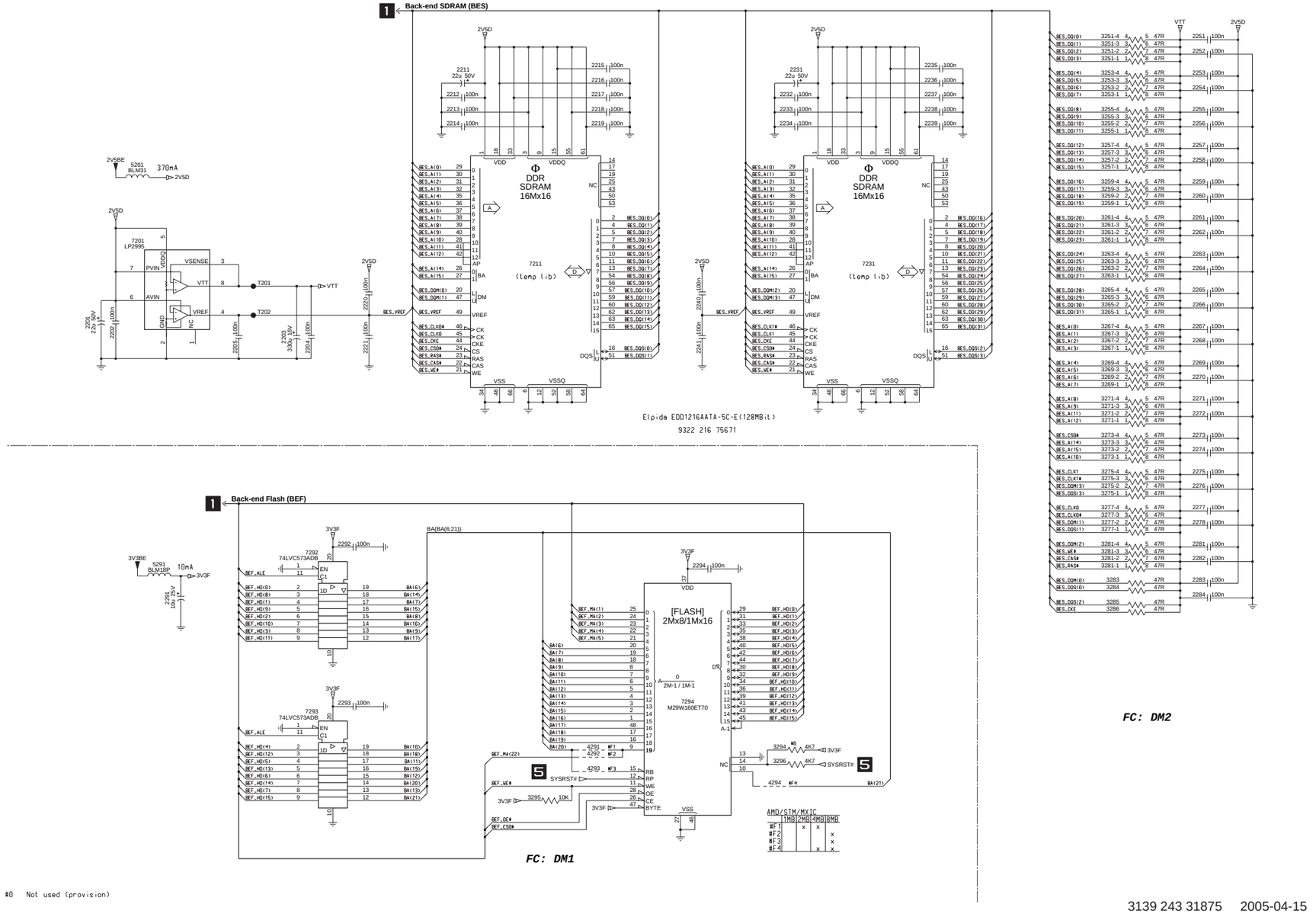
#0 Not used (provision)

3139 243 31875 2005-04-15

1101 B10	3176-4 H1
1111 E10	3177-1 I1
2101 B10	3177-2 I1
2102 B11	3177-3 I1
2105 G12	3177-4 I1
2108 F1	3178-1 I1
2109 F2	3178-2 I1
2120 B6	3178-3 I1
2121 F9	3178-4 I1
2122 F9	3181-1 G4
2123 F9	3181-2 G4
2124 F9	3181-3 H4
2125 F9	3181-4 H4
2126 F10	3182-1 G4
2127 F10	3182-2 H4
2128 F10	3182-3 G4
2129 F10	3182-4 H4
2130 F10	3183-1 G4
2131 G8	3183-2 G4
2141 G9	3183-3 H4
2142 G9	3183-4 G4
2143 G10	3184-1 G4
2144 G10	3184-2 G4
2145 G10	3184-3 G4
2146 G10	3184-4 G4
2147 G10	3185-1 H4
2151 H10	3185-2 I4
2152 I10	3185-3 I4
2153 I10	3185-4 H4
2154 I10	3186-1 H4
2155 I10	3186-2 I4
2156 I10	3186-3 H4
2157 I11	3186-4 H4
2158 I11	3187-1 I4
2161 I12	3187-2 I4
2162 I12	3187-3 I4
2171 I10	3187-4 H4
2172 I10	3188-1 I4
2173 I10	3188-2 I4
2174 I10	3188-3 I4
2175 I10	3188-4 I4
2176 I10	3191 H8
2181 I11	3192 F12
2182 I12	3193 F12
2183 I12	3194 F12
2191 I12	3195 F12
2199 E11	3196 F12
3101 B1	3197 E12
3102 B1	3198 E12
3103 B1	3199 E11
3104 C1	5121 F9
3111 D5	5131 G8
3112 D6	5141 G9
3113 D6	5151 H10
3114 D6	5161 H11
3121 B6	5162 H12
3122 B6	5171 I10
3123 B6	5181 I11
3124 A9	6101 C3
3125 B9	7101-1 D5
3131 C9	7101-10 I7
3132 C9	7101-2 A5
3133 C9	7101-3 B12
3134 C9	7101-4 A2
3135 C9	7101-5 F7
3136 C9	7101-6 D2
3137 C9	7101-7 A8
3138 C9	7101-8 F3
3139 D9	7101-9 A12
3141 E7	7105 G12
3142 E8	7111-1 E12
3143 E7	7111-2 F13
3144 E8	F101 B6
3145 E7	F102 B6
3146 E8	F103 B6
3147 E7	T101 B1
3148 E8	T102 B1
3149 E7	T103 B1
3150 E8	T104 B1
3151 E7	T105 B1
3152 E8	T106 B1
3153 E7	T111 E11
3154 E8	T112 E11
3155 E7	T113 E11
3156 E8	T121 A11
3161 A11	T122 B11
3162 B12	
3163 B10	
3164 C10	
3165 C10	
3166 C10	
3167 C10	
3168 G13	
3169 H13	
3171-1 G1	
3171-2 G1	
3171-3 G1	
3171-4 G1	
3172-1 G1	
3172-2 G1	
3172-3 G1	
3172-4 G1	
3173-1 G1	
3173-2 G1	
3173-3 H1	
3173-4 H1	
3174-1 H1	
3174-2 H1	
3174-3 H1	
3174-4 H1	
3175-1 H1	
3175-2 H1	
3175-3 H1	
3175-4 H1	
3176-1 H1	
3176-2 H1	
3176-3 H1	

Digital: Memory

2 Memory



3139 243 31875 2005-04-15

2201 D1
2202 D2
2203 D3
2204 D4
2205 D3
2211 B5
2212 B5
2213 B5
2214 B5
2215 A7
2216 B7
2217 B7
2218 B7
2219 B7
2220 D4
2221 D4
2231 B8
2232 B8
2233 B8
2234 B8
2235 A10
2236 B10
2237 B10
2238 B10
2239 B10
2240 D8
2241 D8
2251 A12
2252 A12
2253 B12
2254 B12
2255 B12
2256 B12
2257 B12
2258 B12
2259 C12
2260 C12
2261 C12
2262 C12
2263 C12
2264 C12
2265 D12
2266 D12
2267 D12
2268 D12
2269 D12
2270 E12
2271 E12
2272 E12
2273 E12
2274 E12
2275 E12
2276 F12
2277 F12
2278 F12
2281 F12
2282 F12
2283 G12
2284 G12
2291 G2
2292 F4
2293 H4
2294 F8
3251-1 A12
3251-2 A12
3251-3 A12
3251-4 A12
3253-1 B12
3253-2 B12
3253-3 B12
3253-4 B12
3255-1 B12
3255-2 B12
3255-3 B12
3255-4 B12
3257-1 B12
3257-2 B12
3257-3 B12
3257-4 B12
3259-1 C12
3259-2 C12
3259-3 C12
3259-4 C12
3261-1 C12
3261-2 C12
3261-3 C12
3261-4 C12
3263-1 D12
3263-2 C12
3263-3 C12
3263-4 C12
3265-1 D12
3265-2 D12
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3265-4 D12
3267-1 D12
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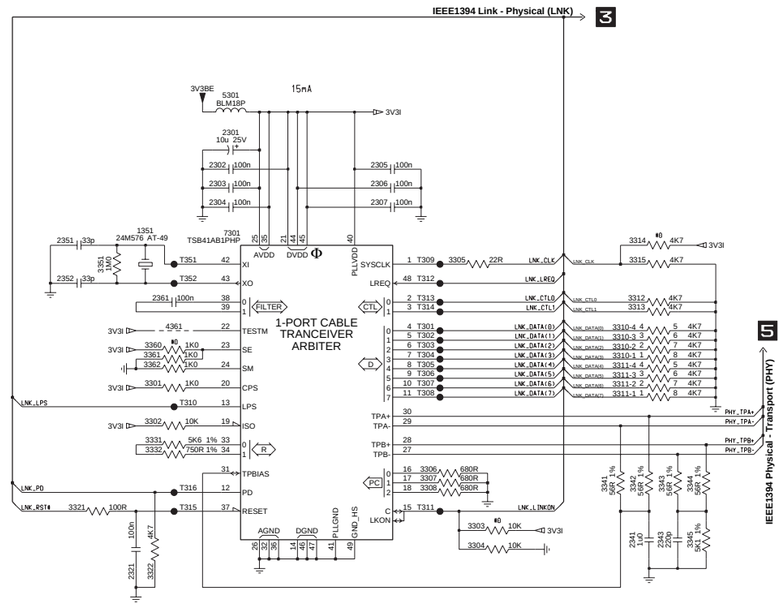
3273-3 E12
3273-4 E12
3275-1 F12
3275-2 F12
3275-3 F12
3275-4 E12
3277-1 F12
3277-2 F12
3277-3 F12
3277-4 F12
3281-1 F12
3281-2 F12
3281-3 F12
3281-4 F12
3283 G12
3284 G12
3285 G12
3286 G12
3294 H8
3295 I6
3296 H8
4291 H6
4292 H6
4293 H6
4294 I8
5201 B2
5291 F2
7201 C2
7211 C6
7231 C9
7292 F4
7293 H4
7294 H7
T201 D3
T202 D3

Digital: IEEE 1394 Physical Layer

3 IEEE1394 Physical Layer



FC: ME0

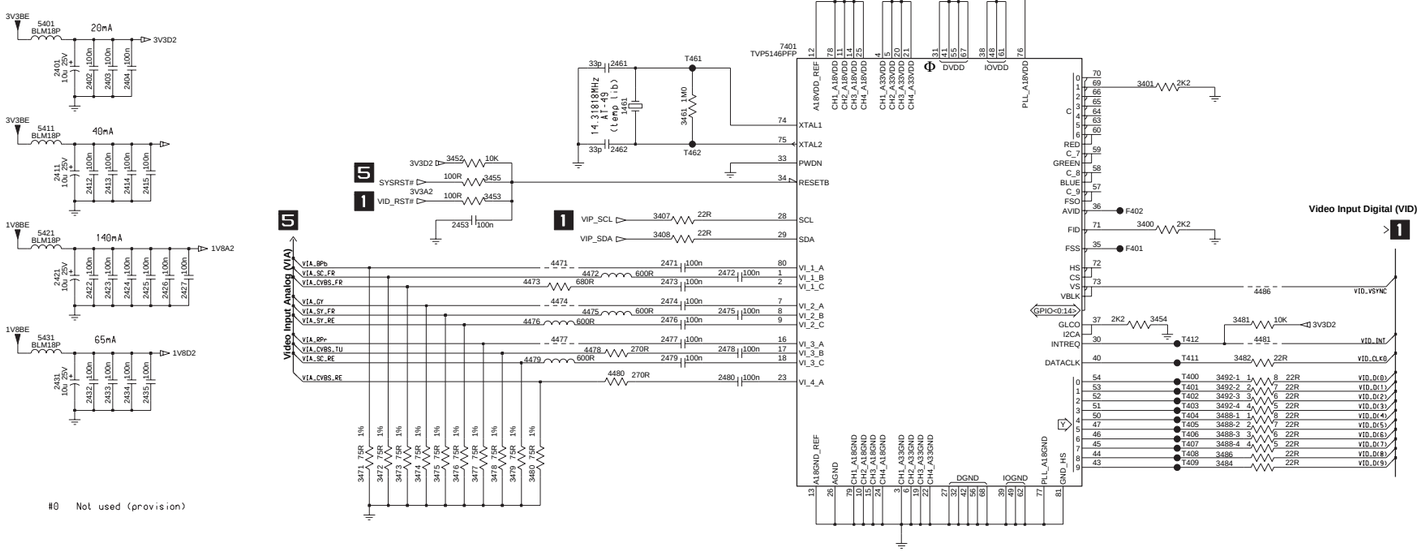
#0 Not used (provision)

3139 243 31875 2005-04-15

1351 D5
2301 D6
2302 D6
2303 D6
2304 D6
2305 D7
2306 D7
2307 D7
2321 G5
2341 G9
2343 G9
2351 D5
2352 E5
2361 E5
3301 E5
3302 F5
3303 G8
3304 G8
3305 E8
3306 F7
3307 F7
3308 F7
3310-1 E9
3310-2 E9
3310-3 E9
3310-4 E9
3311-1 E9
3311-2 E9
3311-3 E9
3311-4 F9
3312 E9
3313 E9
3314 D9
3315 E9
3321 F5
3322 G5
3331 F5
3332 F5
3341 F9
3342 F9
3343 F9
3344 F9
3345 G9
3351 E5
3360 E5
3361 E5
3362 E5
4361 E5
5301 C6
7301 D6
T301 E7
T302 E7
T303 E7
T304 E7
T305 E7
T306 E7
T307 E7
T308 F7
T309 E7
T310 F5
T311 F7
T312 E7
T313 E7
T314 E7
T315 F5
T316 F5
T351 E5
T352 E5

Digital: Video Input Processor

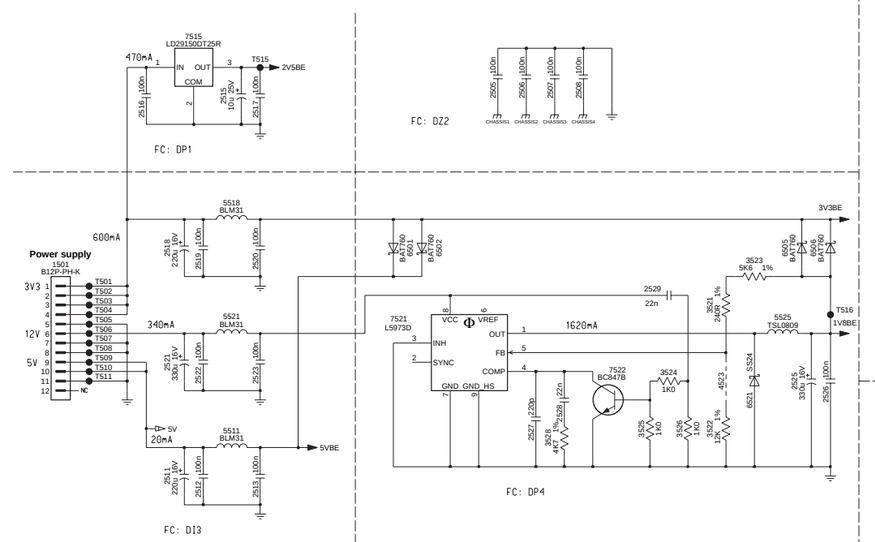
4 Video Input Processor

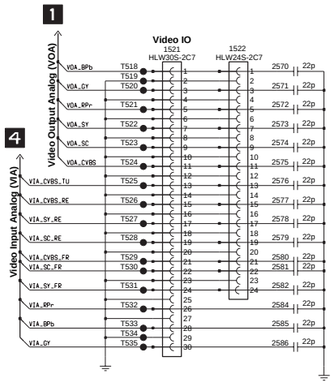


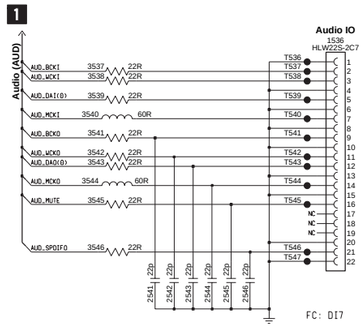
1461 C6
2401 C2
2402 C2
2403 C2
2404 C2
2411 D2
2412 D2
2413 D2
2414 D2
2415 D2
2421 E2
2422 E2
2423 E2
2424 E2
2425 E2
2426 E3
2427 E3
2431 E2
2432 F2
2433 F2
2434 F2
2435 F2
2453 D5
2461 C6
2462 D6
2471 E6
2472 E7
2473 E6
2474 E6
2475 E7
2476 E6
2477 E6
2478 E7
2479 E6
2480 E7
3400 D10
3401 C10
3407 D6
3408 D6
3452 D5
3453 D5
3454 E10
3455 D5
3461 C7
3471 F4
3472 F4
3473 F4
3474 F5
3475 F5
3476 F5
3477 F5
3478 F5
3479 F5
3480 F5
3481 E11
3482 E11
3484 F11
3486 F11
3488-1 F11
3488-2 F11
3488-3 F11
3488-4 F11
3492-1 E11
3492-2 F11
3492-3 F11
3492-4 F11
4471 E6
4472 E6
4473 E5
4474 E6
4475 E6
4476 E5
4477 E6
4478 E6
4479 E5
4480 E6
4481 E11
4486 E11
5401 C2
5411 D2
5421 D2
5431 E2
7401 C7
F401 D10
F402 D10
T400 E10
T401 F10
T402 F10
T403 F10
T404 F10
T405 F10
T406 F10
T407 F10
T408 F10
T409 F10
T411 E10
T412 E10
T461 C7
T462 D7

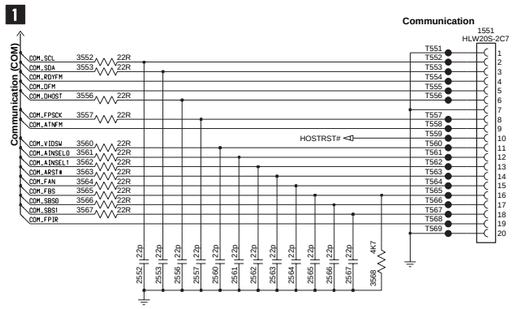
Digital: Interfaces

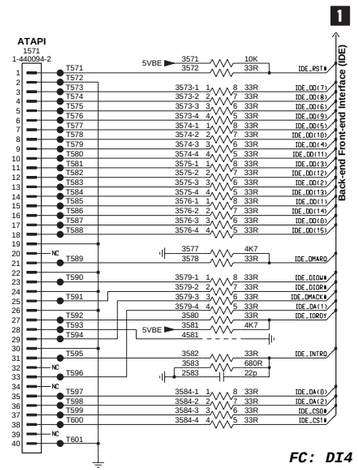
5 Interfaces

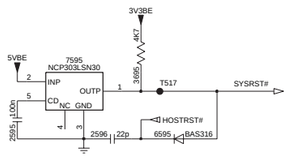


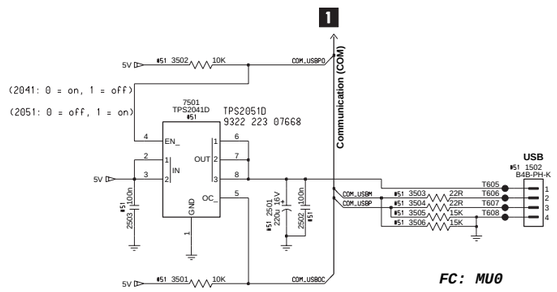


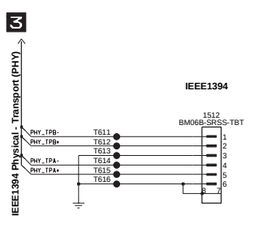












#0 Not used (provision)

#51 USB circuit, for version with USB feature only

3139 243 31875 2005-04-15

1501 C1
1502 H9
1512 H12
1521 A9
1522 A9
1536 A13
1551 D12
1571 F1
2501 I7
2502 I7
2503 I6
2505 B4
2506 B4
2507 B5
2508 B5
2511 D2
2512 E2
2513 E2
2515 B2
2516 B2
2517 B2
2518 C2
2519 C2
2520 C2
2521 D2
2522 D2
2523 D2
2525 D6
2526 D7
2527 D4
2528 D5
2529 C5
2541 C11
2542 C12
2543 C12
2544 C12
2545 C12
2546 C12
2552 F9
2553 F9
2556 F10
2557 F10
2560 F10
2561 F10
2562 F10
2563 F10
2564 F10
2565 F11
2566 F11
2567 F11
2570 A9
2571 A9
2572 A9
2573 B9
2574 B9
2575 B9
2576 B9
2577 B9
2578 B9
2579 B9
2580 C9
2581 C9
2582 C9
2583 H2
2584 C9
2585 C9
2586 C9
2595 F5
2596 F5
3501 I6
3502 H6
3503 I8
3504 I8
3505 I8
3506 I8
3521 C6
3522 D6
3523 C6
3524 D5
3525 D5
3526 D6
3528 D5
3537 A11
3538 A11
3539 A11
3540 A11
3541 B11
3542 B11
3543 B11
3544 B11
3545 B11
3546 B11
3552 D9
3553 E9
3556 E9
3557 E9
3560 E9
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3562 E9
3563 E9
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3565 E9
3566 F9
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3581 H2
3582 H2
3583 H2
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3584-4 I2
3695 F6
4523 D6
4581 H2
5511 D2
5518 B2
5521 C2
5525 C6
6501 C4
6502 C4
6505 C6
6506 C7
6521 D6
6595 F6
7501 H6
7515 A2
7521 C3
7522 D5
7595 F5
T501 C1
T502 C1
T503 C1
T504 C1
T505 C1
T506 C1
T507 C1
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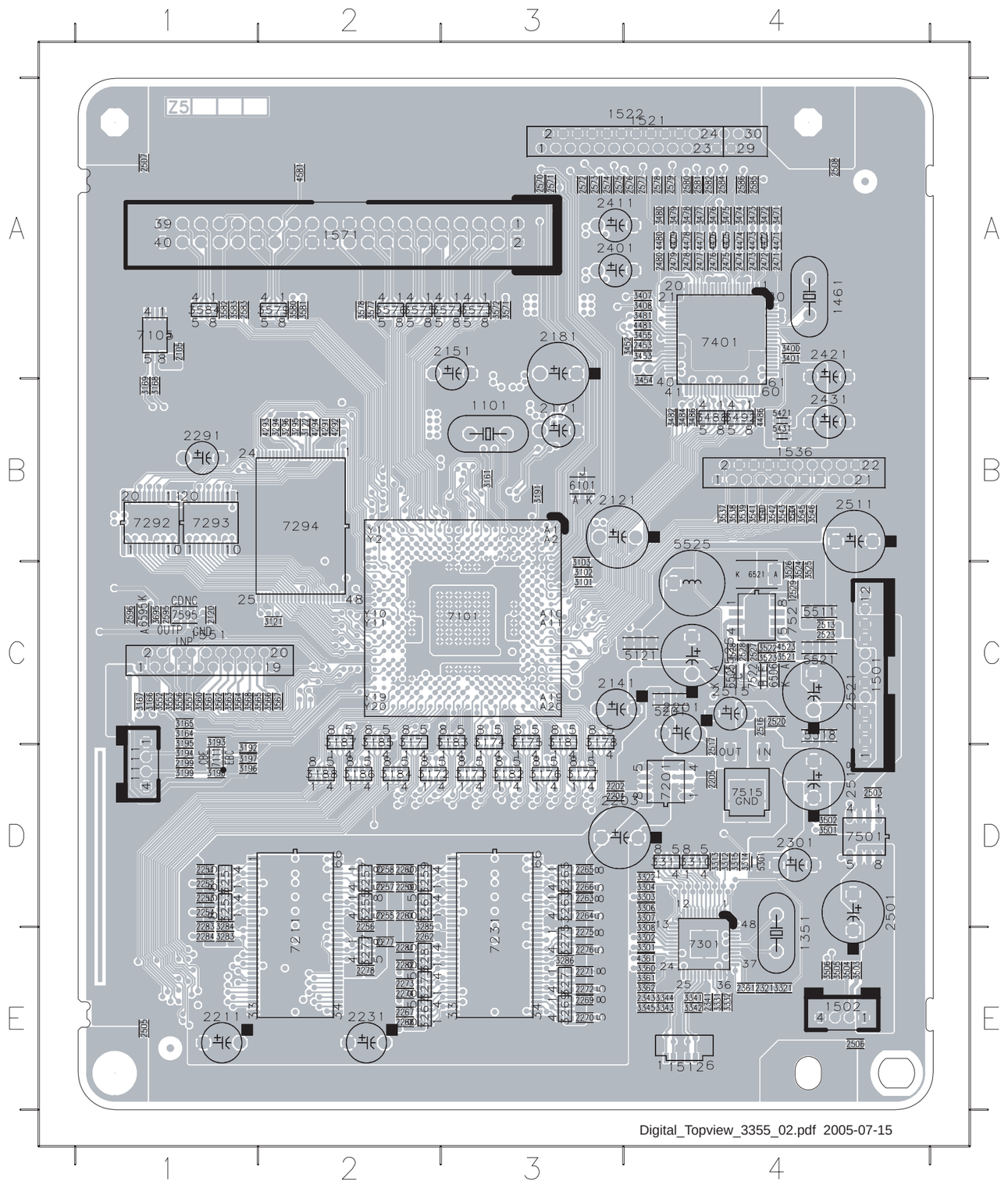
T600 I1
T601 I1
T605 H8
T606 I8
T607 I8
T608 I8
T611 H11
T612 H11
T613 H11
T614 H11
T615 H11
T616 I11

Layout: Digital-Main Part (Top View)



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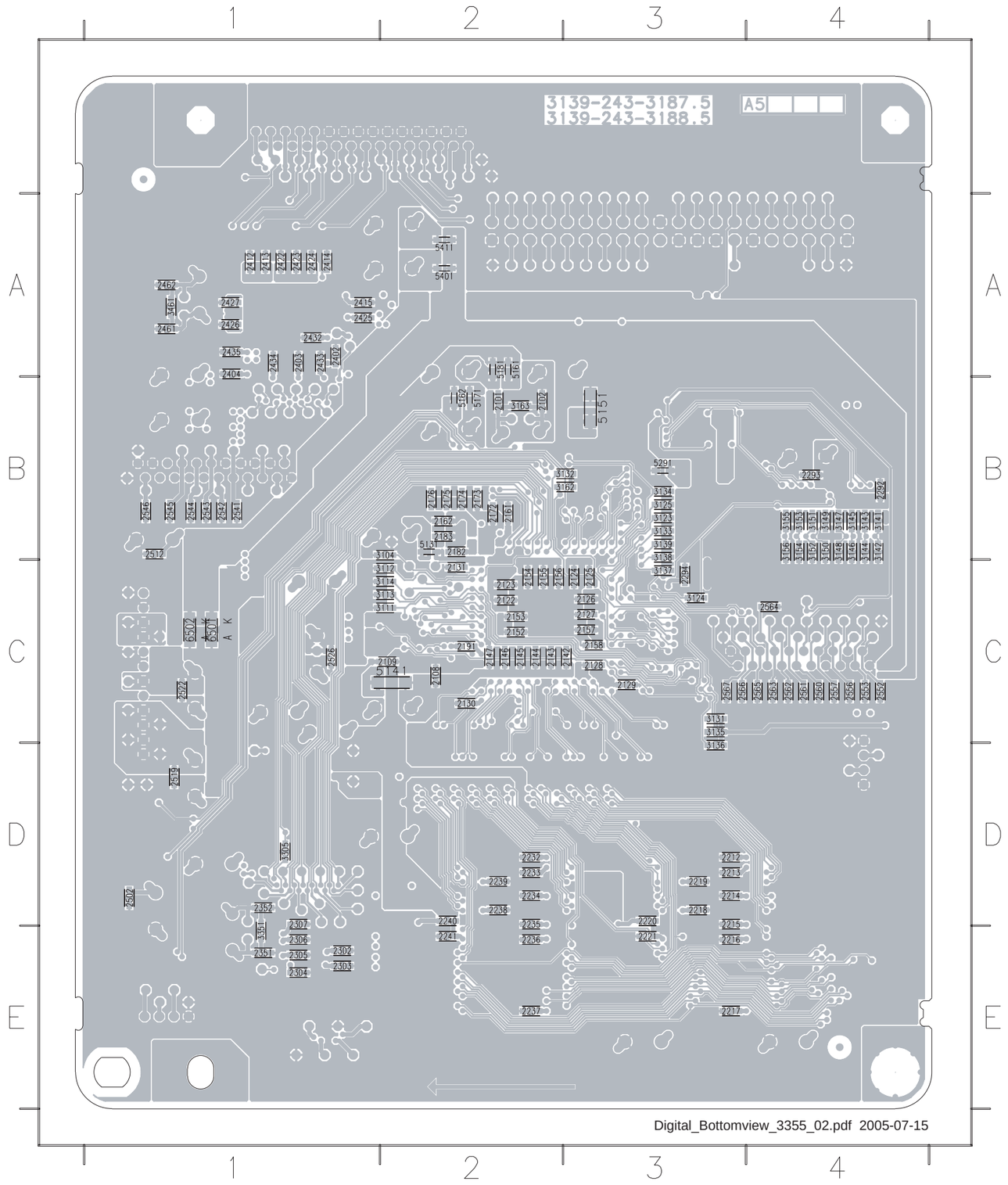
1111	D1	2513	C4	3286	E3	3566	C2
1351	E4	2515	C4	3294	B2	3567	C2
1461	A4	2516	C4	3295	B2	3568	C1
1501	C4	2517	D4	3296	B2	3571	A3
1502	E4	2518	D4	3301	E4	3572	A3
1512	E4	2520	C4	3302	E4	3573	A3
1521	A4	2521	C4	3303	D4	3574	A3
1522	A4	2523	C4	3304	D4	3575	A2
1536	B4	2525	C4	3306	D4	3576	A2
1551	C1	2527	C4	3307	D4	3577	A2
1571	A2	2528	C4	3308	E4	3578	A2
2105	A1	2529	C4	3310	D4	3579	A2
2120	C1	2570	A3	3311	D4	3580	A2
2121	B3	2571	A3	3312	D4	3581	A2
2141	C3	2572	A3	3313	D4	3582	A1
2151	A3	2573	A3	3314	D4	3583	A1
2171	B3	2574	A3	3315	D4	3584	A1
2181	A3	2575	A3	3321	E4	3695	C1
2199	D1	2576	A4	3322	D4	4291	B2
2201	C4	2577	A4	3331	E4	4292	B2
2202	D3	2578	A4	3332	E4	4293	B2
2203	D3	2579	A4	3341	E4	4294	B2
2204	D3	2580	A4	3342	E4	4361	E4
2205	D4	2581	A4	3343	E4	4471	A4
2211	E1	2582	A4	3344	E4	4472	A4
2231	E2	2583	A1	3345	E4	4473	A4
2251	D1	2584	A4	3360	E4	4474	A4
2252	D1	2585	A4	3361	E4	4475	A4
2253	D1	2586	A4	3362	E4	4476	A4
2254	D1	2595	C1	3400	A4	4477	A4
2255	D2	2596	C1	3401	A4	4478	A4
2256	D2	3101	C3	3407	A4	4479	A4
2257	D2	3102	C3	3408	A4	4480	A4
2258	D2	3103	C3	3452	A4	4481	A4
2259	D2	3121	C2	3453	A4	4486	B4
2260	D2	3122	B2	3454	B4	4523	C4
2261	D2	3161	B3	3455	A4	4581	A2
2262	E2	3164	C1	3471	A4	5121	C4
2263	D3	3165	C1	3472	A4	5201	C4
2264	D3	3166	C1	3473	A4	5301	D4
2265	D3	3167	C1	3474	A4	5421	B4
2266	D3	3168	B1	3475	A4	5431	B4
2267	E2	3169	B1	3476	A4	5511	C4
2268	E2	3171	C2	3477	A4	5518	C4
2269	E3	3172	D2	3478	A4	5521	C4
2270	E3	3173	D3	3479	A4	5525	B4
2271	E3	3174	C3	3480	A4	6101	B3
2272	E3	3175	C3	3481	A4	6505	C4
2273	E2	3176	D3	3482	B4	6506	C4
2274	E2	3177	D3	3484	B4	6521	C4
2275	E3	3178	C3	3486	B4	6595	C1
2276	E3	3181	C3	3488	B4	7101	C3
2277	E3	3182	D3	3492	B4	7105	A1
2278	E2	3183	C3	3501	D4	7111	D1
2281	E2	3184	D2	3502	D4	7201	D4
2282	E2	3185	C2	3503	E4	7211	E2
2283	D1	3186	D2	3504	E4	7231	E3
2284	E1	3187	C2	3505	E4	7292	B1
2291	B1	3188	D2	3506	E4	7293	B1
2301	D4	3191	B3	3521	C4	7294	B2
2321	E4	3192	D1	3522	C4	7301	E4
2341	E4	3193	C1	3523	C4	7401	A4
2343	E4	3194	D1	3524	C4	7501	D4
2361	E4	3195	C1	3525	C4	7515	D4
2401	A3	3196	D1	3526	C4	7521	C4
2411	A3	3197	D1	3528	C4	7522	C4
2421	A4	3198	D1	3537	B4	7595	C1
2431	B4	3199	D1	3538	B4		
2453	A4	3251	D1	3539	B4		
2471	A4	3253	D1	3540	B4		
2472	A4	3255	D2	3541	B4		
2473	A4	3257	D2	3542	B4		
2474	A4	3259	D2	3543	B4		
2475	A4	3261	D2	3544	B4		
2476	A4	3263	D3	3545	B4		
2477	A4	3265	D3	3546	B4		
2478	A4	3267	E2	3552	C1		
2479	A4	3269	E3	3553	C1		
2480	A4	3271	E3	3556	C1		
2501	D4	3273	E2	3557	C1		
2503	D4	3275	E3	3560	C1		
2505	E1	3277	E2	3561	C1		
2506	E4	3281	E2	3562	C1		
2507	A1	3283	E1	3563	C1		
2508	A4	3284	D1	3564	C1		

Layout: Digital-Main Part (Bottom View)



Digital_Bottomview_3355_02.pdf 2005-07-15

2101	B2	2462	A1
2102	B2	2502	D1
2108	C2	2512	B1
2109	C2	2519	D1
2122	C2	2522	C1
2123	C2	2526	C1
2124	C3	2541	B1
2125	C3	2542	B1
2126	C3	2543	B1
2127	C3	2544	B1
2128	C3	2545	B1
2129	C3	2546	B1
2130	C2	2552	C4
2131	C2	2553	C4
2142	C3	2556	C4
2143	C2	2557	C4
2144	C2	2560	C4
2145	C2	2561	C4
2146	C2	2562	C4
2147	C2	2563	C4
2152	C2	2564	C4
2153	C2	2565	C4
2154	C2	2566	C3
2155	C2	2567	C3
2156	C2	3104	B2
2157	C3	3111	C2
2158	C3	3112	C2
2161	B2	3113	C2
2162	B2	3114	C2
2172	B2	3123	B3
2173	B2	3124	C3
2174	B2	3125	B3
2175	B2	3131	C3
2176	B2	3132	B3
2182	B2	3133	B3
2183	B2	3134	B3
2191	C2	3135	C3
2212	D3	3136	D3
2213	D3	3137	C3
2214	D3	3138	B3
2215	D3	3139	B3
2216	E3	3141	B4
2217	E3	3142	B4
2218	D3	3143	B4
2219	D3	3144	B4
2220	D3	3145	B4
2221	E3	3146	B4
2232	D2	3147	B4
2233	D2	3148	B4
2234	D2	3149	B4
2235	D2	3150	B4
2236	E2	3151	B4
2237	E2	3152	B4
2238	D2	3153	B4
2239	D2	3154	B4
2240	D2	3155	B4
2241	E2	3156	B4
2292	B4	3162	B3
2293	B4	3163	B2
2294	C3	3305	D1
2302	E1	3351	E1
2303	E1	3461	A1
2304	E1	5131	B2
2305	E1	5141	C2
2306	E1	5151	B3
2307	D1	5161	A2
2351	E1	5162	B2
2352	D1	5171	B2
2402	A1	5181	A2
2403	A1	5291	B3
2404	A1	5401	A2
2412	A1	5411	A2
2413	A1	6501	C1
2414	A1	6502	C1
2415	A1		
2422	A1		
2423	A1		
2424	A1		
2425	A1		
2426	A1		
2427	A1		
2432	A1		
2433	A1		
2434	A1		
2435	A1		
2461	A1		

Notes:

8. Circuit- and IC description

8.1. Front Board (Panel – Display + Key)

8.1.1. General

This board consists of the following parts:
- Slave µP
- Frontend (Audio & Video)
- VFD Heater voltage Generator

8.1.2. Slave µP (IC 7105: UPD16316GB)

The core element of the Front Display + Keyboard is the slave µP. It runs on a 5V supply and is responsible for the following functions:
- Interface with the Domino chip on the Digital Board
- Evaluation of the keyboard matrix within Front board
- Decoding the remote control commands from the infra-red receiver
- Activation and control of the display
- Timer Wake-up activation

It runs on two clock frequencies namely:
- 5MHz for normal operation
- 32.768KHz for the real time clock

8.1.3. Interface to the Domino chip

It communicates with the Domino Host on the Digital board via a 6-wire synchronous serial interface. The Host is always the master to generate the communication clock to the slave µP irrespective of the direction of data transfer.

8.1.4. Evaluation of the keyboard matrix

A key matrix is used on the Front board. The slave µP does the key scanning with FIP9 - FIP24 (pin 23-26 and 29-40) as output and KEY_A - KEY_C (pin 41-43) as input. Each key is assigned a key code based on the output and input ports, and the slave µP will do the evaluation by getting the key codes.

8.1.5. IR receiver and signal evaluation

The IR receiver on the Front Board contains a selectively controlled amplifier as well as a photodiode. The photo-diode changes the received infrared transmission to electrical pulses, which are then amplified and demodulated. On the output of the IR receiver, a pulse sequence with TTL-level, which corresponds to the envelope curve of the received IR remote control command, can be measured. This pulse sequence is fed into the slave µP for further processing via pin 13.

8.1.6. Vacuum Fluorescent Display [1203: HUV-08SS65T]

The VFD is fully controlled and driven by the slave µP.

8.1.7. VFD Heater Voltage Generator

The oscillator circuit provided by [5100, 2101, 2102 & 7100] provides the necessary sine wave signal for transistors [7101, 7102 & 7103] to generate the 50% duty-cycle 48KHz AC square-wave signal for the filament of the VFD.

8.1.8. Timer Wake-up activation

During the Standby mode, the slave µP provides a wakeup call (POWER_CTL-line switches to high) to the Domino Host on the Digital Board. It will then starts up and asks for the wake-up reason.

8.2. Analog Board

8.2.1. General

The pc board consist of the following parts:
- Fan Control (OPTION)
- Power Supply Unit
- Tuner Frontend
- Audio ADC/DAC

8.2.2. Fan Control

The Laser on the OPU of the drive is very sensitive to temperature. A fan control circuit [7802 & 7803] is built into the board as a provision. The fan is ON when the set is in active mode, and OFF when the tray opens. When the set is in Standby mode, the fan is switched off. The control of the fan is coming from the Digital Board.

8.2.3. Power Supply Unit

This power supply functions on a circuitry combination of a SMPS control IC [7400], switching FET [7401] and transformer [5400] as a switched-mode power supply (SMPS).
Feedback control is provided by the IC 7404, which compares the 5V-output voltage via voltage dividers [3421, 3422 & 3423] with an internal 2.5V reference voltage. The output voltage is fed to an optocoupler [7403] that provide the insulation between the primary and secondary parts as a current value into pin 3 of the IC 7400.

The following are the various supply lines provided:
- 3V3SW to CU, DAC_ADC, Digital Board
- 5V to IOA, IOV, CU, CINCH, MSP, DIGIO and FV
- 5N to MSP (provision only) and Digital Board (provision only)
- 5VE to Basic Engine
- 5V_BE to Digital Board
- 5NSTBY to IOA, CINCH and DAC_ADC
- 5VSTBY to IOA, IOV, FV, MSP, DAC_ADC, Front Board
- 8VSTBY to MSP
- 12V to Digital Board
- 12VSTBY to CU, IOV, DAC_ADC, Front Board
- 12VE to Basic Engine and Digital Board (provision only)
- 33VSTBY to FV
- VGNSTBY to Front Board

Standby modes:
In Standby mode, the STBY control line is low, switching off the 3V3SW, 5V, 5N (provision), 5VE, 12V and 12VE supply and thus reducing the power consumption.

8.2.4. Tuner Frontend [1100 : TMQZ2]

It has a RF IN for antenna connection and RF OUT which provides a RF loop through for connection to the TV.
The Frontend (Tuner & IF-demodulator) is controlled by I^2C (SCL_5V- and SDA_5V-) lines coming from the Domino Host on the Digital board.
Complete video processing is done in this unit and the video output (CVBS) is taken out from the [VID_OUT] pin via a transistor as CVBS_TV-line to the Video I/O circuitry. The audio-IF component SIF1 is taken out from the [SIFOUT] pin for the demodulation by the Multi-sound processor (MSP).

Audio demodulator
The sound demodulation is done by the MSP3415 [7500], which is also fully controlled via I^2C bus by the Domino Host. The audio signals are available at pin 26 and pin 27 and fed as AFER- & AFEL- line to the audio I/O for further processing.

8.2.5. Audio routing

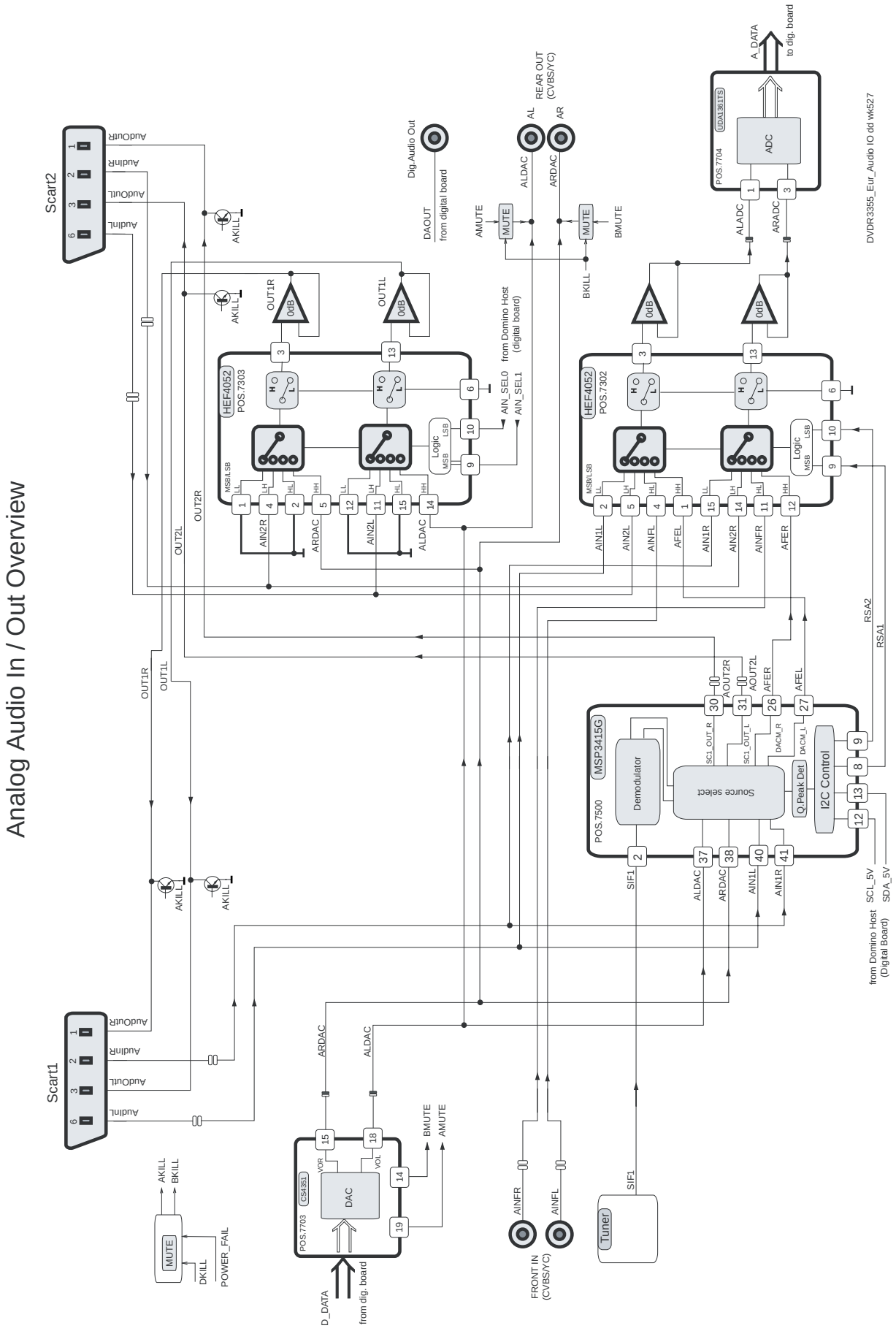


Figure 8-1 Analog Audio In / Out Overview

The sound processing is always done in stereo (that means separate left- and right- channel) and the complete switching is realized by using HEF4052 which is a dual four-to-one multiplexer and MSP3415G which is a multi-sound processor.

a) Scart 1 – Output path
The multiplexer [7303] selects either signals from the Scart 2 Input (AIN2L/AIN2R) or the Audio DAC (ALDAC/ARDAC) as the output source for Scart 1 (AOUT1L/AOUT1R).

b) Scart 2 – Output path
The MSP [7500] selects either signals from the Scart 1 Input (AIN1L/AIN1R), the Audio DAC (ALDAC/ARDAC) or the Tuner Frontend as the output source for Scart 2 (AOUT2L/AOUT2R).

c) Digital audio-out path
In addition, a digital output (DAOUT) coming from the Digital board is passed through a 6-fold inverter [7900] for performance reasons (noise reduction, jitter, …) and transformer (level correction, ground isolation,…) to the digital out cinch socket at the rear.

d) Record path
The record-selector [7302] selects either signals from the Scart 1 Input (AIN1L/AIN1R), Scart 2 Input (AIN2L/AIN2R), Front Cinch (AINFL/AINFR) or the MSP (AFEL/AFER) and routes to the audio ADC (ALADC/ARADC) for record purposes. The switch is controlled via RSA1 and RSA2 signals coming from the MSP.

8.2.6. Audio ADC/DAC

The conversion of analog audio signals from the record-selector [7302] outputs (ALADC/ARADC) is done via UDA1361TS [7704]. This IC can process input signals up to 2Vrms by using external resistors in series to the input pins. All required clock signals are generated on the digital board and only the audio data (A_DAT-line) are routed to Digital board for further processing.

The transformation of digital audio back into analog domain is done by CS4351 [7703]. All necessary clock signals are coming from the digital board and digital audio data (D_DATA0-line) are converted into analog signals (pin 15 and 18). The output signals from the audio DAC part (ALDAC/ARDAC) are directly routed to the rear cinch sockets. To avoid plops and any other audible noise on the output muting circuits are implemented for each channel.
Muting for the various other output lines are done via AKILL & BKILL-lines which is a combination of the D_KILL from the Digital board and POWER_FAIL from power supply and AMUTE & BMUTE (digital silence mute) from DAC-part.

8.2.7. Video-routing

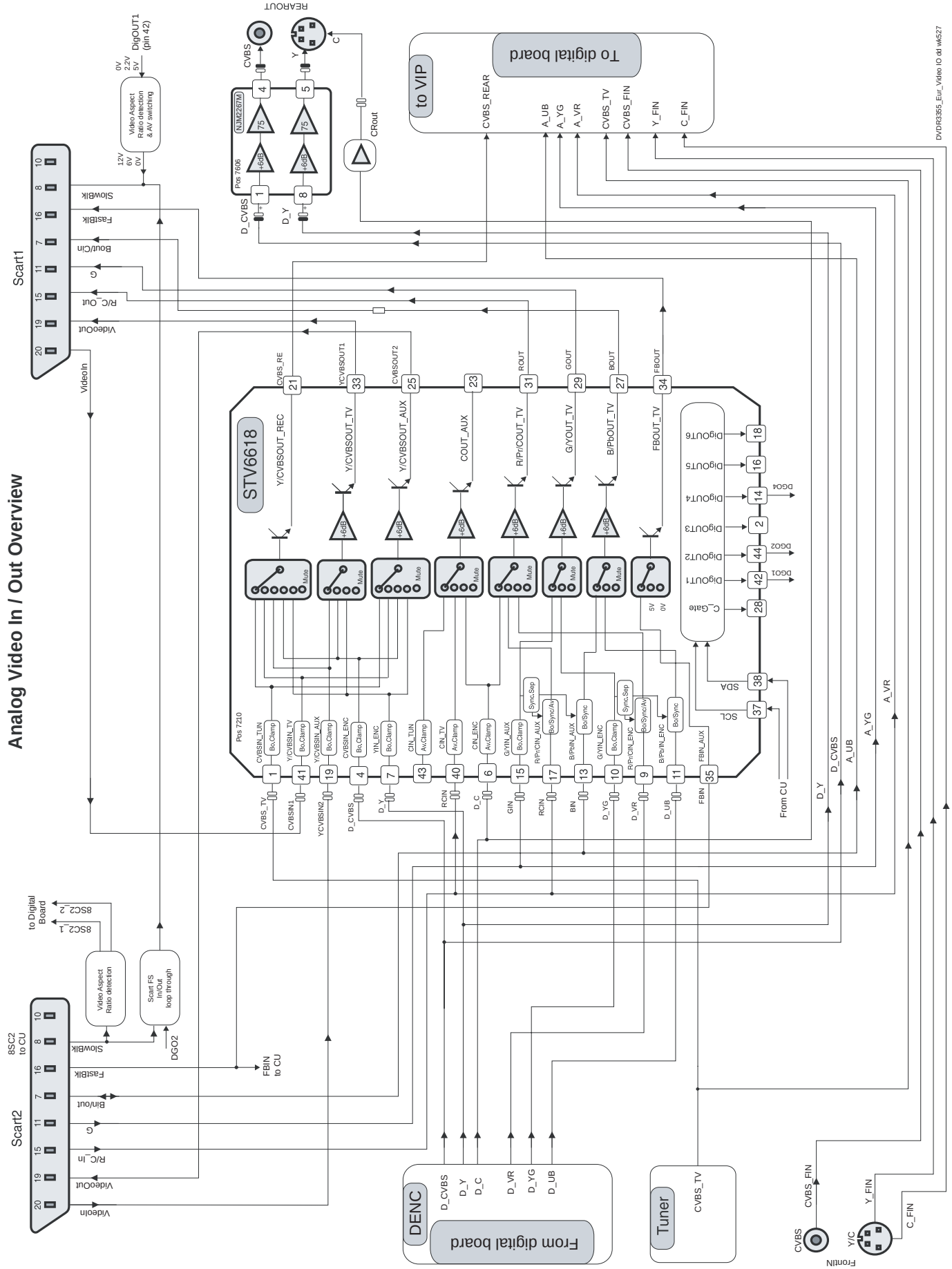


Figure 8-2 Analog Video In / Out Overview

A matrix switch STV6618 [7210] controlled by the Domino Host via I^2C-bus is used for Video I/O switching. All used outputs excluding pin 21 (Y/CVBS-REC) have a 6dB-amplification and a 75 ohms-driver-stage inside. This IC also includes several digital outputs, which are used for switching purposes on the Analog board.
This matrix switch routes the selected inputs to the correct output lines for TV viewing and further processing in the Digital board.

The record selector inside the switch selects between the inputs from Tuner Frontend (CVBS_TV), CVBS Scart1 (CVBSIN1), CVBS Scart2 (CVBSIN2) or D_CVBS from the DENC (on Digital board). The output signal CVBS_RE together with the other signals CVBS_FIN, Y_FIN & C_FIN from the Front and RCB from Scart2 are routed directly to the VIP (on Digital board) for further processing.

The signals D_C and D_Y are fed through [7606] (6dB amplification) and D_C via transistors [7213 & 7212] as driver to the S-Video output socket. Likewise the signal D_CVBS is fed through [7606] (6dB amplification) to the rear CVBS cinch socket.

8.3. Digital Board

The Digital Board is based on the highly integrated LSI 'Domino' BGA chip (Ball Grid Array), DMN-8602. This IC has an on-chip ATAPI controller and integrates an analog video encorder, and provides build-in support for non-simultaneous progressive and interlaced video output. A 1394 link layer function is also integrated so a simple external physical layer device is required. The DMN-8602 also has a set of integrated USB Physical Layer Interface.
The board encodes and multiplexes analogue video and digital uncompressed audio (I^2S) into an MPEG2 stream. This MPEG2 stream is formatted for recording by the DVD+RW engine. In the playback, the board will decode the MPEG2 video into analogue video. In addition, a DV stream can be received via IEEE 1394 (i-Link), and transformed to MPEG2 format.

8.3.1. Record Mode

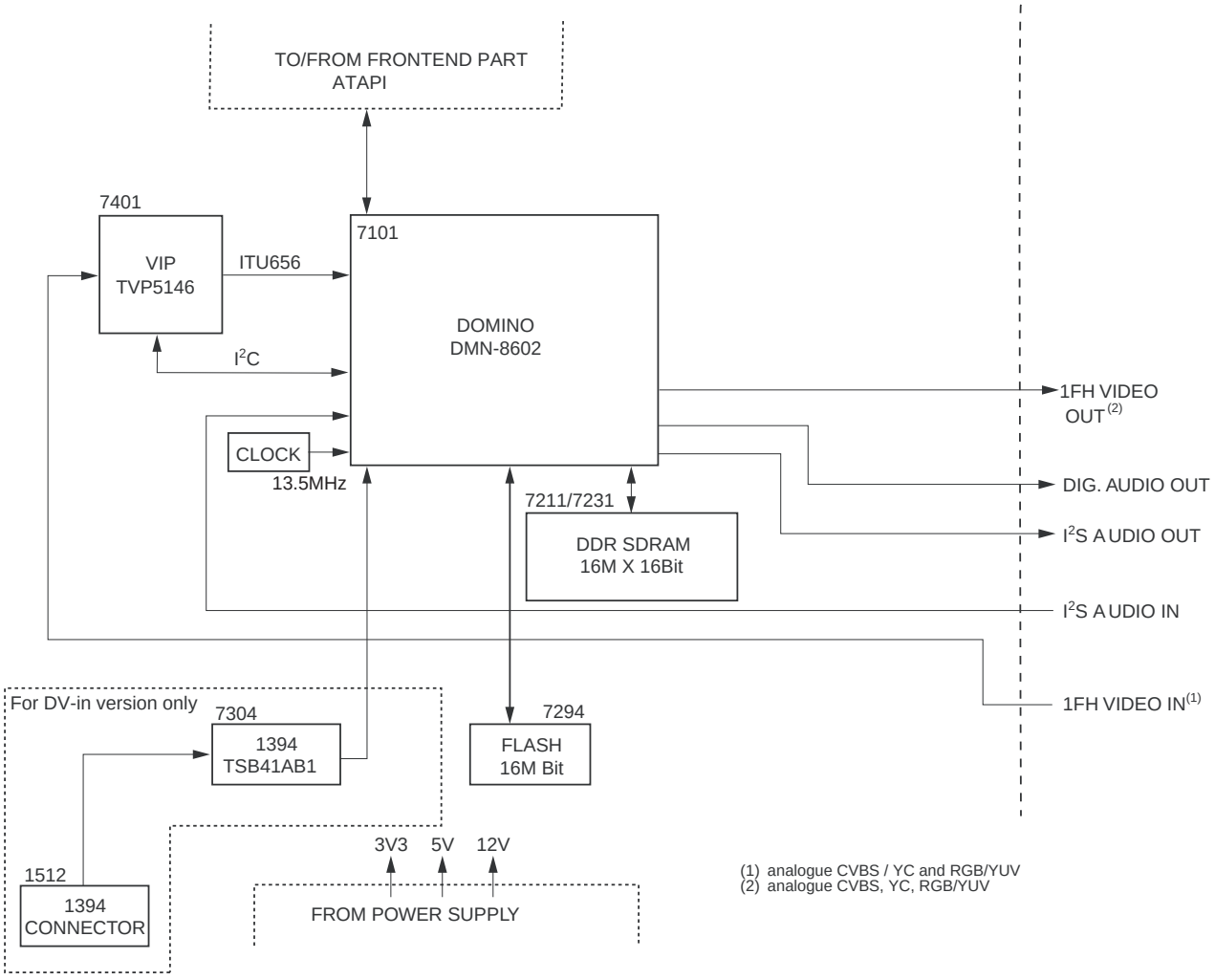


Figure 8-3 Domino block

Video Part
The analogue video input signals CVBS, YC and RGB are routed via the board to connector 1521 and sent to Video Input Processor, TVP5146P [7401].
The digital video input signals from the DV-in on the Front board are routed from connector 1521 via the IEEE 1394 PHY IC [7301] to the Domino chip [7101].

The Video Input Processor encodes the analogue video to digital video stream (CCIR656 format). The output stream, named VID_D (9:0), is then routed to the Domino chip. This IC encodes and decodes the digital video stream into / from MPEG2 format.

Audio Part
I^2S audio is sent from the Analog board to the Domino chip via connector 1536.
The Domino chip compresses the I^2S audio data into an MPEG1-L2 / AC3 audio stream.

Front-end I^2S
The Domino chip interfaces directly to the basic Engine via ATAPI connector 1571.
It buffers the data streams that are coming from (or going to) the Basic Engine.
In the Domino chip, the video MPEG2 stream and the audio AC3 stream are sent to the basic Engine for recording through ATAPI bus.

8.3.2. Playback mode
During playback, the data from the Basic Engine is going directly to the Domino chip via ATAPI interface. The Domino chip has the following outputs:
- Analogue video CVBS, YC and RGB outputs on connector 1521
- I^2S audio (PCM format) on connector 1536
- SPDIF audio (digital audio output) on connector 1536
- Progressive Scan output connector 1522 (Not for European version)

8.3.3. Basic Engine Interface
The Digital board is equipped with an IDE bus (ATAPI) for connecting to the Basic Engine.

8.3.4. Clock Distribution

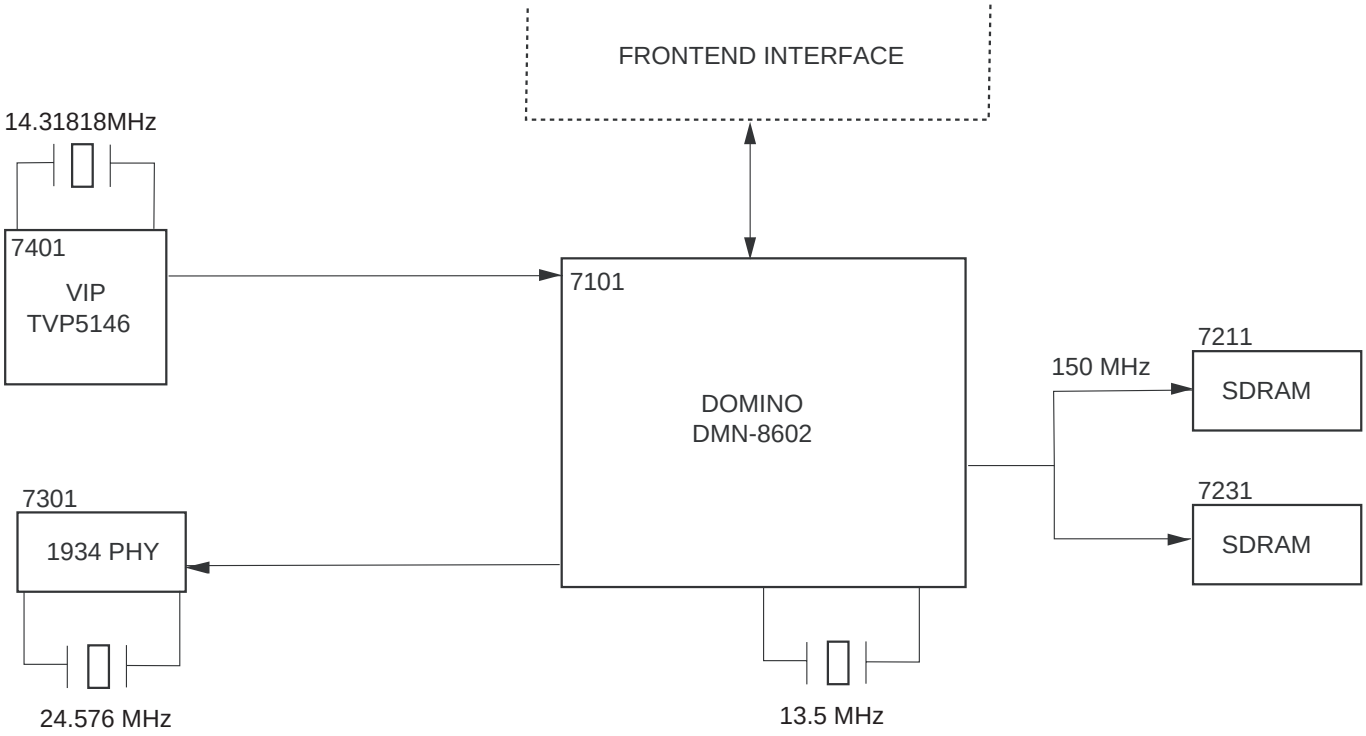


Figure 8-4 DIMINO_CLOCK

The Domino chip has a complex system, which is needed to support the processes running at different frequencies such as video decoding, audio decoding or peripheral I/O devices etc. To ensure a synchronous initialization of all the registers and state machines, all the PLLs are switched to their default frequency 27MHz.
Then when the booting control unit is correctly initialized and once it has captured all the booting parameters, it sets the PLLs to its functional frequencies. Thanks to a clock blocking mechanism, the frequency switching is glitch free.

System clocks:
- DMN-8602 (7101, pin E1 and F1): 13.5 MHz provided by the x'tal 1101
- DMN-8602 1394-LINK (7101, pin L1): 49.152MHz provided by 1394-PHY
- TVP5146 (7401, pin 74 and 75): 14.31818MHz provided by x'tal 1461
- SDRAM (7211 and 7231, pin 45 and 46): 150MHz provided by the DMN-8602
- TSB41AB1PHP IEEE 1394 PHY IC (7301, pin 42 and 43): 24.576MHz provided by x'tal 1351

8.3.5. Power Supply

The Digital board is not powered in standby mode. The control signal STBY on the analog board will enable the PSU and power the digital board.

- STBY = Low: the digital board is in powered down standby mode
- STBY = High: the power supply to the digital board is enabled.

The 3V3, +5V and +12V come from the PSU, while the following voltages are generated in the digital board:

- 1.8V core voltage is generated on the board by a 2A switching step down voltage regulator [7521]
- 2.5V supply for the SDRAM is generated by an ultra fast low dropout linear regulator [7515]
- 1.25V DDR termination supply is generated by regulator [7201]

8.3.6. Memory

- FLASH IC7294: this memory contains the boot parameters and application firmware

8.3.7. Reset

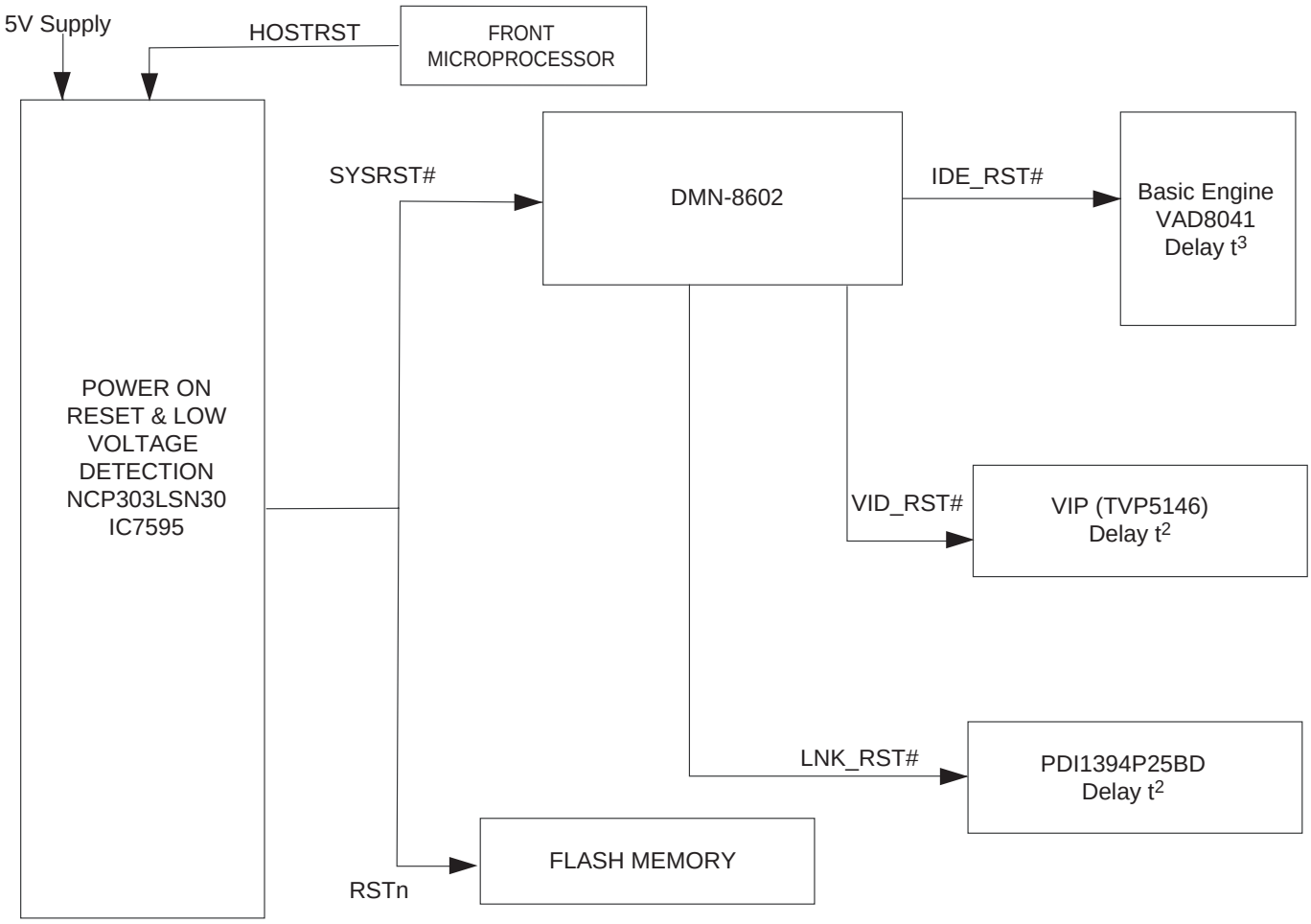


Figure 8-5 DOMINO_RESET

Reset concept Digital board

The rest circuitry [7595] takes cares that the different devices on the digital board are boot-up in the correct order. At power on the reset circuitry provides the following resets (delay $\tau 1$):

- SYS_RST# to the Domino chip [7101] and Flash Memory [7294]

The Domino chip then generates other reset signals (delay $\tau 2$) via its GPIOs:

- VID_RST# to reset the VIP [7401]
- LINK_RST# to reset the IEEE1394 DV PHY IC [7301]
- IDE_RST# to reset Basic Engine

8.3.8. I/O Connector

Audio IO Connector (item 136)

The Audio In/Out (AIO) connector is used to interchange digital audio signals between the Analog and Digital board

Video IO Connector (item 1521)

The Video In/Out (VIO) Connector is used to interchange analogue video signals between the Analog and Digital board

8.4 IC Description

8.4.1 Analog Board

IC7421 - TEA1507 - SMPS Control IC

BLOCK DIAGRAM

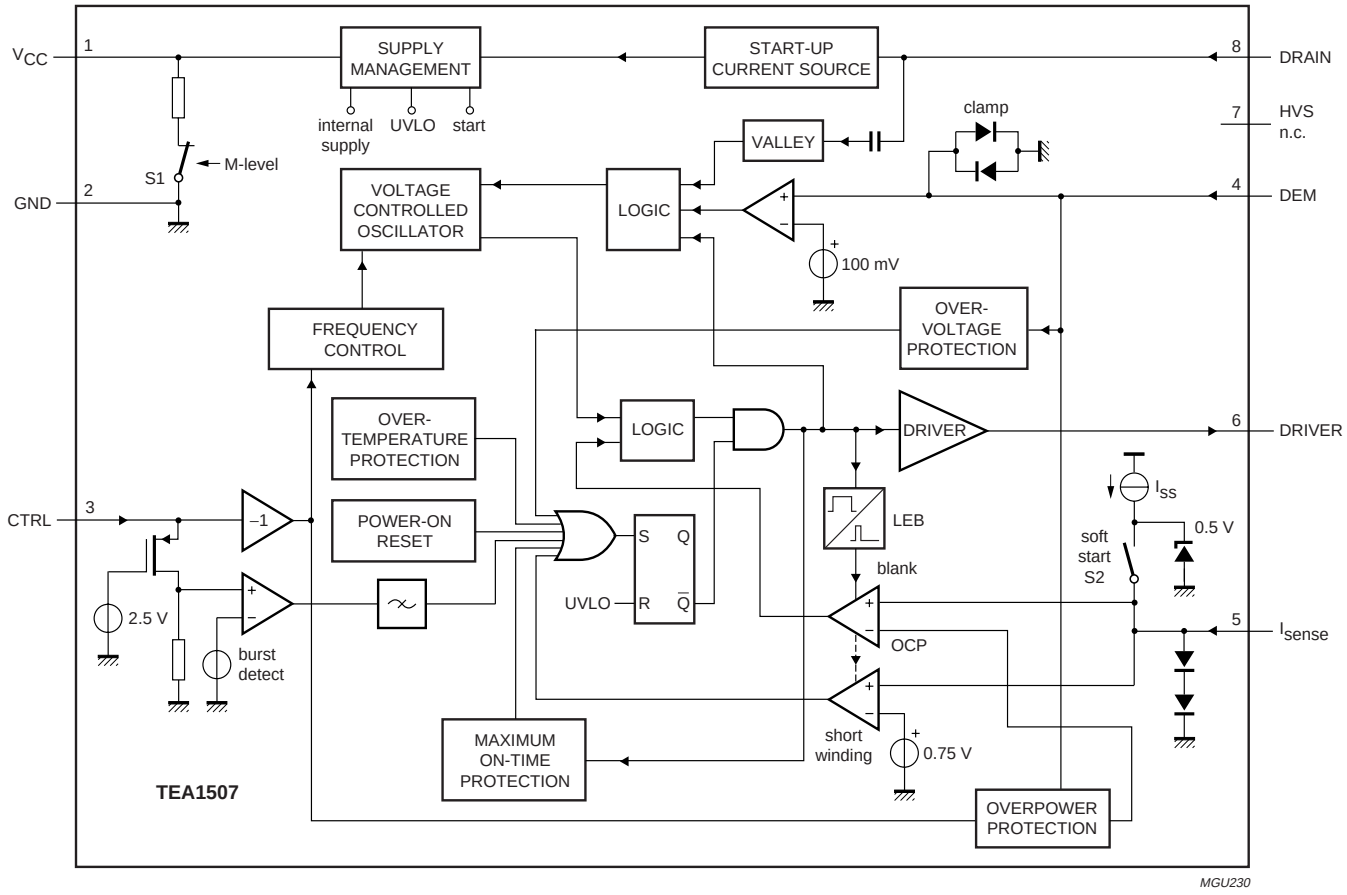


Figure 8-6

PIN DESCRIPTION AND CONFIGURATION

SYMBOL	PIN	DESCRIPTION
V_{CC}	1	supply voltage
GND	2	ground
CTRL	3	control input
DEM	4	input from auxiliary winding for demagnetization timing, OVP and OPP
I_{sense}	5	programmable current sense input
DRIVER	6	gate driver output
HVS	7	high voltage safety spacer, not connected
DRAIN	8	drain of external MOS switch, input for start-up current and valley sensing

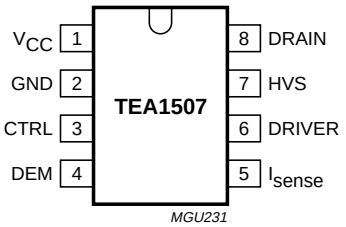


Fig.3 Pin configuration.

IC7500 - MSP34X5G - Multistand Sound Processor Family

BLOCK DIAGRAM

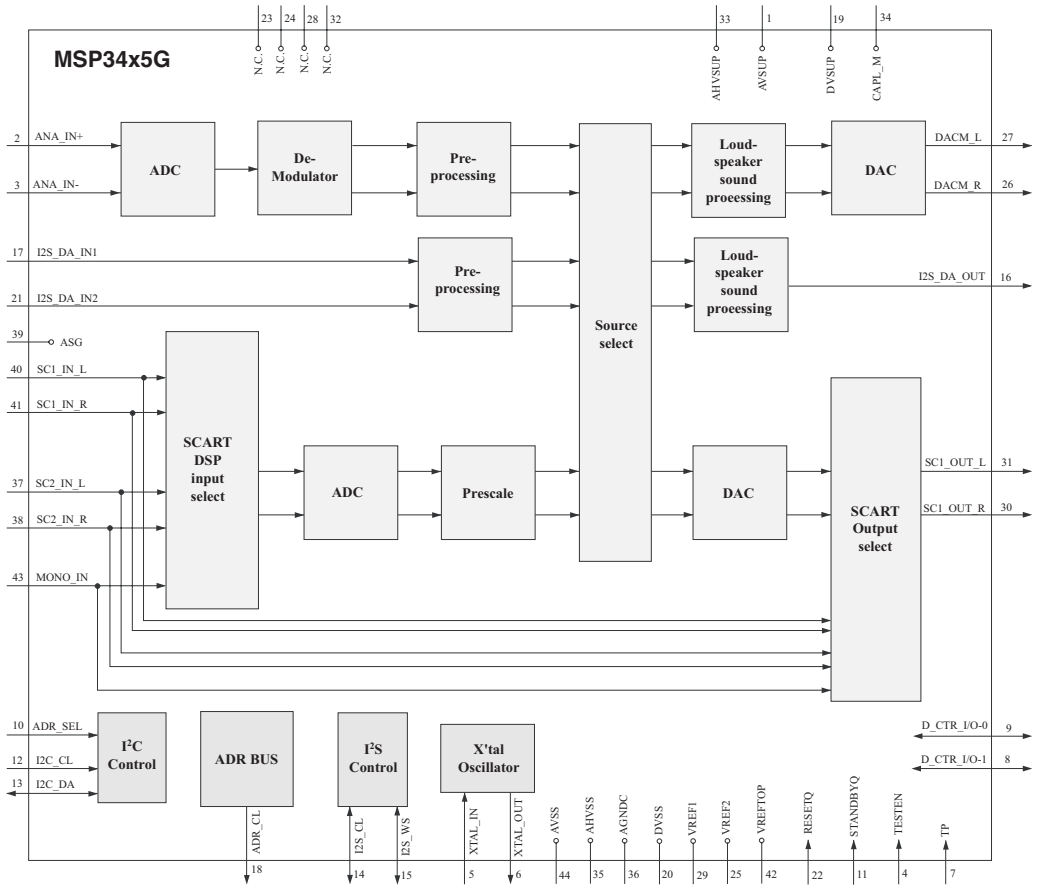
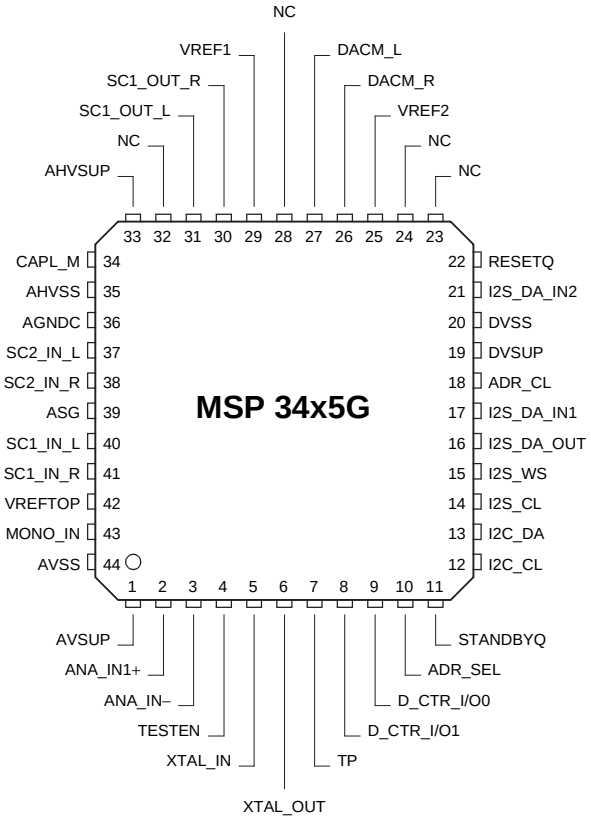


Figure 8-7

PIN CONFIGURATION



PMQFP44 package

Figure 8-8

IC7703 - CS4351 - 192KHz Stereo DAC with 2vrms line-out

BLOCK DIAGRAM

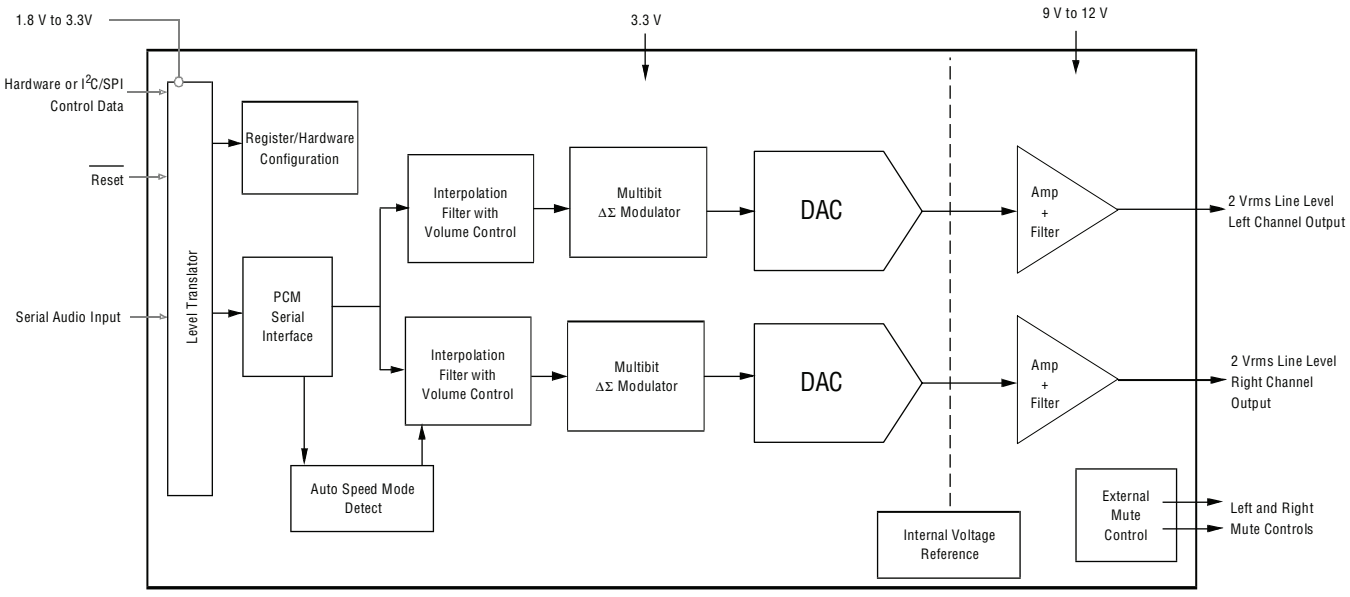
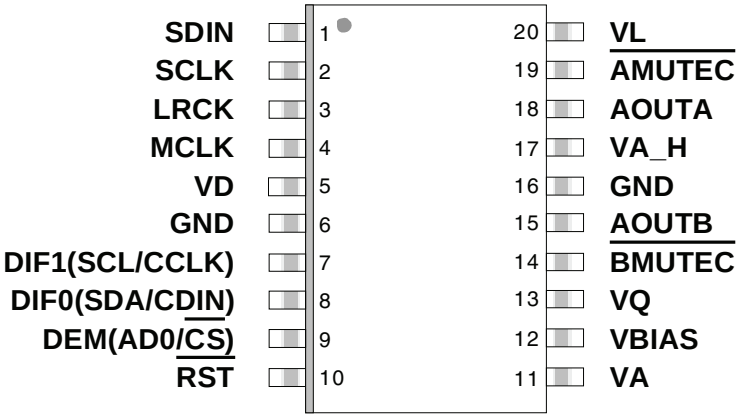


Figure 8-9

PIN DESCRIPTION AND CONFIGURATION



Pin Name	#	Pin Description
SDIN	1	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
SCLK	2	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
LRCK	3	**Left / Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	4	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VD	5	**Digital Power** (*Input*) **-** Positive power supply for the digital section.
GND	6 16	**Ground** (*Input*) - Ground reference.
$\overline{\text{RST}}$	10	**Reset** (*Input*) - Powers down device and resets all internal resisters to their default settings when enabled.
VA	11	**Low Voltage Analog Power** (*Input*) **-** Positive power supply for the analog section.
VBIAS	12	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal DAC.
VQ	13	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
VA_H	17	**High Voltage Analog Power** (*Input*) **-** Positive power supply for the analog section.
VL	20	**Serial Audio Interface Power** (*Input*) **-** Positive power for the serial audio interface
$\overline{\text{BMUTEC}}$ **$\overline{\text{AMUTEC}}$**	14 19	**Mute Control** (*Output*) - Control signal for optional mute circuit.
AOUTB **AOUTA**	15 18	**Analog Outputs** (*Output*) - The full scale analog line output level is specified in the *Analog Characteristics* table.
Control Port Definitions		
SCL/CCLK	7	**Serial Control Port Clock** (*Input*) - Serial clock for the control port interface.
SDA/CDIN	8	**Serial Control Data** (*Input/Output*) - Input/Output for I^2C data. Input for SPI data.
AD0/$\overline{\text{CS}}$	9	**Address Bit 0 / Chip Select** (*Input*) - Chip address bit in I^2C Mode. Control Port enable in SPI mode.
Stand-Alone Definitions		
DIF0 **DIF1**	8 7	**Digital Interface Format** (*Input*) - Defines the required relationship between the Left Right Clock, Serial Clock, and Serial Audio Data.
DEM	9	**De-emphasis** (*Input*) - Selects the standard 15µs/50µs digital de-emphasis filter response for 44.1 kHz sample rates

IC7704 - UDA1361TS - 96KHz Sampling 24-bit stereo audio ADC

BLOCK DIAGRAM

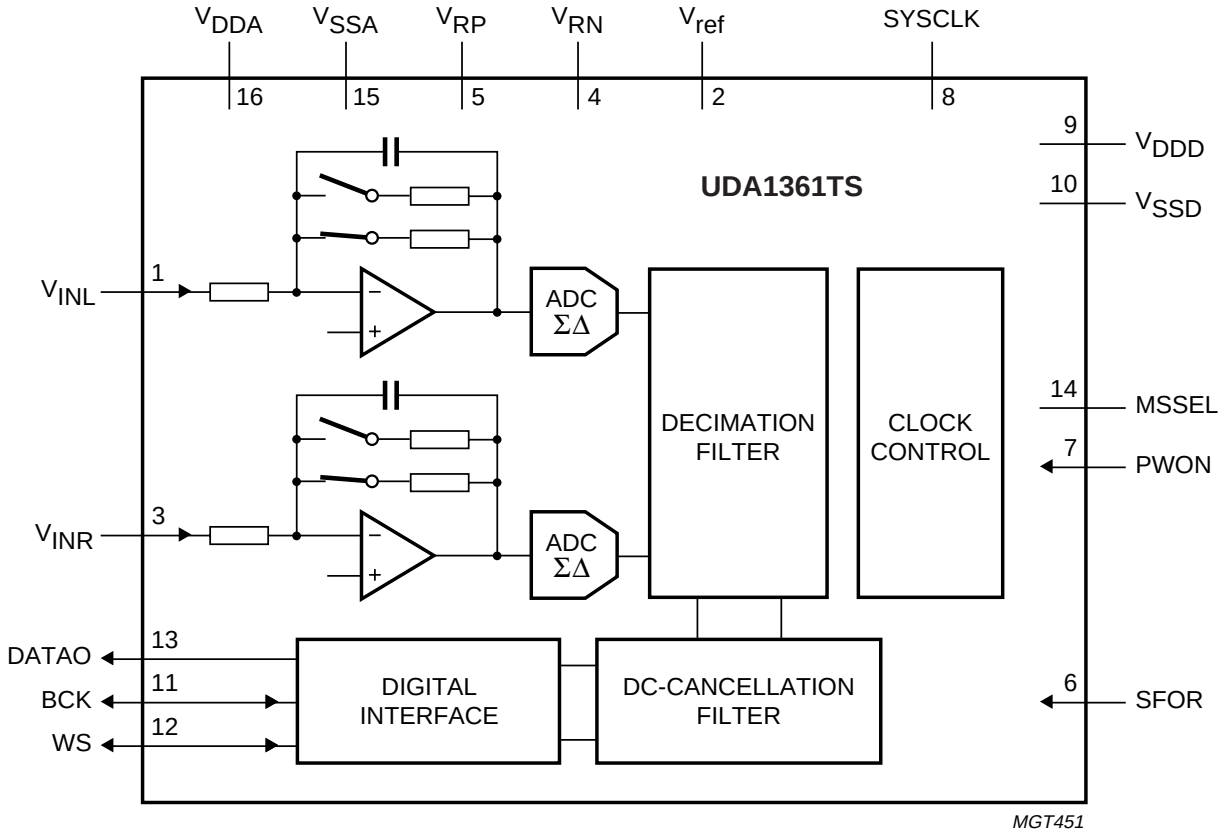
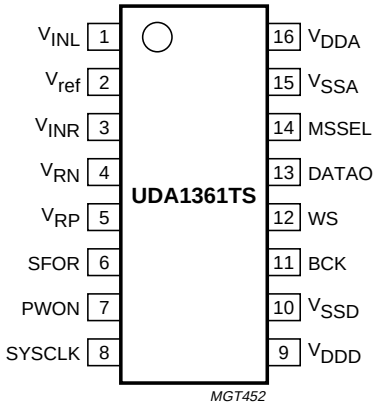


Figure 8-10

PIN DESCRIPTION AND CONFIGURATION

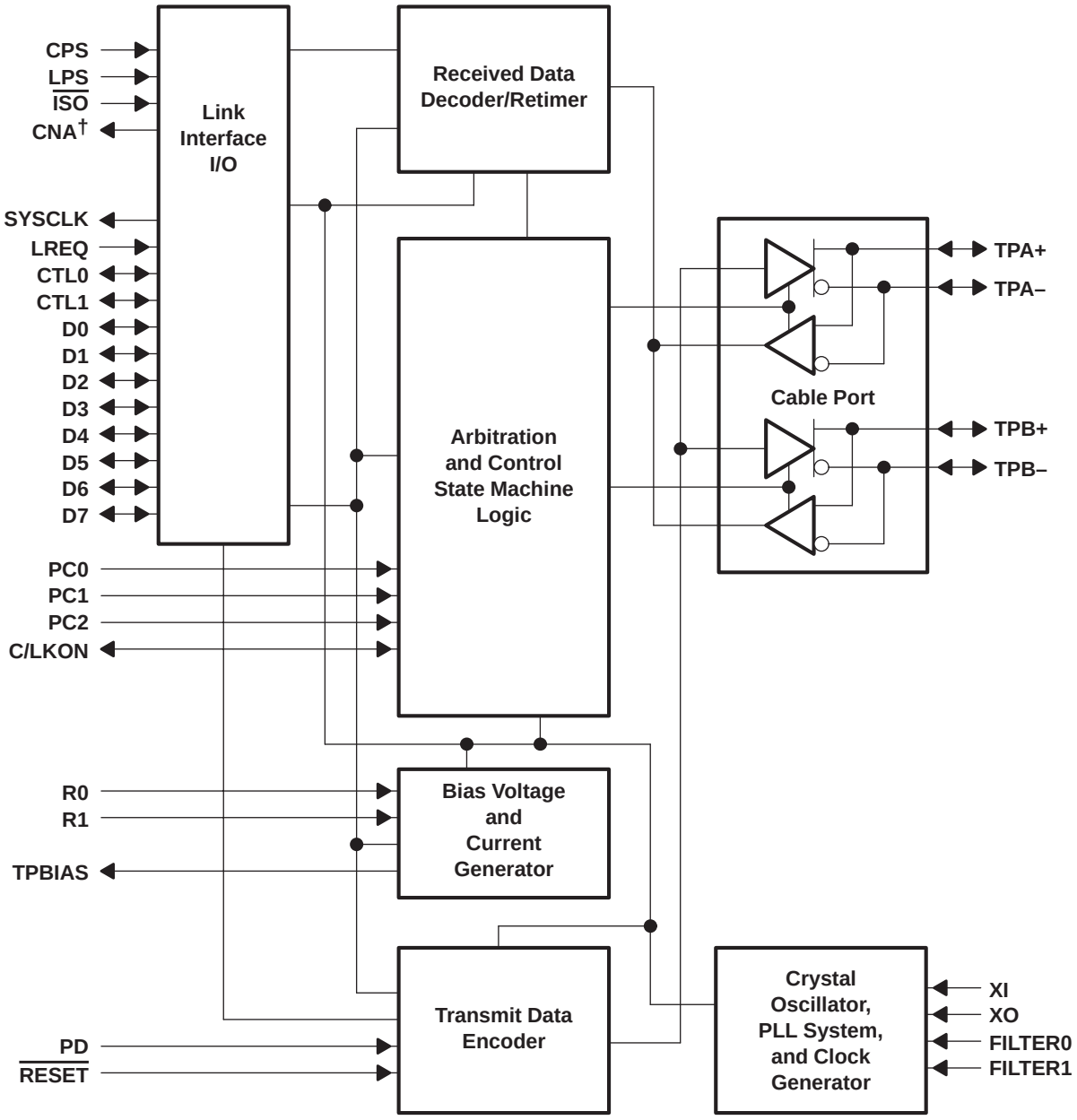
SYMBOL	PIN	DESCRIPTION
V_{INL}	1	left channel input
V_{ref}	2	reference voltage
V_{INR}	3	right channel input
V_{RN}	4	negative reference voltage
V_{RP}	5	positive reference voltage
SFOR	6	data format selection input
PWON	7	power control input
SYSCLK	8	system clock 256, 384, 512 or 768f_s
V_{DDD}	9	digital supply voltage
V_{SSD}	10	digital ground
BCK	11	bit clock input/output
WS	12	word select input/output
DATAO	13	data output
MSSEL	14	master/slave select
V_{SSA}	15	analog ground
V_{DDA}	16	analog supply voltage



8.4.2 Digital Board

IC7301 - TSB41AB1 - IEEE 1394a-2000 one port cable Transceiver/Arbiter

BLOCK DIAGRAM



† CNA output is only available in the 64-pin PAP package

Figure 8-11

PIN CONFIGURATION

PHP package terminal diagram

PHP PACKAGE
(TOP VIEW)

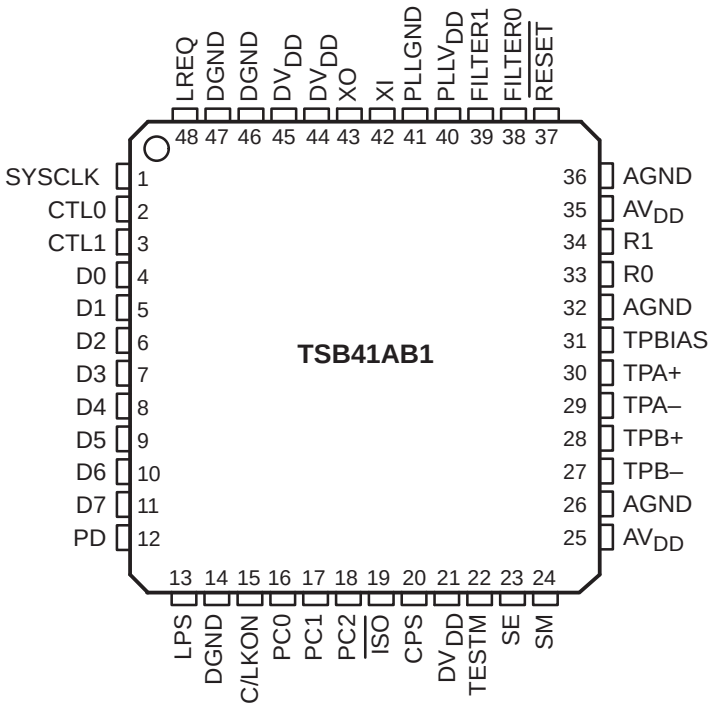


Figure 8-12

PIN DESCRIPTION

TERMINAL		TYPE	I/O	DESCRIPTION
NAME	PHP NO.			
AGND	26, 32, 36	Supply	–	Analog circuit ground terminals. These terminals should be tied together to the low-impedance circuit board ground plane.
AV_{DD}	25, 35	Supply	–	Analog circuit power terminals. A combination of high frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 μF and 0.001 μF. Lower frequency 10 μF filtering capacitors are also recommended. These supply terminals are separated from $PLLV_{DD}$ and DV_{DD} inside the device to provide noise isolation. They should be tied at a low-impedance point on the circuit board.
C/LKON	15	CMOS	I/O	Bus manager contender programming input and link-on output. On hardware reset, this terminal is used to set the default value of the contender status indicated during self-ID. Programming is done by tying the terminal through a 10-kΩ resistor to a high (contender) or low (not contender). The resistor allows the link-on output to override the input. However, it is recommended that this terminal should be programmed low, and that the contender status be set via the C register bit. If the TSB41AB1 is used with an LLC that has a dedicated terminal for monitoring LKON and also setting the contender status, then a 1-kΩ series resistor should be placed on the LKON line between the PHY and LLC to prevent bus contention. Following hardware reset, this terminal is the link-on output, which is used to notify the LLC to power up and become active. The link-on output is a square-wave signal with a period of approximately 163 ns (8 SYSCLK cycles) when active. The link-on output is otherwise driven low, except during hardware reset when it is high-impedance. The link-on output is activated if the LLC is inactive (LPS inactive or the LCtrl bit cleared) and when: a) the PHY receives a link-on PHY packet addressed to this node, or b) the PEI (port-event interrupt) register bit is 1, or c) any of the CTOI (configuration-time-out interrupt), CPSI (cable-power-status interrupt), or STOI (state-time-out interrupt) register bits are 1 and the RPIE (resuming-port interrupt enable) register bit is also 1. Once activated, the link-on output continues active until the LLC becomes active (both LPS active and the LCtrl bit set). The PHY also deasserts the link-on output when a bus reset occurs unless the link-on output would otherwise be active because one of the interrupt bits is set (that is, the link-on output is active due solely to the reception of a link-on PHY packet). NOTE: If an interrupt condition exists which would otherwise cause the link-on output to be activated if the LLC were inactive, the link-on output is activated when the LLC subsequently becomes inactive.
CNA	N/A	CMOS	O	Cable-not-active output. This terminal is asserted high when there is no incoming bias voltage.
CPS	20	CMOS	I	Cable power status input. This terminal is normally connected to cable power through a 400-kΩ resistor. This circuit drives an internal comparator that is used to detect the presence of cable power. This terminal should be tied directly to DV_{DD} supply if application does not require it to be used.
CTL0 CTL1	2 3	CMOS	I/O	Control I/Os. These bidirectional signals control communication between the TSB41AB1 and the LLC. Bus holders are built into these terminals.
D0 D1 D2 D3 D4 D5 D6 D7	4 5 6 7 8 9 10 11	CMOS	I/O	Data I/Os. These are bidirectional data signals between the TSB41AB1 and the LLC. Bus holders are built into these terminals.

TERMINAL		TYPE	I/O	DESCRIPTION
NAME	PHP NO.			
DGND	14, 46, 47	Supply	–	Digital circuit ground terminals. These terminals should be tied together to the low-impedance circuit board ground plane.
DV_{DD}	21, 44, 45	Supply	–	Digital circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 μF and 0.001 μF. Lower frequency 10 μF filtering capacitors are also recommended. These supply terminals are separated from $PLLV_{DD}$ and AV_{DD} inside the device to provide noise isolation. They should be tied at a low-impedance point on the circuit board.
FILTER0 FILTER1	38 39	CMOS	I/O	PLL filter terminals. These terminals are connected to an external capacitor to form a lag-lead filter required for stable operation of the internal frequency multiplier PLL running from the crystal oscillator. A 0.1 μF ±10% capacitor is the only external component required to complete this filter.
$\overline{ISO}$	19	CMOS	I	Link interface isolation control input. This terminal controls the operation of output differentiation logic on the CTL and D terminals. If an optional Annex J type isolation barrier is implemented between the TSB41AB1 and LLC, the $\overline{ISO}$ terminal should be tied low to enable the differentiation logic. If no isolation barrier is implemented (direct connection), or TI bus holder isolation is implemented, the $\overline{ISO}$ terminal should be tied high to disable the differentiation logic. For additional information refer to TI application note *Galvanic Isolation of the IEEE 1394-1995 Serial Bus*, SLLA011.
LPS	13	CMOS	I	Link power status input. This terminal monitors the active/power status of the link layer controller and controls the state of the PHY-LLC interface. This terminal should be connected through a 10-kΩ resistor either to the V_{DD} supplying the LLC, or to a pulsed output which is active when the LLC is powered (see Figure 9). A pulsed signal should be used when an isolation barrier exists between the LLC and PHY. (See Figure 10.) The LPS input is considered inactive if it is sampled low by the PHY for more than 2.6 μs (128 SYSCLK cycles), and is considered active otherwise (that is, asserted steady high or an oscillating signal with a low time less than 2.6 μs). The LPS input must be high for at least 21 ns to guarantee that a high is observed by the PHY. When the TSB41AB1 detects that LPS is inactive, it places the PHY-LLC interface into a low-power reset state. In the reset state, the CTL and D outputs are held in the logic zero state and the LREQ input is ignored; however, the SYSCLK output remains active. If the LPS input remains low for more than 26 μs (1280 SYSCLK cycles), the PHY-LLC interface is put into a low-power disabled state in which the SYSCLK output is also held inactive. The PHY-LLC interface is placed into the disabled state upon hardware reset. The LLC is considered active only if both the LPS input is active and the LCtrl register bit is set to 1, and is considered inactive if either the LPS input is inactive or the LCtrl register bit is cleared to 0.
LREQ	48	CMOS	I	LLC request input. The LLC uses this input to initiate a service request to the TSB41AB1. Bus holder is built into this terminal.
PC0 PC1 PC2	16 17 18	CMOS	I	Power class programming inputs. On hardware reset, these inputs set the default value of the power class indicated during self-ID. Programming is done by tying these terminals high or low. Refer to Table 9 for encoding.
PD	12	CMOS	I	Power-down input. A high on this terminal turns off all internal circuitry except the cable-active monitor circuits, which control the CNA output (64-terminal PAP package only). Asserting the PD input high also activates an internal pulldown on the $\overline{RESET}$ terminal to force a reset of the internal control logic. (PD is provided for legacy compatibility and is not recommended for power management in place of IEEE 1394a-2000 suspend/resume LPS and C/LKON features.)

TERMINAL		TYPE	I/O	DESCRIPTION
NAME	PHP NO.			
PLLGND	41	Supply	–	PLL circuit ground terminals. These terminals should be tied together to the low-impedance circuit board ground plane.
$PLLV_{DD}$	40	Supply	–	PLL circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 µF and 0.001 µF. Lower frequency 10 µF filtering capacitors are also recommended. This supply terminal is separated from DV_{DD} and AV_{DD} inside the device to provide noise isolation. It should be tied at a low-impedance point on the circuit board.
R0 R1	33 34	Bias	–	Current setting resistor terminals. These terminals are connected through an external resistor to set the internal operating currents and cable driver output currents. A resistance of 6.34 kΩ ±1.0% is required to meet the IEEE Std 1394-1995 output voltage limits.
$\overline{\text{RESET}}$	37	CMOS	I	Logic reset input. Asserting this terminal low resets the internal logic. An internal pullup resistor to V_{DD} is provided so only an external delay capacitor is required for proper power-up operation (see *power-up reset* in the Application Information section). The $\overline{\text{RESET}}$ terminal also incorporates an internal pulldown which is activated when the PD input is asserted high. This input is otherwise a standard logic input, and may also be driven by an open-drain type driver.
SE	23	CMOS	I	Test control input. This input is used in manufacturing test of the TSB41AB1. For normal use this terminal may be tied to GND through a 1-kΩ pulldown resistor or it may be tied to GND directly.
SM	24	CMOS	I	Test control input. This input is used in manufacturing test of the TSB41AB1. For normal use this terminal should be tied to GND.
SYSCLK	1	CMOS	O	System clock output. Provides a 49.152-MHz clock signal, synchronized with data transfers, to the LLC.
TESTM	22	CMOS	I	Test control input. This input is used in manufacturing test of the TSB41AB1. For normal use this terminal should be tied to V_{DD}.
TPA+	30	Cable	I/O	Twisted-pair cable A differential signal terminals. Board traces from the pair of positive and negative differential signal terminals should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPA–	29	Cable	I/O	
TPB+	28	Cable	I/O	Twisted-pair cable B differential signal terminals. Board traces from the pair of positive and negative differential signal terminals should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPB–	27	Cable	I/O	
TPBIAS	31	Cable	I/O	Twisted-pair bias output. This provides the 1.86 V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers, and for signaling to the remote nodes that there is an active cable connection.
XI XO	42 43	Crystal	–	Crystal oscillator inputs. These terminals connect to a 24.576-MHz parallel resonant fundamental mode crystal. The optimum values for the external shunt capacitors are dependent on the specifications of the crystal used (see *crystal selection* in the Application Information section). When an external clock source is used, XI should be the input and XO should be left open, and the clock must be supplied before the device is powered on.

IC7401 - TVP5146PFP - 4x10bit DigitalVideo Decoder with microvision

BLOCK DIAGRAM

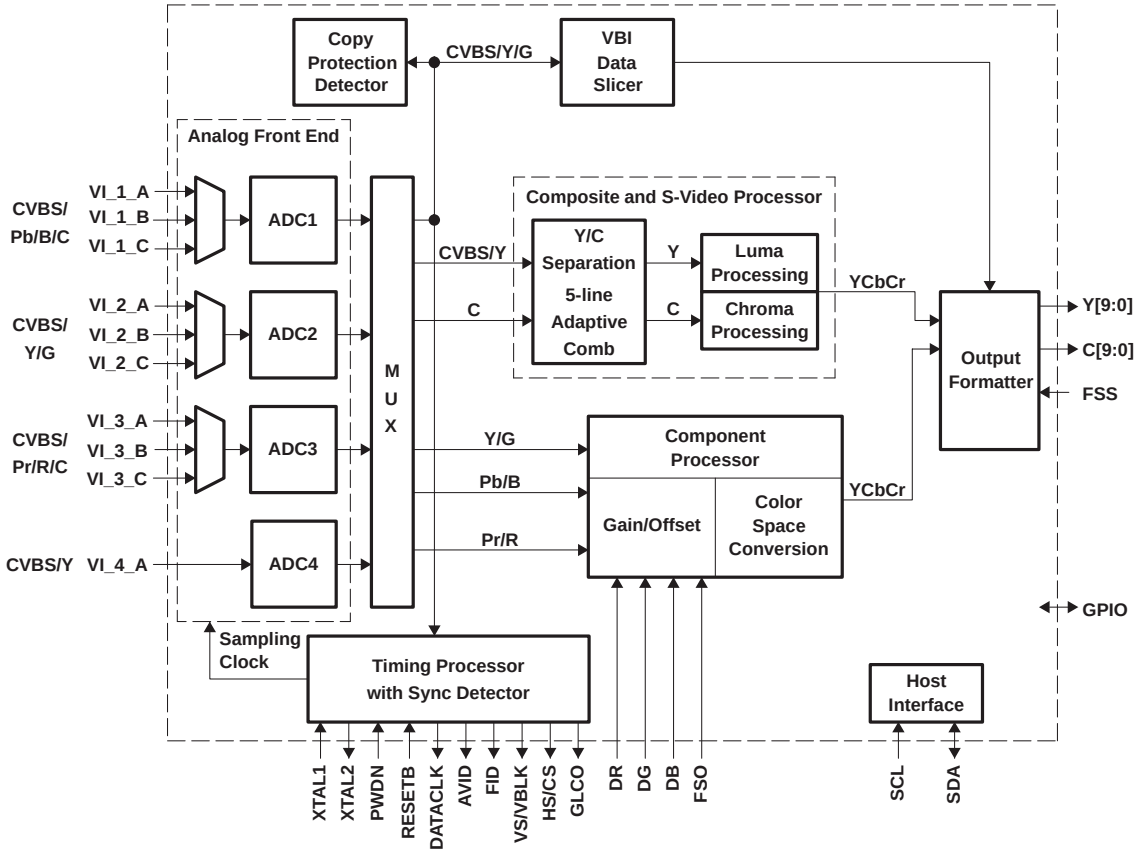


Figure 8-13

PIN CONFIGURATION

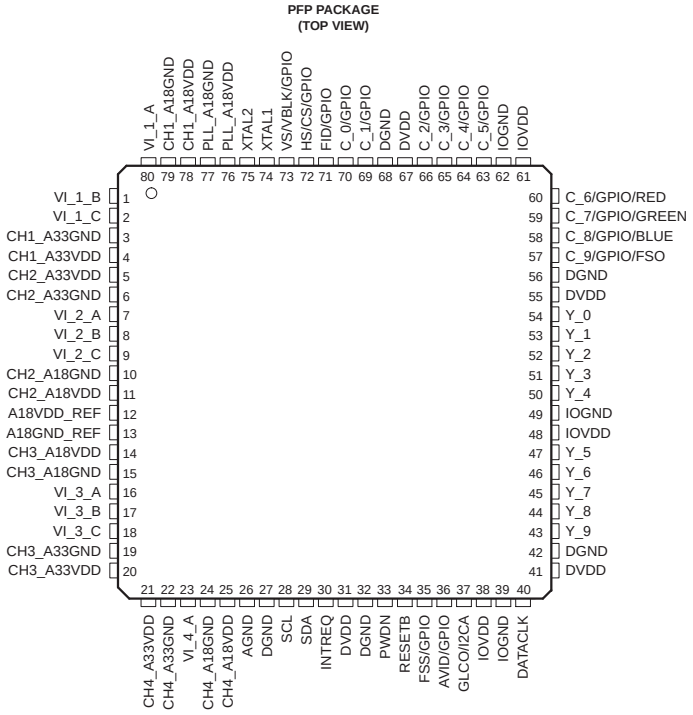


Figure 8-14

PIN DESCRIPTION

TERMINAL NAME	TERMINAL NUMBER	I/O	DESCRIPTION
Analog Video			
VI_1_A VI_1_B VI_1_C VI_2_A VI_2_B VI_2_C VI_3_A VI_3_B VI_3_C VI_4_A	80 1 2 7 8 9 16 17 18 23	I	VI_1_x: Analog video input for CVBS/Pb/B/C VI_2_x: Analog video input for CVBS/Y/G VI_3_x: Analog video input for CVBS/Pr/R/C VI_4_A: Analog video input for CVBS/Y Up to 10 composite, 4 S-video, and 2 composite or 3 component video inputs (or a combination thereof) can be supported. The inputs must be ac-coupled. The recommended coupling capacitor is 0.1 µF. The possible input configurations are listed in the input select register at I^2C subaddress 00h (see Section 2.11.1).
Clock Signals			
DATACLK	40	O	Line-locked data output clock.
XTAL1	74	I	External clock reference input. It may be connected to an external oscillator with a 1.8-V compatible clock signal or a 14.31818-MHz crystal oscillator.
XTAL2	75	O	External clock reference output. Not connected if XTAL1 is driven by an external single-ended oscillator.
Digital Video			
C[9:0]/ GPIO[9:0]	57, 58, 59, 60, 63, 64, 65, 66, 69, 70	O	Digital video output of CbCr, C[9] is MSB and C[0] is LSB. Unused outputs can be left unconnected. Also, these terminals can be programmable general-purpose I/O. For the 8-bit mode, the two LSBs are ignored.
D_BLUE	58	I	Digital BLUE input from overlay device
D_GREEN	59	I	Digital GREEN input from overlay device
D_RED	60	I	Digital RED input from overlay device
FSO	57	I	Fast-switch overlay between digital RGB and any video
Y[9:0]	43, 44, 45, 46, 47, 50, 51, 52, 53, 54	O	Digital video output of Y/YCbCr, Y[9] is MSB and Y[0] is LSB. For the 8-bit mode, the two LSBs are ignored. Unused outputs can be left unconnected.
Miscellaneous Signals			
FSS/GPIO	35	I/O	Fast-switch (blanking) input. Switching signal between the synchronous component video (YPbPr/RGB) and the composite video input. Programmable general-purpose I/O
GLCO/I2CA	37	I/O	Genlock control output (GLCO). Two Genlock data formats are available: TI format and real time control (RTC) format. During reset, this terminal is an input used to program the I^2C address LSB.
INTREQ	30	O	Interrupt request
PWDN	33	I	Power down input: 1 = Power down 0 = Normal mode
RESETB	34	I	Reset input, active low

TERMINAL NAME	TERMINAL NUMBER	I/O	DESCRIPTION
Host Interface			
SCL	28	I	I^2C clock input
SDA	29	I/O	I^2C data bus
Power Supplies			
AGND	26	I	Analog ground. Connect to analog ground.
A18GND_REF	13	I	Analog 1.8-V return
A18VDD_REF	12	I	Analog power for reference 1.8 V
CH1_A18GND CH2_A18GND CH3_A18GND CH4_A18GND	79 10 15 24	I	Analog 1.8-V return
CH1_A18VDD CH2_A18VDD CH3_A18VDD CH4_A18VDD	78 11 14 25	I	Analog power. Connect to 1.8 V.
CH1_A33GND CH2_A33GND CH3_A33GND CH4_A33GND	3 6 19 22	I	Analog 3.3-V return
CH1_A33VDD CH2_A33VDD CH3_A33VDD CH4_A33VDD	4 5 20 21	I	Analog power. Connect to 3.3 V.
DGND	27, 32, 42, 56, 68	I	Digital return
DVDD	31, 41, 55, 67	I	Digital power. Connect to 1.8 V.
IOGND	39, 49, 62	I	Digital power return
IOVDD	38, 48, 61	I	Digital power. Connect to 3.3 V or less for reduced noise.
PLL_A18GND	77	I	Analog power return
PLL_A18VDD	76	I	Analog power. Connect to 1.8 V.
Sync Signals			
HS/CS/GPIO	72	I/O	Horizontal sync output or digital composite sync output Programmable general-purpose I/O
VS/VBLK/GPIO	73	I/O	Vertical sync output (for modes with dedicated VSYNC) or VBLK output Programmable general-purpose I/O
FID/GPIO	71	I/O	Odd/even field indicator output. This terminal needs a pulldown resistor. Programmable general-purpose I/O
AVID/GPIO	36	I/O	Active video indicator output Programmable general-purpose I/O

IC7501 - TPS2041 - Power Distribution Switches

BLOCK DIAGRAM

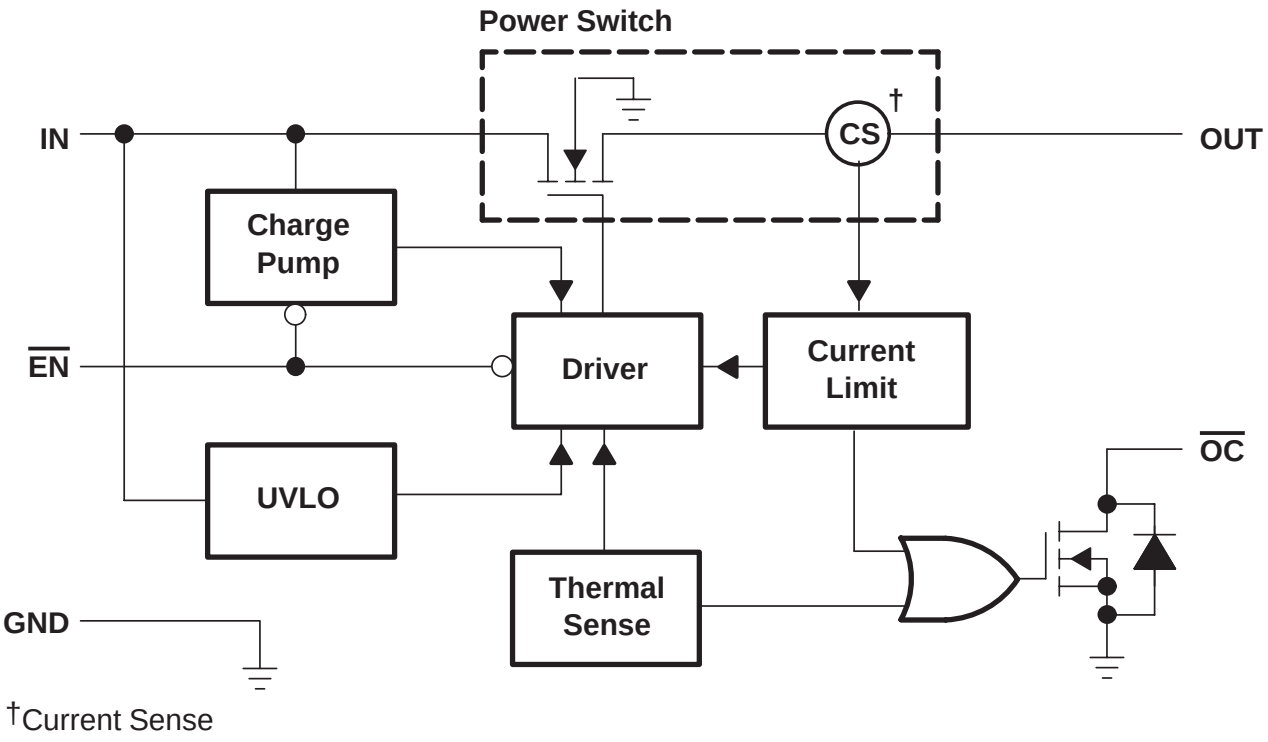


Figure 8-15

PIN CONFIGURATION

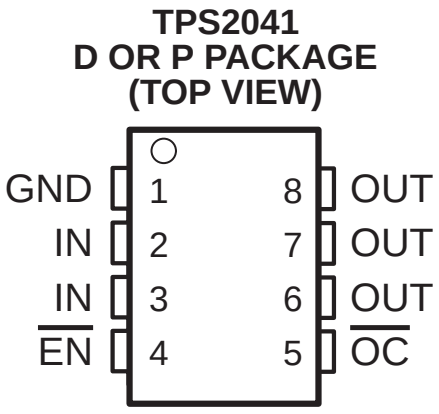


Figure 8-16

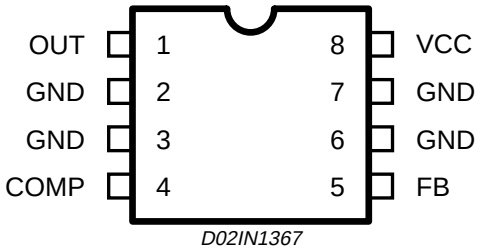
PIN DESCRIPTION

TERMINAL			I/O	DESCRIPTION
NAME	NO. D OR P			
	TPS2041	TPS2051		
$\overline{EN}$	4	–	I	Enable input. Logic low turns on power switch.
EN	–	4	I	Enable input. Logic high turns on power switch.
GND	1	1	I	Ground
IN	2, 3	2, 3	I	Input voltage
$\overline{OC}$	5	5	O	Over current. Logic output active low
OUT	6, 7, 8	6, 7, 8	O	Power-switch output

IC7521 - L5972D - 2A Switch Step Down Switching Regulator

PIN DESCRIPTION AND CONFIGURATION

PIN CONNECTION



PIN DESCRIPTION

N°	Pin	Function
1	OUT	Regulator Output.
2,3,6,7	GND	Ground.
4	COMP	E/A output for frequency compensation.
5	FB	Feedback input. Connecting directly to this pin results in an output voltage of 1.23V. An external resistive divider is required for higher output voltages.
8	VCC	Unregulated DC input voltage.

IC7595 - NCP303 - Voltage Detector Series with Programmable Delay

BLOCK DIAGRAM

NCP303LSNxxT1
Open Drain Output Configuration

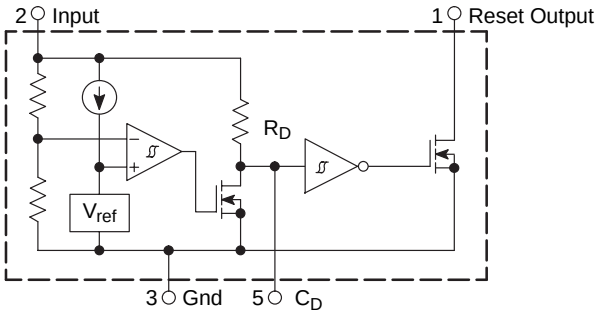
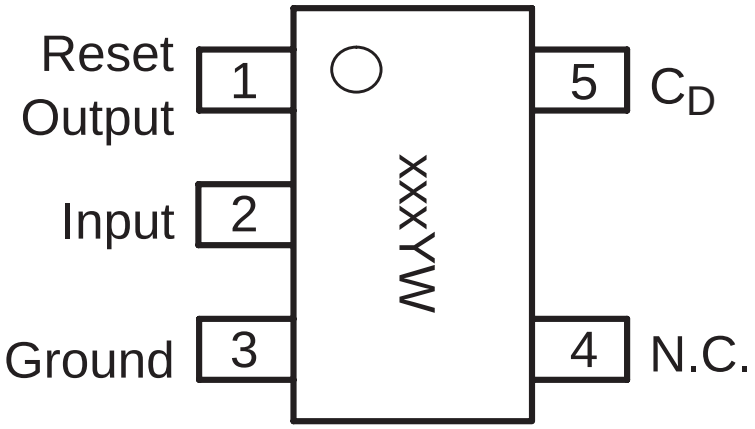


Figure 8-17

PIN DESCRIPTION AND CONFIGURATION

PIN CONNECTIONS AND MARKING DIAGRAM



xxx = 302 or 303
Y = Year
W = Work Week

(Top View)

Figure 8-18

Exploded View of the Set

3139 249 2798 2005-03-02

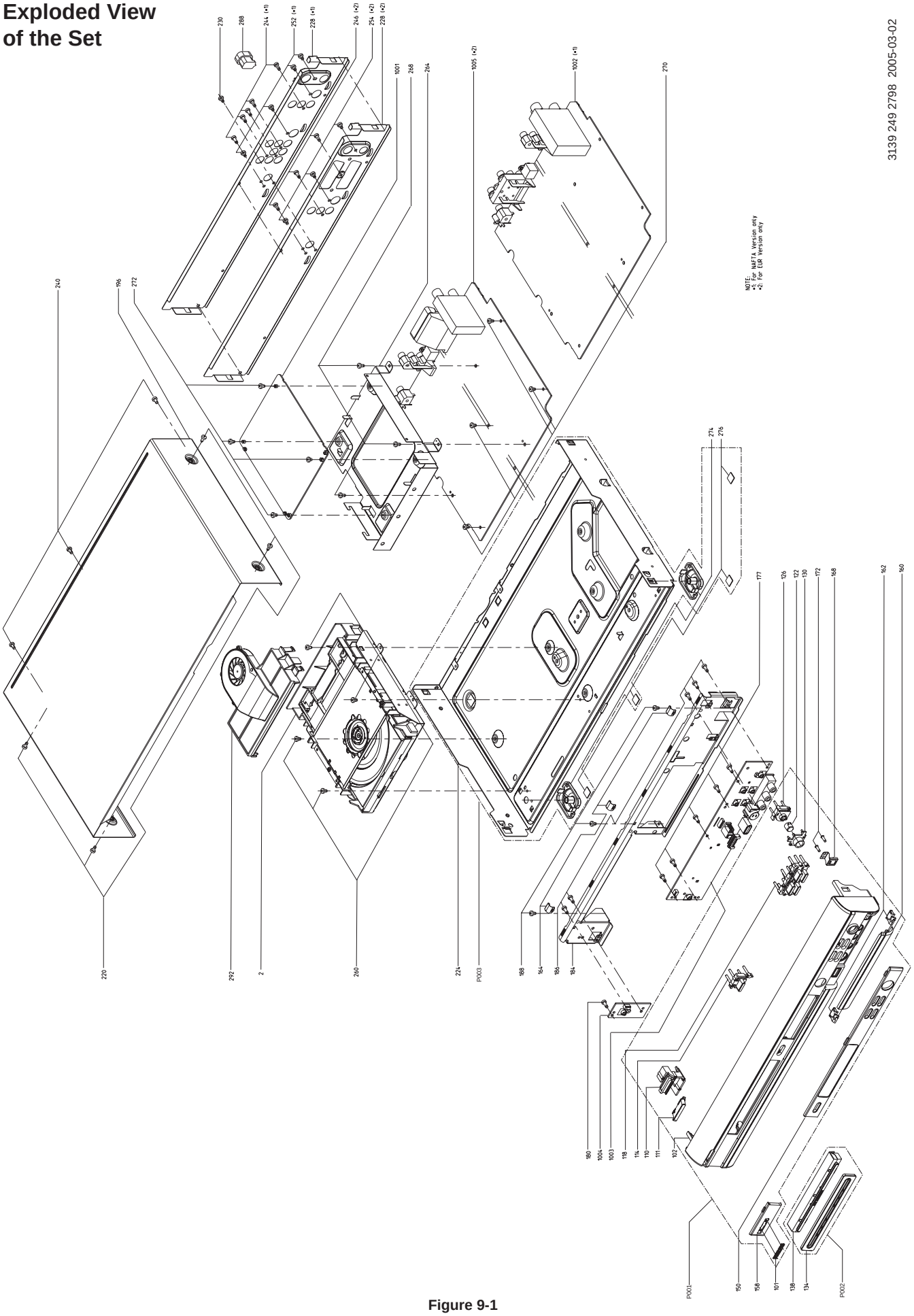


Figure 9-1

Spare Parts List

0002	3139 247 11131		MODULE DRIVE D4.3	
0164	3103 601 20231		SPRING GROUND	
0168	3103 601 20212		SPRING I-LINK	
0196	3139 241 22761		COVER TOP DVDR3305	
0228	3139 241 22791		PLATE REAR EU DVDR3305	
0288	4822 532 60948		BUSH	
0333	2422 549 00607		REMOTE CONTR DVDR3365/EU B	
0333	2422 549 00611		REMOTE CONTR DVDR3355/DVDR3305	
0336	4822 321 11499	⚠	MAINSCORD	/02, /19, /51 only
0336	2422 070 98236	⚠	MAINSCORD UK 5A 1M8 VH BK B	/05 only
0342	2422 076 00532		CBLE SCART 1M5 SCART 21P BK B	
0345	4822 320 50377		CONNECT. CABLE PAL	
0901	3143 027 62231		FRONT ASSY DVDR3365	/02, /19, /51 only
0901	3143 027 62261		FRONT ASSY DVDR3365	/05 only
0901	3143 027 62311		FRONT ASSY DVDR3355	/02, /19, /51 only
0901	3143 027 62331		FRONT ASSY DVDR3355	/05 only
0901	3143 027 62681		FRONT ASSY DVDR3305	/02, /19, /51 only
0901	3143 027 62701		FRONT ASSY DVDR3355	/05 only
0910	3143 027 61951		COVER TRAY ASSY DVDR3365	
0910	3143 027 62351		COVER TRAY ASSY DVDR3355	
0910	3143 027 62411		COVER TRAY ASSY DVDR3305	
0920	3143 027 62251		FRAME ASSY	
1001	3139 248 86731		DIGITAL BOARD DVDR3365	/05 only
1001	3139 248 84651		DIGITAL BOARD DVDR3365	/02, /19 only
1001	3139 248 86721		DIGITAL BOARD DVDR3365	/51 only
1001	3139 248 86691		DIGITAL BOARD DVDR3305	/05 only
1001	3139 248 86061		DIGITAL BOARD DVDR3305	/02, /19 only
1001	3139 248 86681		DIGITAL BOARD DVDR3305	/51 only
1001	3139 248 86711		DIGITAL BOARD DVDR3355	/05 only
1001	3139 248 85941		DIGITAL BOARD DVDR3355	/02, /19 only
1001	3139 248 86701		DIGITAL BOARD DVDR3355	/51 only
1003	3139 248 84591		FRONT BOARD DVDR3365	
1003	3139 248 86561		FRONT BOARD DVDR3305	
1003	3139 248 86291		FRONT BOARD DVDR3355	
1004	3139 248 84751		STB BOARD DVDR 3355/DVDR3365	
1004	3139 248 86551		STB BOARD DVDR 3305	
1005	3139 248 84631		ANALOG BOARD DVDR3355/DVDR3365	
1005	3139 248 86571		ANALOG BOARD DVDR3305	
8002	3139 110 35631		FFC FOIL 22P/180/22P BD 1MMP	
8003	3139 241 01081		FFC FOIL 20P/140/20P BD 1MMP	
8004	3139 241 00241		FFC FOIL 30P/140/30P BD 1MMP	
8007	3139 241 00591		CBLE HR 04P/220/04P LOADER SUP	
8008	3139 241 01011		FFC FOIL 14P/180/14P BD 1MMP	
8010	3139 241 00921		CBLE IDE 40P/280/40P IDE UL	
8011	2422 076 00676		CBLE IEEE1394 DVDR3355/DVDR3365	

10. REVISION LIST

Version 1.0
* Original Release

Version 1.1
* Add missing Exploded View drawing