Service
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Service Information

General

The DVIO 1.8 DV input board replaces the DVIO 1.5 using a different chip set.
Attached are the DVIO 1.8 board schematics, layout and parts list for updating the service manuals of DVDR890 with 12NCs 3122 785 12200 (Euro) and 3122 785 12550 (APAC).

Remarks

The DVIO 1.8 board has been used in the production of the DVDR890 from week 0237 onwards.
The factory change code printed on the type plate of the sets was increased from VN06 to VN07.

EU models:
- DVD890/001/021/051

APAC models:
-DVDR890/131/691/971

Contents

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PHILIPS

Personal Notes:

1. Waveforms

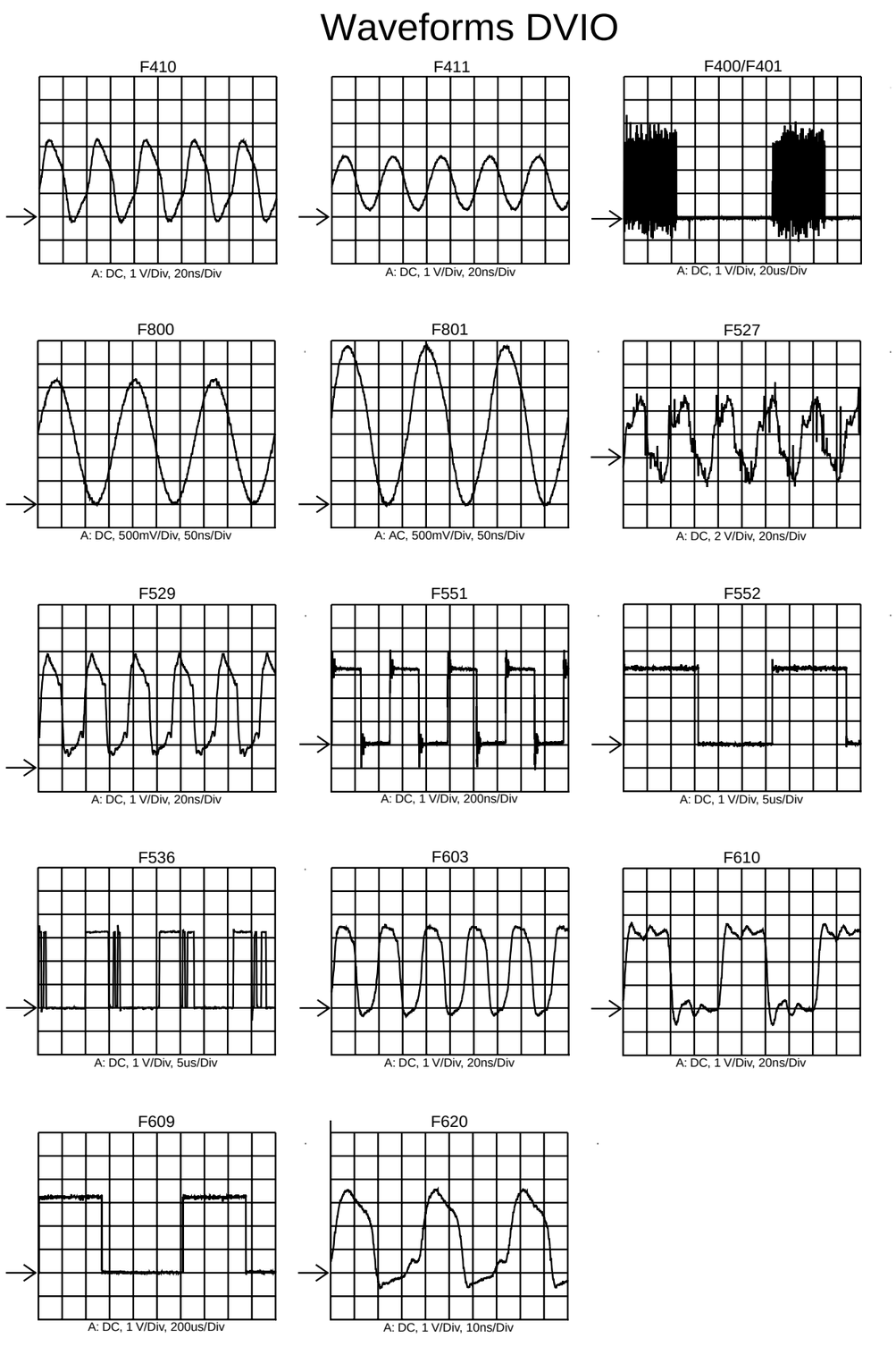
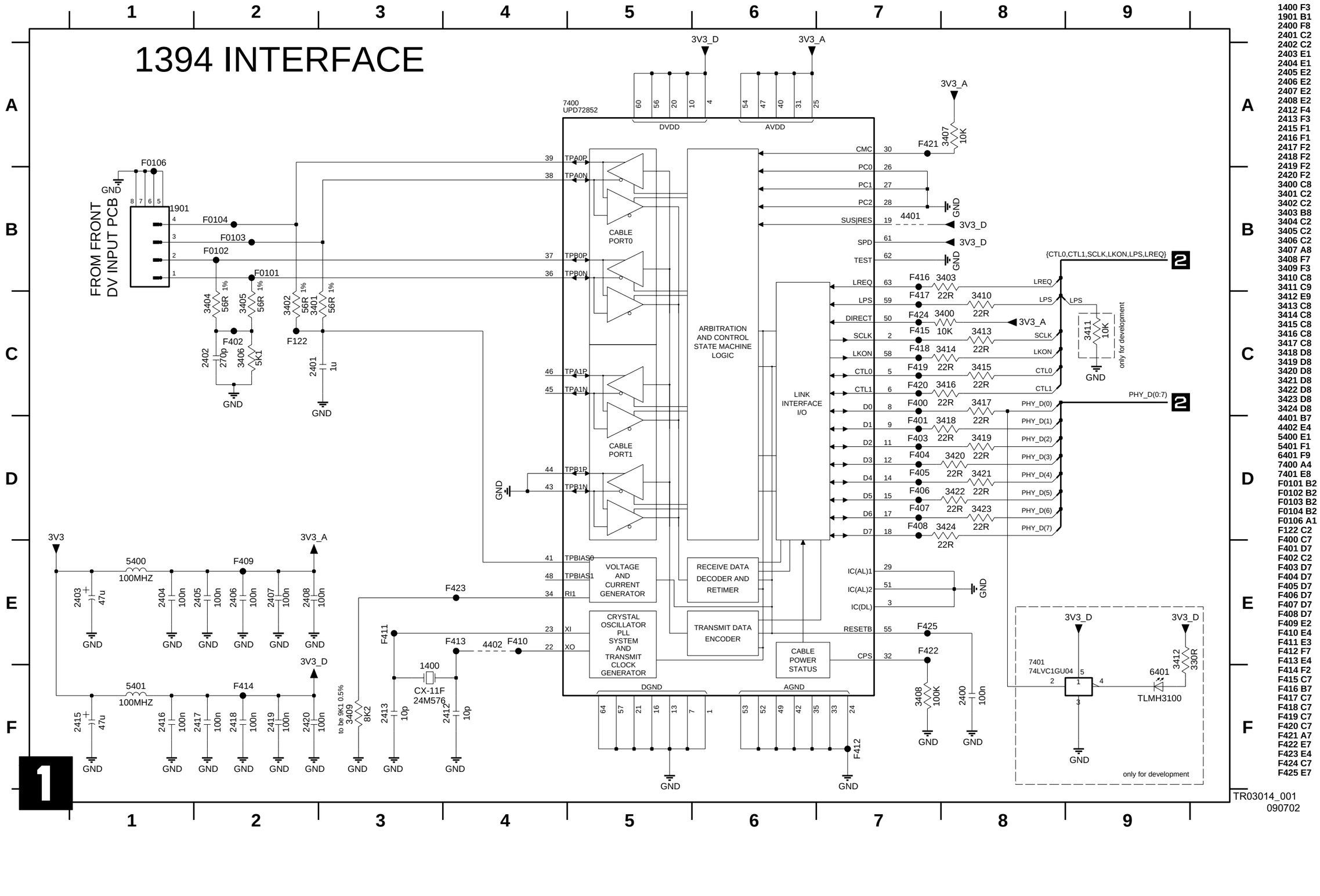


Figure 1-1

2. Circuit Diagrams and PWB Layouts

DVIO 1.8 Board: 1394 Interface



1400 F3
1901 B1
2400 F8
2401 C2
2402 C2
2403 E1
2404 E1
2405 E2
2406 E2
2407 E2
2408 E2
2412 F4
2413 F3
2415 F1
2416 F1
2417 F2
2418 F2
2419 F2
2420 F2
3400 C8
3401 C2
3402 C2
3403 B8
3404 C2
3405 C2
3406 C2
3407 A8
3408 F7
3409 F3
3410 C8
3411 C9
3412 E9
3413 C8
3414 C8
3415 C8
3416 C8
3417 C8
3418 D8
3419 D8
3420 D8
3421 D8
3422 D8
3423 D8
3424 D8
4401 B7
4402 E4
5400 E1
5401 F1
6401 F9
7400 A4
7401 E8
F0101 B2
F0102 B2
F0103 B2
F0104 B2
F0106 A1
F122 C2
F400 C7
F401 D7
F402 C2
F403 D7
F404 D7
F405 D7
F406 D7
F407 D7
F408 D7
F409 E2
F410 E4
F411 E3
F412 F7
F413 E4
F414 F2
F415 C7
F416 B7
F417 C7
F418 C7
F419 C7
F420 C7
F421 A7
F422 E7
F423 E4
F424 C7
F425 E7

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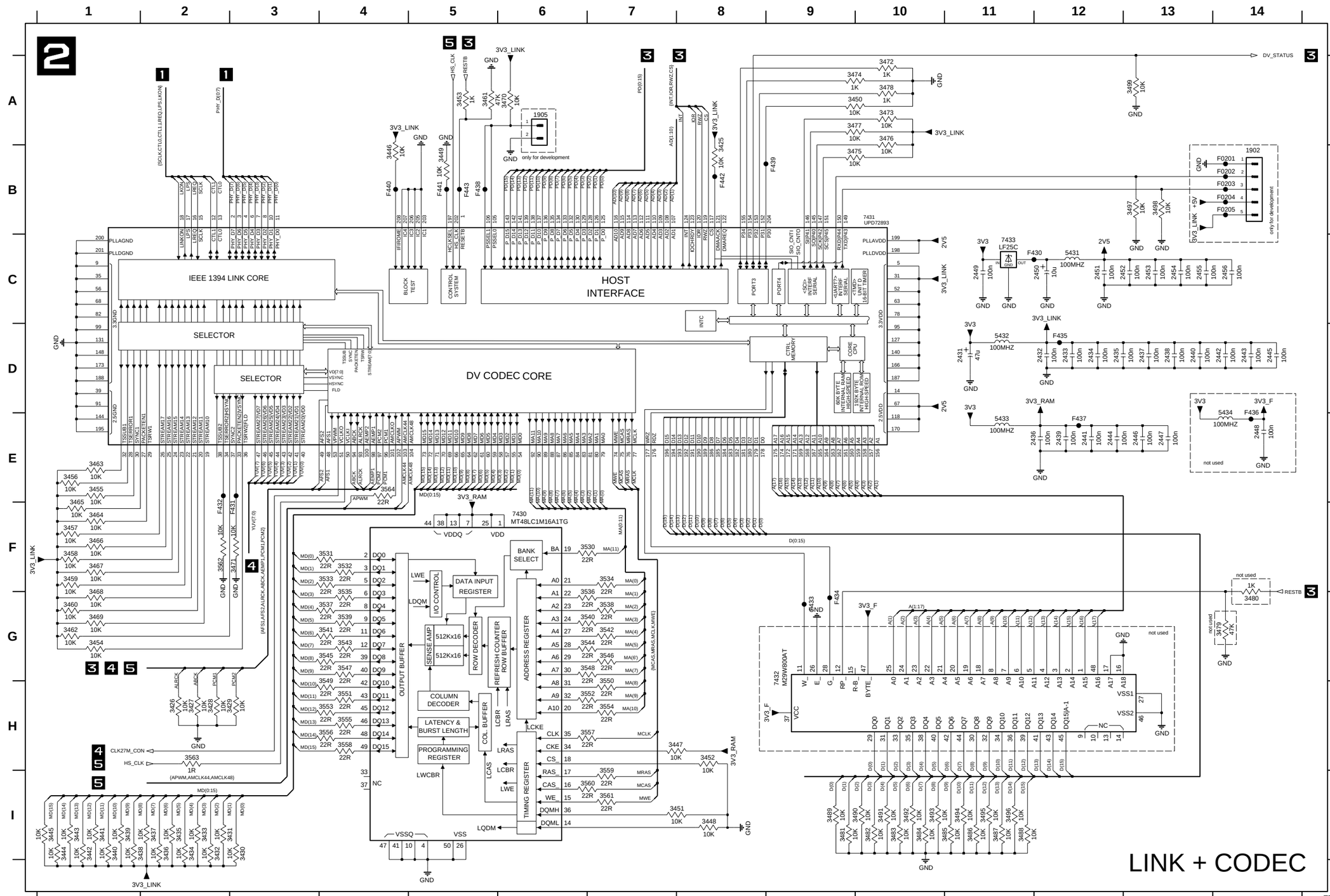
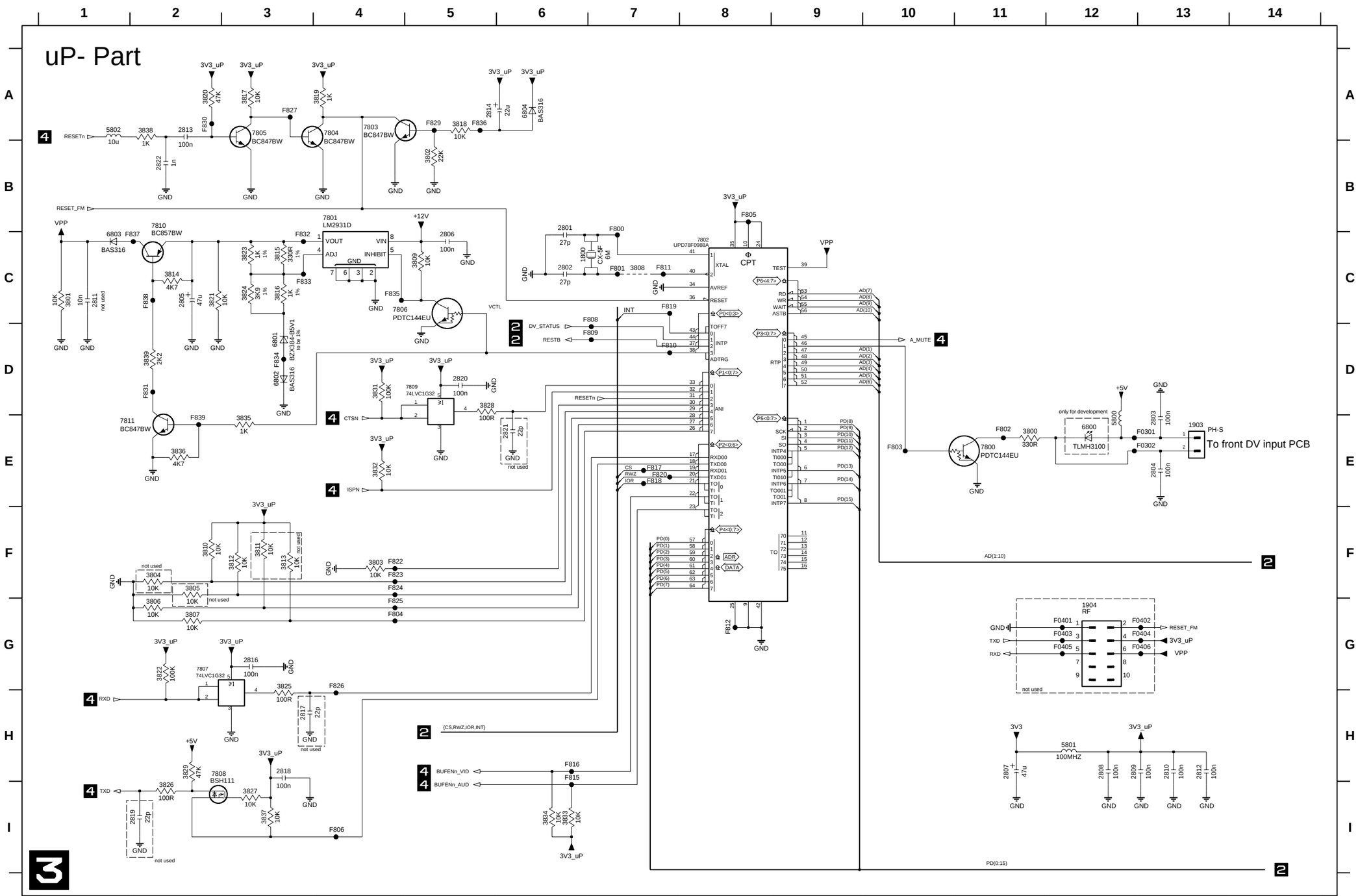
DVIO 1.8 Board: Link + Codec



DVIO 1.8 Board: uP Part



1800 C6
1903 E13
1904 G12
2801 B6
2802 C6
2803 E13
2804 E13
2805 C2
2806 C5
2807 H11
2808 H12
2809 H12
2810 H13
2811 C1
2812 H13
2813 A2
2814 A5
2816 G3
2817 H3
2818 H3
2819 I2
2820 D5
2821 E6
2822 B2
3800 E11
3801 C1
3802 B5
3803 F4
3804 F2
3805 F2
3806 G2
3807 G2
3808 C7
3809 C5
3810 F2
3811 F3
3812 F3
3813 F3
3814 C2
3815 C3
3816 C3
3817 A3
3818 A5
3819 A4
3820 A2
3821 C2
3822 G2
3823 C3
3824 C3
3825 G3
3826 I2
3827 I3
3828 D5
3829 H2
3831 D4
3832 E4
3833 I6
3834 I6
3835 E3
3836 E2
3837 I3
3838 A2
3839 D2
5800 E12
5801 H12
5802 A1
6800 E12
6801 D3
6802 D3
6803 C1
6804 A6
7800 E11
7801 B4
7802 C8
7803 A4
7804 A4
7805 A3
7806 C4
7807 G2
7808 H2
7809 D5
7810 B2
7811 E1
F0301 E13
F0302 E13
F0401 G12
F0402 G13
F0403 G12
F0404 G13
F0405 G12
F0406 G13
F800 B7
F801 C7
F802 E11
F803 E10
F804 G4
F805 B8
F806 I4
F808 C7
F809 D7
F810 D7
F811 C7
F812 G8
F815 H6
F816 H6
F817 E7
F818 E7
F819 C7
F820 E7
F822 F4
F823 F4
F824 F4
F825 G4
F826 G4
F827 A3
F829 A5
F830 A2
F831 D2
F832 C3
F833 C3
F834 D3
F835 C4
F836 A5
F837 C2
F838 C2
F839 E2

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DVIO 1.8 Board: Interface + DAC

Interface + DAC

Clock delay

Buffer

To digital PCB

To analog PCB - Sound Processing

DAC

Shielding connection on mounting holes

Hole 4.9mm

Hole 3.6 mm

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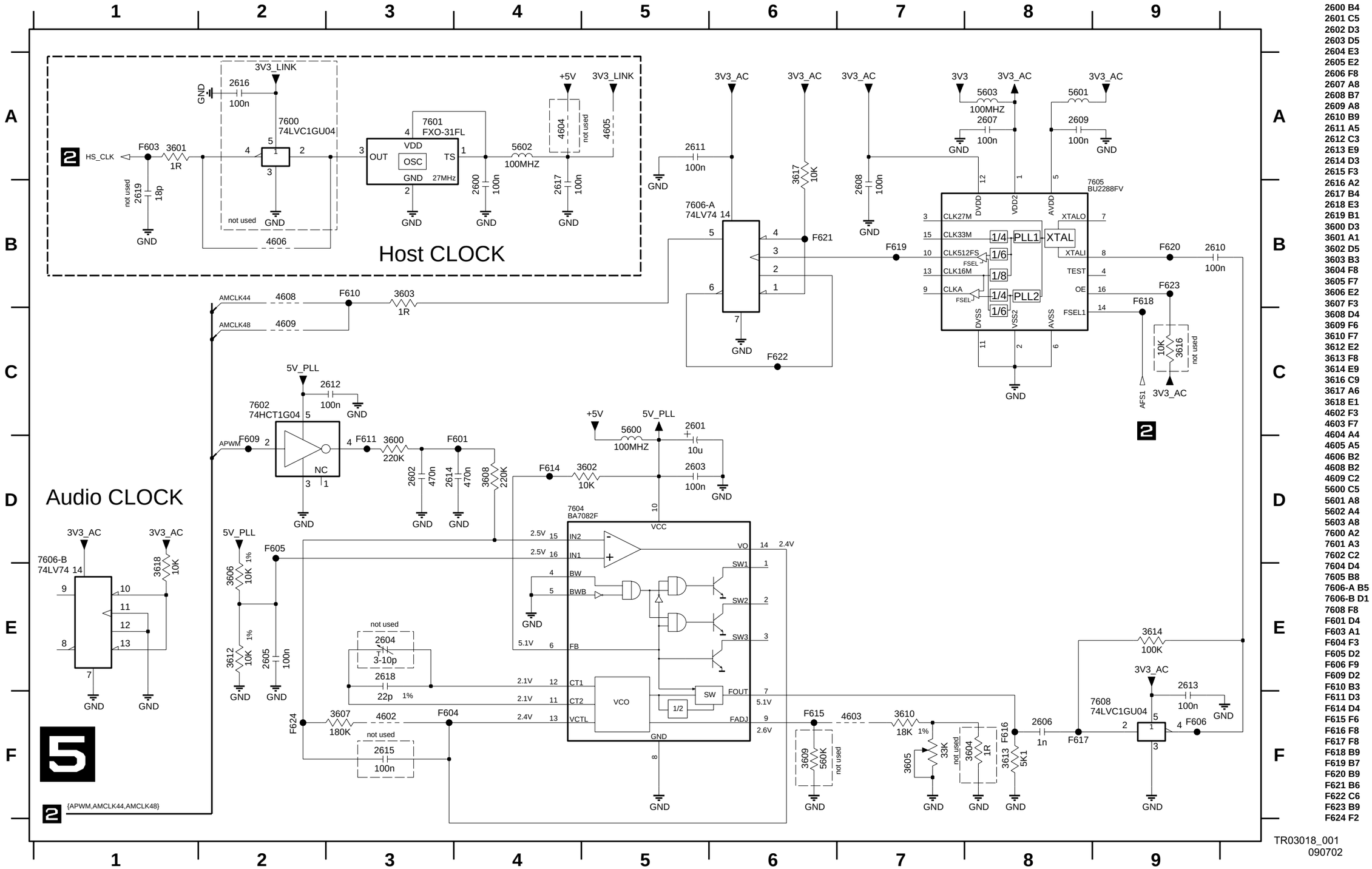
0003 I4
0004 I5
0005 I5
0006 I6
0007 I7
1500 C7
1501 H14
1502 E9
1503 F9
1906 I8
1907 I9
1908 I9
1909 I9
2500 A6
2501 C3
2502 C3
2503 C3
2504 C3
2505 C3
2506 E12
2507 E12
2508 E12
2509 C5
2510 C6
2511 C6
2512 E12
2513 E7
2514 G11
2515 C6
2516 D5
2517 D6
2518 D6
2519 D6
2520 F9
2521 F9
2522 G13
2523 G10
2524 G14
2525 H12
2526 H13
2527 A11
2528 C12
2529 F9
2530 F5
2531 F5
2532 F6
2533 F6
2534 E10
3500 B5
3501 B3
3502 B5
3503 B5
3504 C5
3505 C5
3506 D5
3507 D5
3508 D5
3509 D5
3510 E5
3511 B3
3512 B2
3514 E5
3515 F5
3516 F5
3517 G10
3518 G13
3519 G11
3520 G13
4500 A3
4501 B2
4502 F9
4503 G9
4504 G10
4507 A12
5500 A5
5501 C4
5503 E12
5504 E12
5505 A10
7500-A A1
7500-B A2
7500-C A2
7500-D A4
7500-E A3
7500-F I1
7501 F10
7505 D4
7506 E11
7507-A B11
7507-B B13
7508 C11
F501 A5
F502 A3
F503 C7
F504 C5
F505 C7
F506 C5
F507 B7
F508 B5
F509 B7
F510 B5
F511 D7
F512 D7
F513 D7
F514 D7
F515 E7
F516 E6
F517 F10
F518 D7
F519 D5
F520 D5
F521 E7
F522 D5
F523 F8
F524 D5
F525 E12
F526 E12
F527 E3
F528 F8
F529 E5
F530 E7
F531 E7
F532 E9
F533 E9
F534 F7
F535 F7
F536 F11
F537 F9
F538 G7
F539 G9
F540 G11
F541 G13
F542 G14
F543 G14
F544 G13
F545 G11
F547 G9
F548 G13
F549 H7
F550 G7
F551 F11
F552 F11
F553 G10
F556 F5
F557 F6
F558 F6
F559 E6
F560 G10
F561 F11
F562 F7
F563 A10
F564 B12
F565 B10
F566 B12
F567 A10

DVIO 1.8 Board: Clock



2600 B4
2601 C5
2602 D3
2603 D5
2604 E3
2605 E2
2606 F8
2607 A8
2608 B7
2609 A8
2610 B9
2611 A5
2612 C3
2613 E9
2614 D3
2615 F3
2616 A2
2617 B4
2618 E3
2619 B1
3600 D3
3601 A1
3602 D5
3603 B3
3604 F8
3605 F7
3606 E2
3607 F3
3608 D4
3609 F6
3610 F7
3612 E2
3613 F8
3614 E9
3616 C9
3617 A6
3618 E1
4602 F3
4603 F7
4604 A4
4605 A5
4606 B2
4608 B2
4609 C2
5600 C5
5601 A8
5602 A4
5603 A8
7600 A2
7601 A3
7602 C2
7604 D4
7605 B8
7606-A B5
7606-B D1
7608 F8
F601 D4
F603 A1
F604 F3
F605 D2
F606 F9
F609 D2
F610 B3
F611 D3
F614 D4
F615 F6
F616 F8
F617 F8
F618 B9
F619 B7
F620 B9
F621 B6
F622 C6
F623 B9
F624 F2

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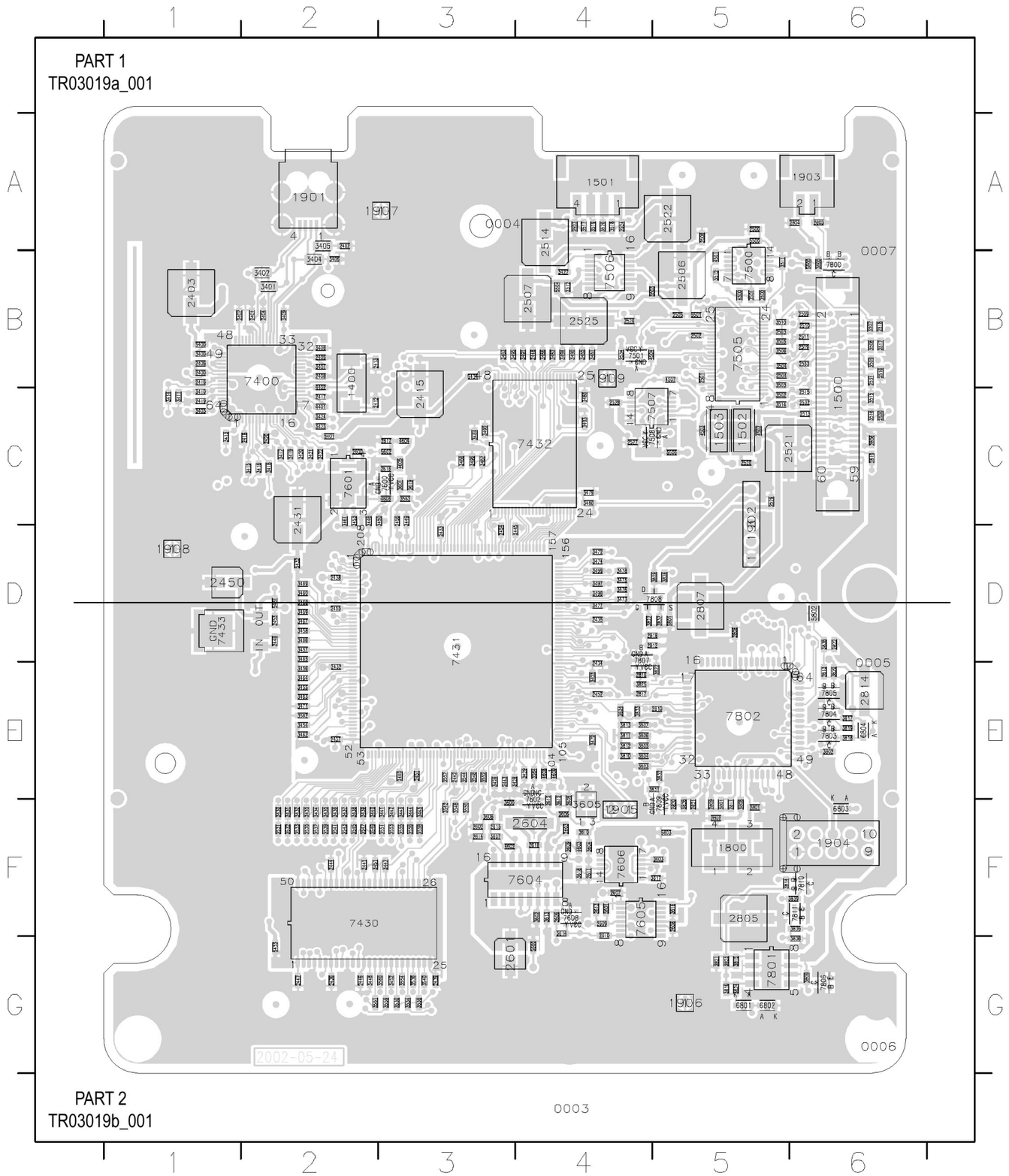
Layout DVIO 1.8 Board (Overview Top View)



1400 B2	2503 B5	2810 E5	3450 C3	3511 B5	3800 B6	5501 B5
1500 C6	2504 B5	2811 F5	3451 F2	3512 B5	3801 F5	5503 B4
1501 A4	2505 B5	2812 D4	3452 G3	3514 C5	3802 E6	5504 B4
1502 C5	2506 B5	2813 E6	3453 C2	3515 C6	3803 E4	5505 C5
1503 C5	2507 B4	2814 E6	3454 E2	3516 C6	3804 E4	5600 G4
1800 F5	2508 A5	2816 E4	3455 E2	3517 A4	3805 E4	5601 F4
1901 A2	2509 B6	2817 E4	3456 E2	3518 A4	3806 E4	5602 C3
1902 C5	2510 B6	2818 D4	3457 D2	3519 A4	3807 E4	5603 F5
1903 A6	2511 B6	2819 C6	3458 D2	3520 A4	3808 F5	5800 B6
1904 F6	2512 B4	2820 F5	3459 D2	3530 G3	3809 G6	5801 D5
1905 F4	2513 C6	2821 F5	3460 D2	3531 F2	3810 E4	5802 D6
1906 G5	2514 A4	2822 D6	3461 C2	3532 F2	3811 E4	6801 G5
1907 A3	2515 C6	3400 B1	3462 E2	3533 F2	3812 E4	6802 G5
1908 D1	2516 B6	3401 B2	3463 E2	3534 G3	3813 E4	6803 F6
1909 B4	2517 B6	3402 B2	3464 E2	3535 F2	3814 F5	6804 E6
2400 B1	2518 B6	3403 C1	3465 D2	3536 G3	3815 G5	7400 B2
2401 B2	2519 B6	3404 B2	3466 D2	3537 F2	3816 G5	7430 F2
2402 A2	2520 C5	3405 A2	3467 D2	3538 G3	3817 E6	7431 D3
2403 B1	2521 C5	3406 B2	3468 D2	3539 F2	3818 E6	7432 C4
2404 B2	2522 A5	3407 B2	3469 D2	3540 G3	3819 E6	7433 D1
2405 B2	2523 A4	3408 B2	3470 E4	3541 F2	3820 E6	7500 B5
2406 B1	2524 A4	3409 B2	3471 E2	3542 F3	3821 G5	7501 B4
2407 B1	2525 B4	3410 C1	3472 D4	3543 F2	3822 E5	7505 B5
2408 B2	2526 B4	3411 C1	3473 D4	3544 E3	3823 G5	7506 B4
2412 C2	2527 C4	3413 C1	3474 D4	3545 F2	3824 G5	7507 C4
2413 B2	2528 C4	3414 C1	3475 D4	3546 F3	3825 E4	7508 C4
2415 C3	2529 C5	3415 C2	3476 D4	3547 F2	3826 D5	7600 C3
2416 B1	2530 C6	3416 C2	3477 D4	3548 E3	3827 D4	7601 C2
2417 C2	2531 B6	3417 C2	3478 D4	3549 F2	3828 F5	7602 F4
2418 C2	2532 C6	3418 C2	3479 C4	3550 F3	3829 D5	7604 F4
2419 C1	2533 B6	3419 C2	3480 C4	3551 F3	3831 E5	7605 F4
2420 C2	2534 B4	3420 C2	3481 B4	3552 E3	3832 E5	7606 F4
2431 C2	2600 C2	3421 C2	3482 B4	3553 F3	3833 E4	7608 F4
2432 E2	2601 G3	3422 C2	3483 B3	3554 G3	3834 E4	7800 B6
2433 D3	2602 F3	3423 C2	3484 C3	3555 F3	3835 F6	7801 G5
2434 E4	2603 F4	3424 C2	3485 B4	3556 F3	3836 G6	7802 E5
2435 D4	2604 F4	3425 E4	3486 B4	3557 E3	3837 D5	7803 E6
2436 G2	2605 F4	3426 E3	3487 C3	3558 F3	3838 D6	7804 E6
2437 E2	2606 F4	3427 B4	3488 C3	3559 G3	3839 F6	7805 E6
2438 D2	2607 F4	3428 E3	3489 C4	3560 G3	4401 C2	7806 G6
2439 G3	2608 F5	3429 E4	3490 B4	3561 G2	4402 B2	7807 D4
2440 E3	2609 F4	3430 F2	3491 B4	3562 E2	4500 B5	7808 D5
2441 F2	2610 F4	3431 F2	3492 C3	3563 C3	4501 B5	7809 F5
2442 E3	2611 F4	3432 F2	3493 C4	3564 E4	4502 C5	7810 F6
2443 E3	2612 F4	3433 F2	3494 B4	3600 F3	4503 C5	7811 F6
2444 F2	2613 F4	3434 F2	3495 B3	3601 C3	4504 B4	
2445 D3	2614 F3	3435 F2	3496 C3	3602 F4	4507 B5	
2446 G2	2615 F3	3436 F2	3497 D4	3603 F5	4602 F3	
2447 G2	2616 C3	3437 F2	3498 D4	3604 F4	4603 F4	
2448 B4	2617 C3	3438 F2	3499 D4	3605 F4	4604 C3	
2449 D2	2618 F4	3439 F2	3500 B5	3606 F4	4605 C3	
2450 D1	2619 C3	3440 F2	3501 B5	3607 F3	4606 C3	
2451 E3	2801 F5	3441 F3	3502 C5	3608 F3	4608 E4	
2452 E4	2802 F5	3442 F3	3503 B5	3609 F4	4609 E4	
2453 D2	2803 A6	3443 F3	3504 B5	3610 F4	5400 B1	
2454 D3	2804 A6	3444 F3	3505 B5	3612 F4	5401 C2	
2455 D2	2805 F5	3445 F3	3506 B5	3613 F4	5431 D2	
2456 C3	2806 C6	3446 C2	3507 B6	3614 F4	5432 D2	
2500 A5	2807 D5	3447 F3	3508 B6	3616 F5	5433 G2	
2501 B5	2808 D5	3448 G2	3509 B6	3617 F5	5434 B3	
2502 B5	2809 F5	3449 C3	3510 B5	3618 F4	5500 A5	

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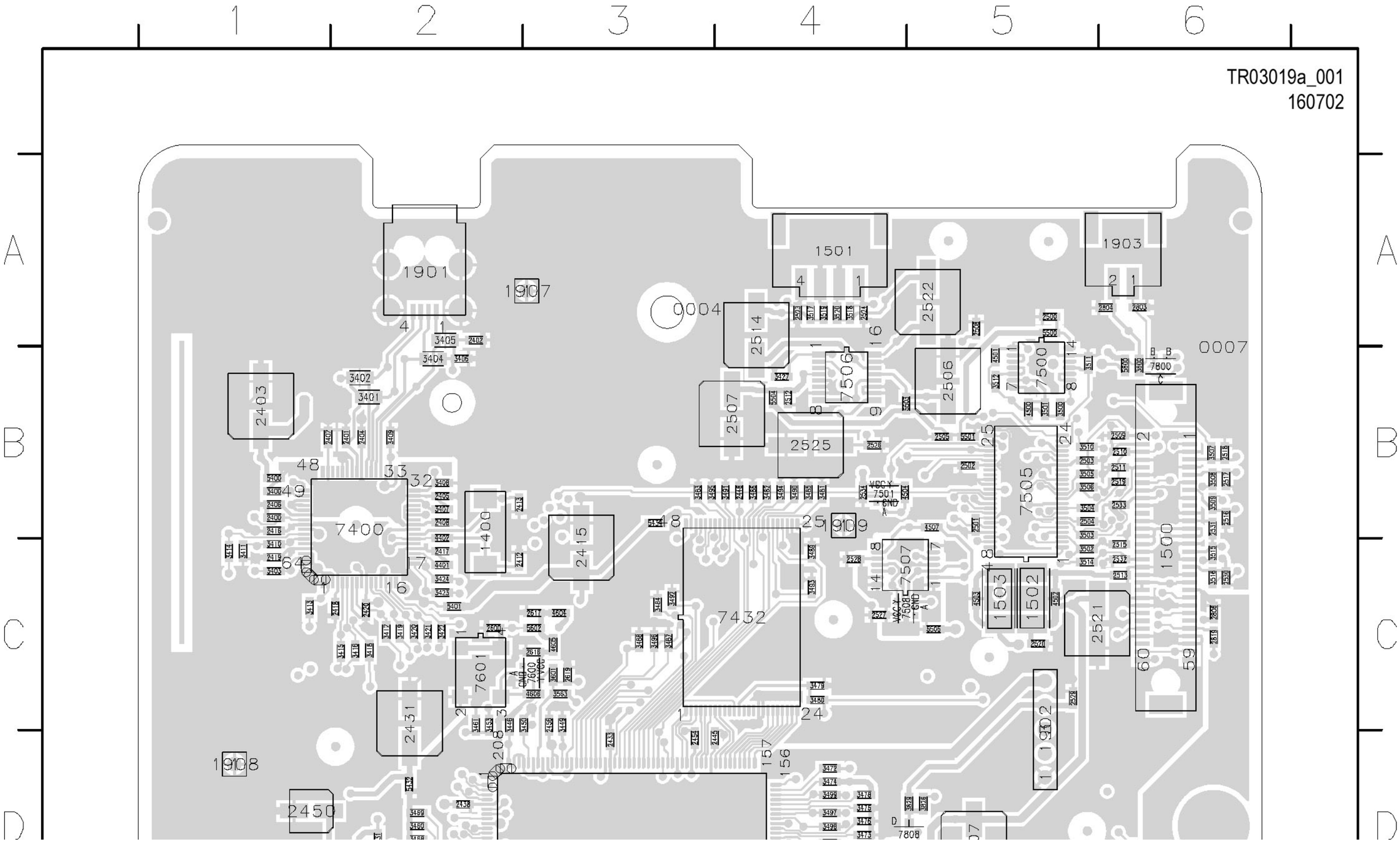
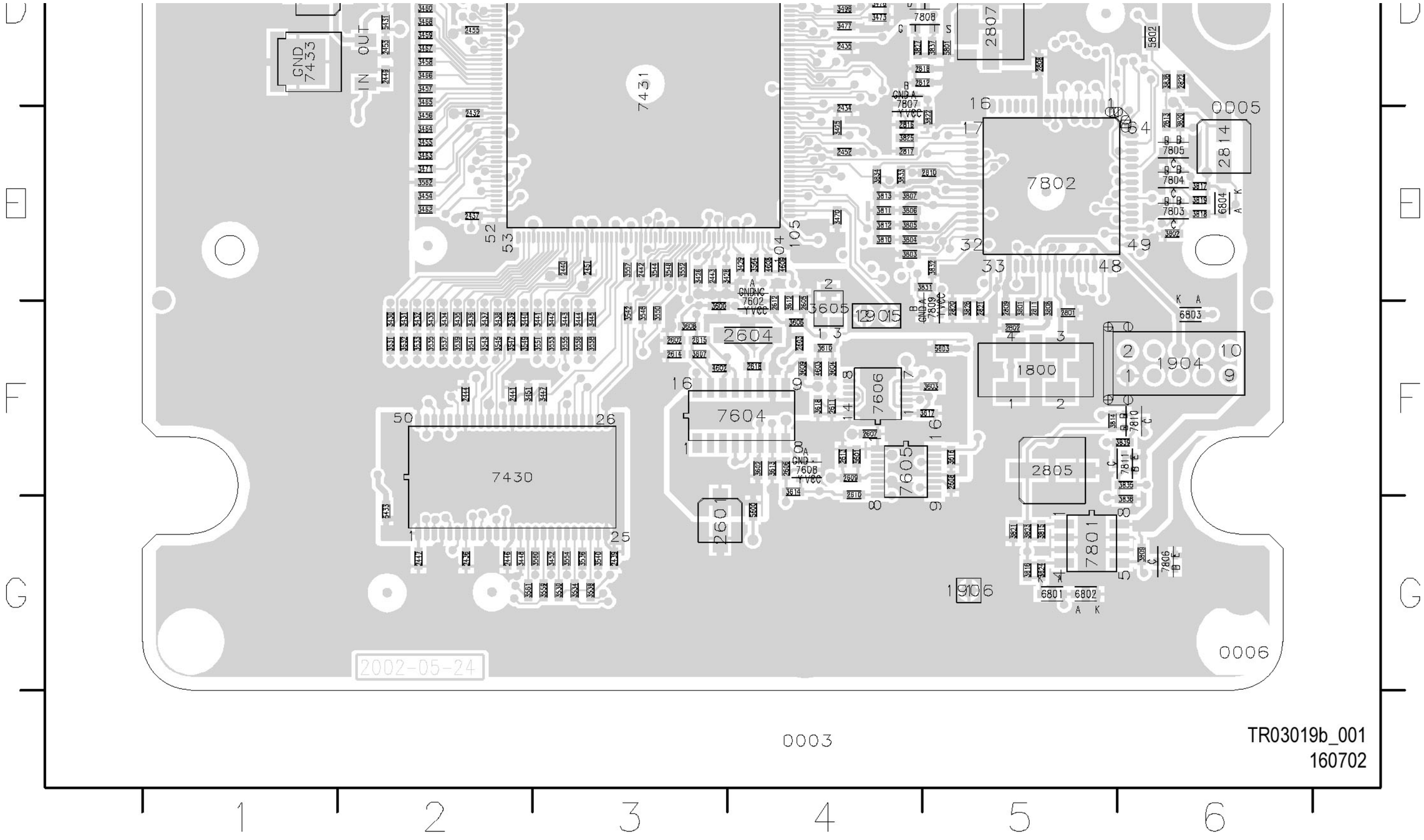
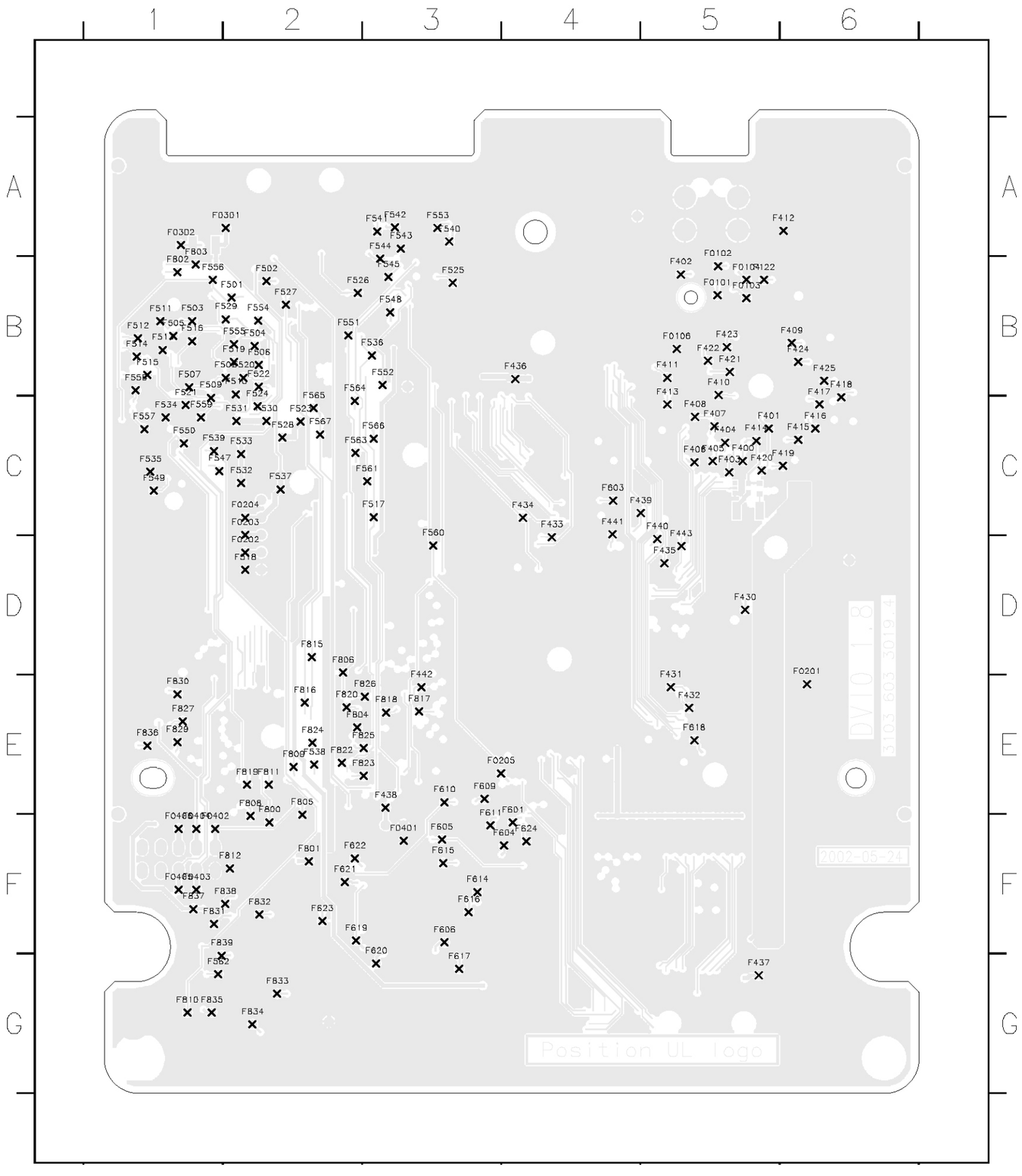
Layout DVIO 1.8 Board (Part 1 Top View)



Layout DVIO 1.8 Board (Part 2 Top View)



Layout DVIO 1.8 Board (Testlands Bottom View)



F0101 B5	F503 B1	F565 C2
F0102 B5	F504 B2	F566 C3
F0103 B5	F505 B1	F567 C2
F0104 B5	F506 B2	F601 F4
F0106 B5	F507 B1	F603 C4
F0201 E6	F508 B2	F604 F4
F0202 D2	F509 C1	F605 F3
F0203 C2	F510 B2	F606 F3
F0204 C2	F511 B1	F609 E3
F0205 E3	F512 B1	F610 E3
F0301 A2	F513 B1	F611 F3
F0302 A1	F514 B1	F614 F3
F0401 F3	F515 B1	F615 F3
F0402 F1	F516 B1	F616 F3
F0403 F1	F517 C3	F617 G3
F0404 F1	F518 D2	F618 E5
F0405 F1	F519 B2	F619 F2
F0406 F1	F520 B2	F620 G3
F122 B5	F521 C1	F621 F2
F400 C5	F522 B2	F622 F2
F401 C5	F523 C2	F623 F2
F402 B5	F524 C2	F624 F4
F403 C5	F525 B3	F800 F2
F404 C5	F526 B2	F801 F2
F405 C5	F527 B2	F802 B1
F406 C5	F528 C2	F803 B1
F407 C5	F529 B2	F804 E2
F408 C5	F530 C2	F805 F2
F409 B6	F531 C2	F806 D2
F410 B5	F532 C2	F808 F2
F411 B5	F533 C2	F809 E2
F412 A6	F534 C1	F810 G1
F413 C5	F535 C1	F811 E2
F414 C5	F536 B3	F812 F2
F415 C6	F537 C2	F815 D2
F416 C6	F538 E2	F816 E2
F417 C6	F539 C1	F817 E3
F418 C6	F540 A3	F818 E3
F419 C6	F541 A3	F819 E2
F420 C5	F542 A3	F820 E2
F421 B5	F543 A3	F822 E2
F422 B5	F544 B3	F823 E3
F423 B5	F545 B3	F824 E2
F424 B6	F547 C1	F825 E3
F425 B6	F548 B3	F826 E3
F430 D5	F549 C1	F827 E1
F431 E5	F550 C1	F829 E1
F432 E5	F551 B2	F830 E1
F433 D4	F552 B3	F831 F1
F434 C4	F553 A3	F832 F2
F435 D5	F554 B2	F833 G2
F436 B4	F555 B2	F834 G2
F437 G5	F556 B1	F835 G1
F438 E3	F557 C1	F836 E1
F439 C5	F558 B1	F837 F1
F440 D5	F559 C1	F838 F2
F441 C4	F560 D3	F839 G1
F442 E3	F561 C3	
F443 D5	F562 G1	
F501 B2	F563 C2	
F502 B2	F564 C2	

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3. Alignments

3.1 Adjustment DVIO 1.8 PCB

This adjustment sets the free running frequency of the VCO of the audio PLL. It should be carried out after replacement of IC 7604.

1. Disconnect DVD+RW set from the mains.
2. Plug DVIO1.8 board via edge-connector onto Digital Board (DVIO board is vertically oriented, so that both sides of the PCB are accessible for measurements).
3. Connect DVD+RW set to the mains.
4. Turn DVD+RW set on and select any video input source except the DV input.
5. Check the signal at test point F611 with an oscilloscope. The signal should be 5V digital with 50% duty-cycle.
6. Measure the frequency of the signal at test point F610 and adjust the potentiometer 3605 to get a frequency of 12.288MHz ±50kHz (after removing the screwdriver from the potentiometer).
   - 6a. In case the frequency can not be increased sufficiently, replace capacitor 2618 by NP0-type capacitor with 18pF. Adjust afterwards again the frequency with the potentiometer.
   - 6b. In case the frequency can not be decreased sufficiently, add (3pF-10pF) trim-capacitor in parallel to capacitor 2618 or replace capacitor 2618 by NP0-type capacitor with 27pF.Adjust afterwards again the frequency with the potentiometer (and/or trim-capacitor).
7. Switch DVD+RW set to Stand-by mode.
8. Disconnect the DVD+RW set from the mains.
9. Plug DVIO1.8 board directly (without edge connector) onto Digital Board.
10. Connect DVD+RW set to the mains.
11. Connect a DV-source that transmits DV-video data with audio to the DVD+RW set.
12. Turn DVD+RW set on, select DV input, and switch DVD+RW set appropriately to output the decoded signal. Audio should be output without distortion.

4. Circuit-, IC Descriptions and List of Abbreviations

4.1 Divio 1.8 Board

4.1.1 Short Description of the Module:

The DVIO Module is a decoder for DV streams. Input is a stream from a DV-camcorder via IEEE1394. Outputs are CCIR656 Video and Analog audio (L+R). A serial control interface is present.
The following picture shows the location of the DVIO Module inside the DVDR set.

Description DIVIO Module

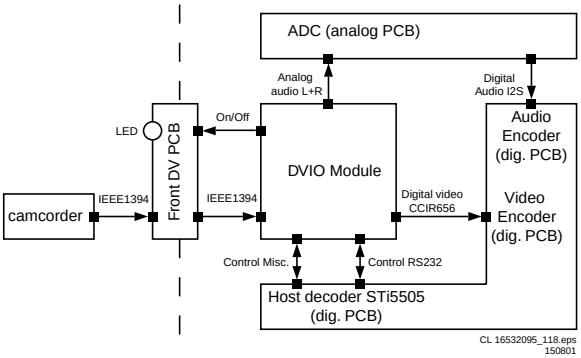

Figure 4-1

4.1.2 Block Diagram

Block Diagram DVIO1.8

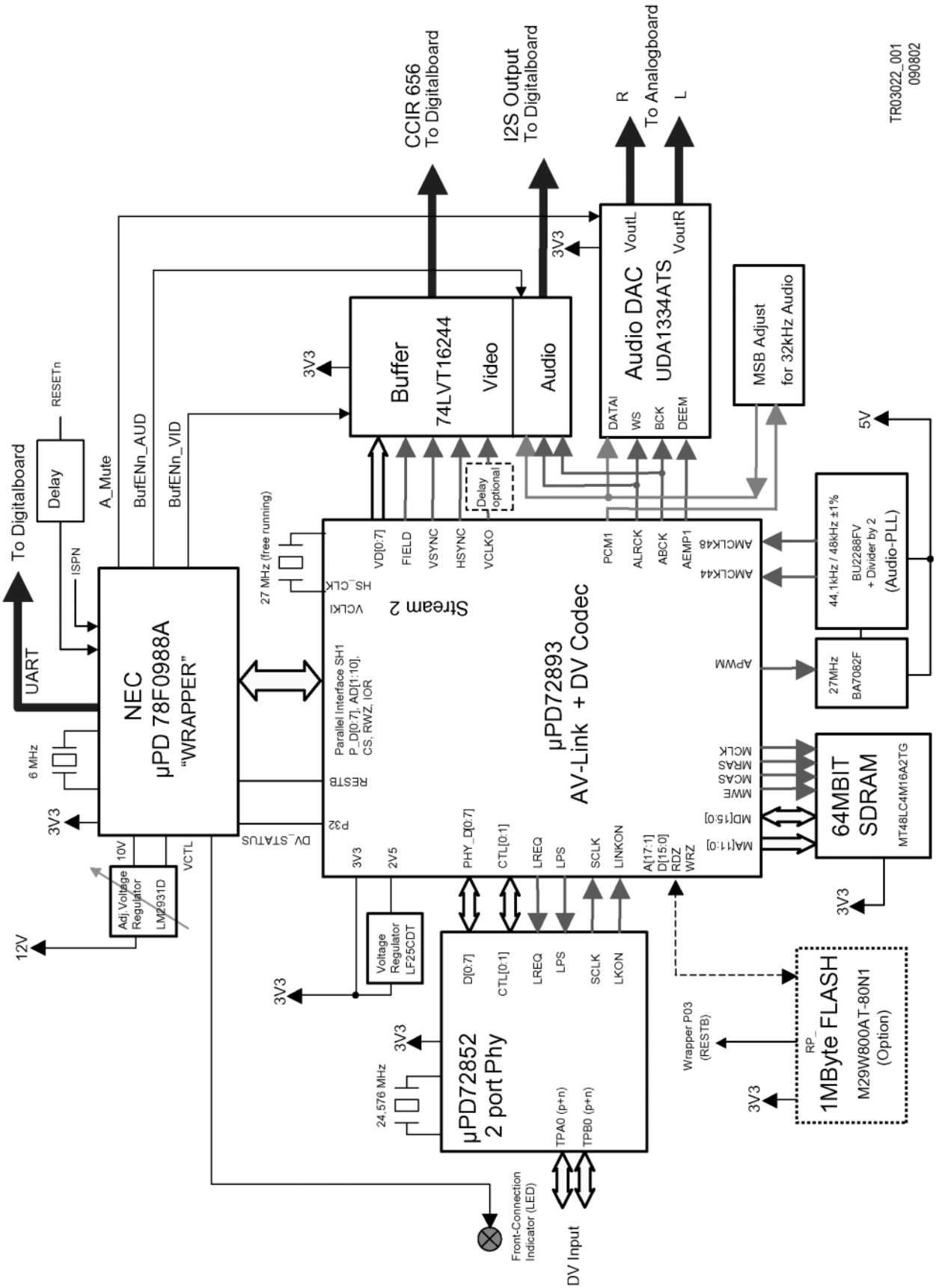

Figure 4-2

4.1.3 Functional Description

The DVIO module consists of the following blocks (see blockdiagram):

1. IEEE1394 Interface
   - uPD72852 (7400) (Phy)
   - uPD72893 (7431) (Link part)
2. Micro-controller
   - uPD78F0988 (7802)
   - Voltage regulator LM2931 for generation of 10V programming voltage (7801)
3. Reset-circuitry
   - Power-on reset
   - Reset pulse-shortener
4. DV-Decoder
   - uPD72893 (7431) (Codec part)
   - 16MBit SDRAM (7430)
   - optional Flah-Memory M29W800AT for Firmware-Update of uPD72893 (7432)
5. Clocking & Audio PLL
   - Clock oscillator FXO-31FT (7601)
   - Audio-PLL: Voltage controlled oscillator BA7082F (7604), clock generator BU2288FV (7605), and clock divider 74LV74 (7606-A)
6. Audio Format adaption (MSB justified -> I2S), option
   - 74LV74 (7507-A, -B)
7. Audio & Video output
   - Audio DAC UDA1334ATS(7602)
   - Clock delay(7500)
   - Tristate buffer(7505)

IEEE1394 Interface

The 1394 interface consists of a uPD72852 physical layer and a uPD72893 link layer IC (uPD72893 integrated also DV-Decoder).
It has the following features:

- S400 operation (400 megabit per second)
- Two i.Link ports (4 pin), only one used
- AV link port

Micro-Controller

The uPD78F0988 processor has following extra features:

- 60 kilobyte of flash memory as program memory
- 2 kilobyte of internal data memory
- watchdog timer
- On board ISP(In-System-Programming) functionality

ISP

By use of In-System-Programming, it is possible to update the software of the DVIO board that is in the uPD78F0988. ISP can be made active by resetting the processor and keeping the ISPN pin low during reset. During ISP, the ISPN signal on the board has to be kept low. A programming voltage of 10V is activeted by the uPD78F0988 itself at the Vpp pin before programming procedure starts. When the ISP mode is active, the new program can be sent to the microprocessor through the serial port.

Reset-circuitry

The reset-circuitry consists of two parts.
First part (around transistor 7803) generates a reset pulse when the board is powered up.
Second part (around transistors 7804 & 7805) acts as a reset-pulse shortener, i.e. a short reset pulse (4ms) is generated from the input signal RESETn which is much longer (usually 100ms). This is required to ensure correct operation of the Micro-controller after booting-up when RESETn is again deactivated

DV-Decoder

The uPD72893 decodes the stream into video data in 656 format and audio data in I2S format.
The microprocessor has the ability to read the status registers of the uPD72893. By reading these registers, extra data from the DV stream, that is not decoded into audio or video, can be sent to the digital board using pin TXD of the serial interface. This data includes time stamp and some more.

Clocking and Audio PLL

The FXO-31FT generates the free-running 27MHz system clock. Video part of input DV-stream is in the uPD72893 adapted to the local 27MHz clock domain (skip, repeat frame). Because audio clock (11.2896Mz [fs=44.1kHz] or 12.288MHz [fs=32kHz, 48kHz]).
The uPD72893 integrates the phase comparator that drives the VCO BA7082F to a nominal frequency of 27MHz which in turn is converted by BU2288FV and 74LV74 to 11.2896MHz or 12.288Mhz, respectively.
The uPD72893 controls directly the frequency ratio of the BU2288FV.

Audio Format adaptation (MSB justified -> I2S), option

Due to a bug in 1st version of uPD72893 digital audio output is not correct in I2S mode when in 32kHz operation. As a workaround uPD72893 is generally configured in MSB justified mode and conversion to I2S mode is done externally via a 74LV74 device.
Can be disabled with later versions of uPD72893.

Audio & Video Output

The audio I2S data are sent to audio DAC UDA1334. Analog audio left and right signals are connected to the analog board. The tri-state buffer enables the digital video stream to the Video Input Processor on the digital board when the DV source is selected.
The clock delay synchronizes the AV clock with the AV data at the output.

4.2 IC's Divio 1.8

4.2.1 IC7400: uPD72852

DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD72852

IEEE1394a-2000 COMPLIANT 400 Mbps TWO-PORT PHY LSI

The μPD72852 is a two-port physical layer LSI that complies with the IEEE1394a-2000 specifications.

The μPD72852 supports transfers of up to 400 Mbps and consumes less power than the μPD72850B. The μPD72852 is suitable for battery systems with an IEEE1394 interface.

FEATURES

- The two-port physical layer LSI complies with IEEE1394a-2000
- Fully interoperable with IEEE1394 std 1394 Link (FireWire™, i.LINK™)
- Meets Intel™ Mobile Power Guideline 2000
- Full IEEE1394a-2000 support includes: Suspend/Resume, connection debounce, arbitrated short bus reset, multi-speed concatenation, arbitration acceleration, fly-by concatenation
- Fully compliant with OHCI requirements
- Small package: 64-pin plastic LQFP
- Super low power: 68 mA (Operating mode)
  : 115 μA (Suspend mode)
- Data rate: 400/200/100 Mbps
- Supports PHY pinging and remote PHY access packets
- 3.3 V single power supply (if power not supplied via node: 3.0 V single power supply)
- 24.576 MHz crystal clock generation, 393.216 MHz PLL multiplying frequency
- 64-bit flexible register incorporated in PHY register
- Electrically isolated Link interface
- Supports LPS/Link-on as part of PHY/Link interface
- External filter capacitors for PLL not required
- Extended Resume signaling for compatibility with legacy DV devices
- System power management by signaling of node power class information
- Cable power monitor (CPS) is equipped

ORDERING INFORMATION

Part number	Package
μPD72852GB-8EU	64-pin plastic LQFP (10 x 10)

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The mark ★ shows major revised points.

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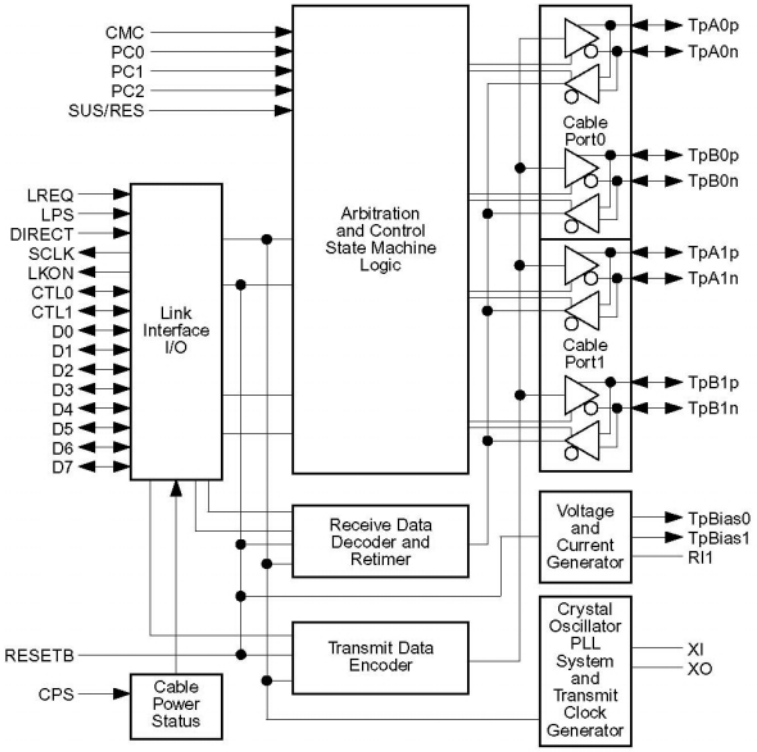
BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 Cable Interface Pins

Name	Pin No.	I/O	Function
TpA0p	39	I/O	Port 0 twisted pair cable A positive phase I/O
TpA0n	38	I/O	Port 0 twisted pair cable A negative phase I/O
TpB0p	37	I/O	Port 0 twisted pair cable B positive phase I/O
TpB0n	36	I/O	Port 0 twisted pair cable B negative phase I/O
TpA1p	46	I/O	Port 1 twisted pair cable A positive phase I/O
TpA1n	45	I/O	Port 1 twisted pair cable A negative phase I/O
TpB1p	44	I/O	Port 1 twisted pair cable B positive phase I/O
TpB1n	43	I/O	Port 1 twisted pair cable B negative phase I/O
SUS/RES	19	I	Suspend/Resume function select 1: Suspend/Resume on (IEEE1394a-2000 compliant) 0: Suspend/Resume off (P1394a draft 1.3 compliant)
CPS	32	I	Cable power status Connect to the cable through a 390 kΩ resistor and to GND through a 100 kΩ resistor. 0: Cable power fail 1: Cable power on

1.2 Link Interface Pins

Name	Pin No.	I/O	Function
D0	8	I/O	Data input/output (bit 0)
D1	9	I/O	Data input/output (bit 1)
D2	11	I/O	Data input/output (bit 2)
D3	12	I/O	Data input/output (bit 3)
D4	14	I/O	Data input/output (bit 4)
D5	15	I/O	Data input/output (bit 5)
D6	17	I/O	Data input/output (bit 6)
D7	18	I/O	Data input/output (bit 7)
CTL0	5	I/O	Link interface control (bit 0)
CTL1	6	I/O	Link interface control (bit 1)
LREQ	63	I	Link request input
SCLK	2	O	Link control output clock LPS 1: 49.152 MHz output LPS 0: Clamp to 0 (The clock signal will be output within 25 μsec after change to "0")
LPS	59	I	Link power status input 0: Link power off 1: Link power on (PHY/Link direct connection)
LKON	58	O	Link-on signal output Link-on signal is 6.144 MHz clock output. Please refer to **4.2 Link-on Indication**.
DIRECT	50	I	PHY/Link isolation barrier control input 0: Isolation barrier 1: PHY/Link direct connection

1.3 Control Pins

Name	Pin No.	I/O	Function
PC0	26	I	Power class set input This pin status will be loaded to Pwr_class bit which allocated to PHY register 4H. IEEE1394a-2000 chapter [4.3.4.1]
PC1	27	I	
PC2	28	I	
CMC	30	I	Configuration manager capable setting This pin status will be loaded to Contender bit which allocated to PHY register 4H. 0: Non contender 1: Contender
RESETB	55	I	Power-on reset input Connect to GND through a 0.1 μF capacitor. 0: Reset 1: Normal
SPD	61	I	Speed select 0: MAX. S200 1: MAX. S400

1.4 IC

Name	Pin No.	I/O	Function
IC(AL)	29, 51	-	Internally Connected (Low Clamped) Connect to GND.
IC(DL)	3	-	Internally Connected (Low Clamped) Connect to GND.

1.5 Power Supply Pins

Name	Pin No.	I/O	Function
AV_{DD}	25, 31, 40, 47, 54	-	Analog power
AGND	24, 33, 35, 42, 49, 52, 53	-	Analog GND
DV_{DD}	4, 10, 20, 56, 60	-	Digital V_{DD}
DGND	1, 7, 13, 16, 21, 57, 64	-	Digital GND

1.6 Other Pins

Name	Pin No.	I/O	Function
TpBias0	41	O	Port 0 twisted pair output
TpBias1	48	O	Port 1 twisted pair output
RI1	34	-	Resistor connection pin1 for reference current generator Connect to GND through a 9.1 kΩ resistor.
XI	23	-	Crystal oscillator connection XI
XO	22	-	Crystal oscillator connection XO
TEST	62	-	Test pin Internally connected (Low clamped). Connect to GND.

4.2.2 IC7431: uPD72893

PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD72893

IEEE1394 LINK LAYER CONTROLLER WITH DV CODEC

DESCRIPTION

The μPD72893 is an IEEE1394 link layer controller developed for digital AV systems and features an on-chip 32-bit RISC CPU (V850E) for IEEE1394 processing.

This link layer controller has two stream interface channels to transmit/receive image data conforming to the IEC61883 Standard, such as MPEG and VD, and these channels can be independently used for transmission and reception. In addition, a total of 8 KB of FIFO buffer space is provided to transmit/receive isochronous signals. This buffer space can be allocated as transmit and receive FIFO buffers in 2 KB units.

The μPD72893 supports IEEE1394 bus control and AV/C commands via the on-chip CPU, as well as external control using either a serial or a parallel interface.

FEATURES

IEC61883 functions

- Supports DVB, DSS, and DVCR formats.
- Supports AV/C commands (for D-VHS).

DV codec functions

- Supports IEEE1394 DV
  Video signal :
  NTSC 720 x 480 x 29.97 Hz (525-60 system)
  PAL 720 x 576 x 25 Hz (625-50 system)
  Audio signal :
  2 channels (48 kHz, 44.1 kHz, 32 kHz, 16 bits)
  4 channels (32 kHz, 12 bits)
- Supports digital AV signal
  Video signal :
  ITU-R REC656
  8 bits, Y/Cb/Cr 4:2:2 (Video CLK = 27 MHz)
  Audio signal :
  Audio PCM serial
  Input 16-bit resolution MCK44, MCK48
  Output LRCKO, BCKO

CPU functions

- 32-bit RISC CPU (V850E)
- Operating frequency : 27 MHz input (@54 MHz internally)
- Memory : ROM 192 KB
  RAM 60 KB

Interface functions

- Stream port (MPEG-TS, DV): 2 ports
  8-bit parallel bus/serial bus support
  Asynchronous transfer format Maximum transfer rate: 13.5 Mbyte/s
- Host interface
  Parallel interface: 16-bit address/data separated type, ISA, 68000, and SH-1 selectable
- ROM interface
  Flash ROM interface. SRAM is also connectable.
- EEPROM™ interface
  For IEEE1394 configuration data
- General-purpose I/O ports: 11 (multiplexed with function pins)

Other functions

- Power-saving function (HALT mode and software STOP mode)
- Supply voltage: Peripheral 3.3 V ±0.3 V
  Internal 2.5 V ±0.2 V
- Package: 208-pin plastic QFP (FP)

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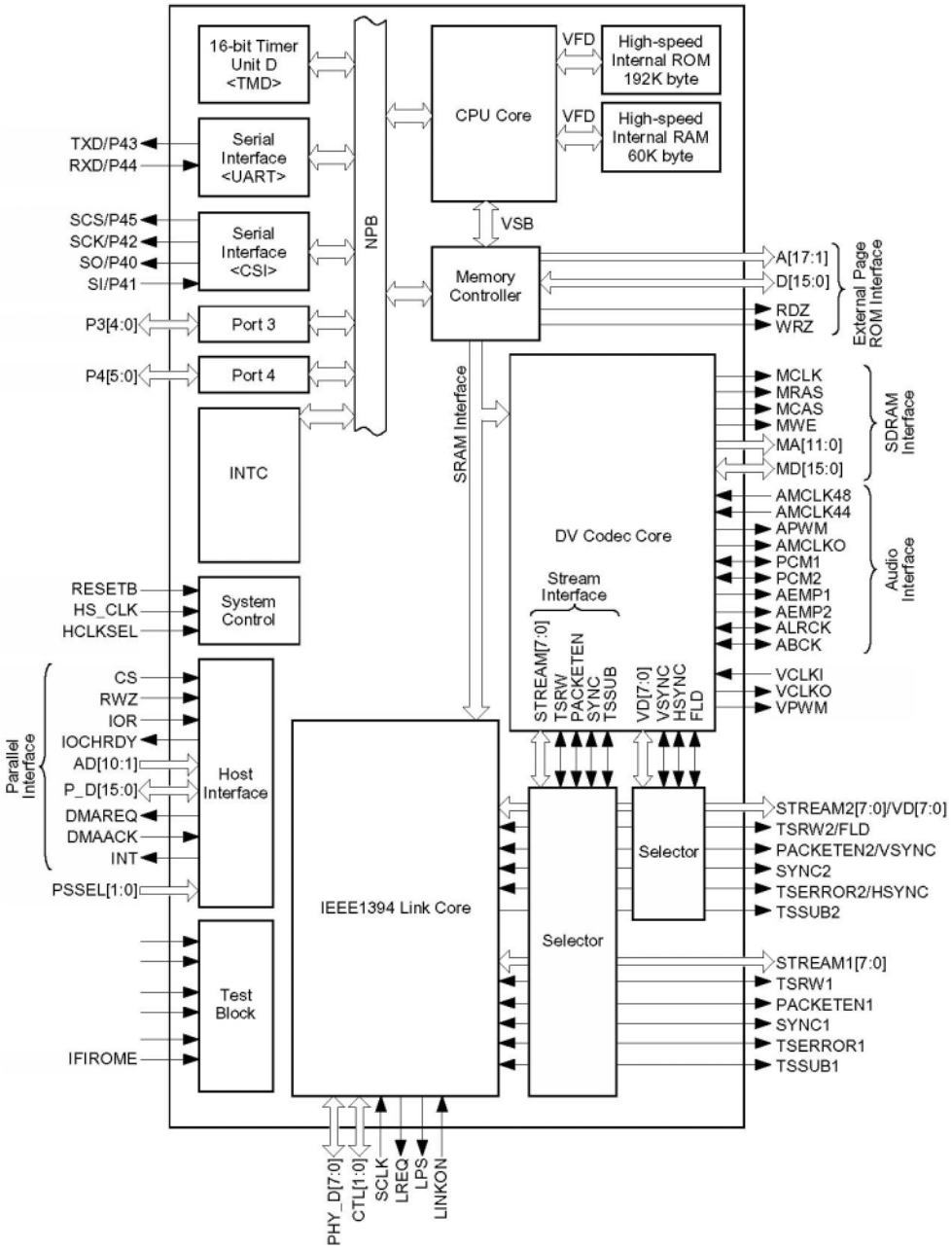
OVERVIEW OF FUNCTIONS

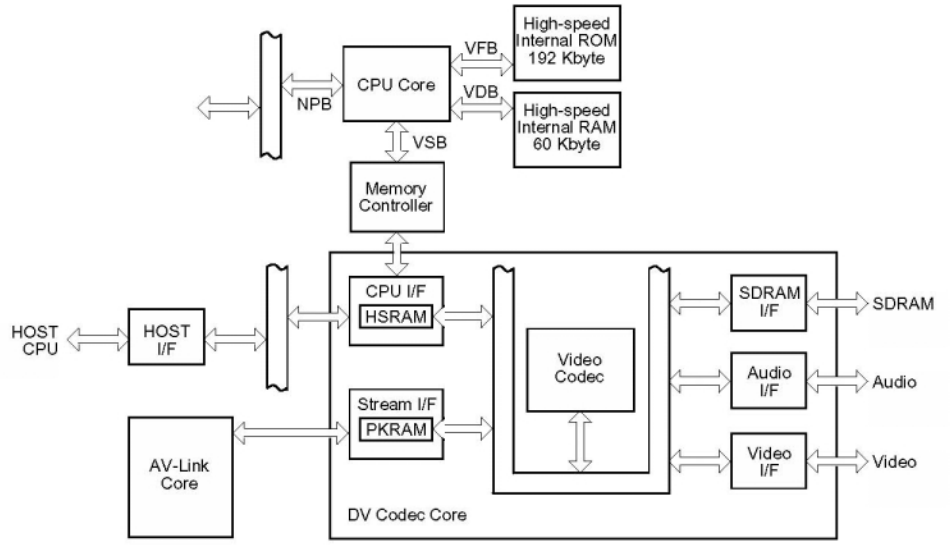
Product Name	μPD72893
IEEE1394 Link core	Conforms to IEEE1394-1995 and IEEE1394a-2000 Standards. Supports data rates of 400 Mbps, 200 Mbps, and 100 Mbps. Two FIFOs for ASYNC transmission/reception Concatenate Isochronous transmission and asynchronous stream transmission are possible. Conforms to IEC61883. CSR's and Config_ROM (RAM) that are frequently accessed incorporated so that response_packet is automatically generated and transmitted by concatenate transfer.
CPU core	32-bit RISC CPU (V850E)
Internal ROM	192 KB
Internal RAM	60 KB
Parallel interface	- 16-bit address/data separated bus (select one mode from the following bus formats) 6800 (Motorola), ISA, SH-1
Serial interface	- Asynchronous serial interface (UART) x 1 channel - Clocked serial interface (CSI) x 1 channel
External ROM connection function	- Page ROM/ROM flash ROM interface - SRAM interface - EEPROM interface
Operating frequency	- 27 MHz clock input - On-chip CPU: 54 MHz (generated by internal PLL from 27 MHz) - IEEE1394 Link core: 49.152 MHz (operates on SCLK from PHY)
Supply voltage	- Peripheral: V_{DD} = 3.3 ±0.3 V - Internal: V_{DD} = 2.5 ±0.2 V
Package	208-pin plastic QFP (fine pitch) (28 x 28)

BLOCK DIAGRAM

μPD72893 Block Diagram



DV Codec Unit Block Diagram



1. PIN FUNCTIONS

(1) Link-related pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
LINKON	18	I	Link-on signal input. Clock input. Inputs 0 if LPS is active.	–	I	–
LPS	17	O	Link power status output Link power OFF : 0 Link power ON : 2.7 MHz pulse output (54 MHz host clock divided by 20)	–	O	–
LREQ	16	O	Link request output	–	O	–
SCLK	15	I	Clock input for Link control When LPS is active : 49.152 MHz input LPS = 0 : Fixed to 0	–	I	–
CTL[1:0]	12, 13	I/O	PHY/Link control signal I/O	–	I	–
PHY_D[7:0]	2 to 4, 6 to 8, 10, 11	I/O	Data I/O between PHY and Link	–	I	–
STREAM1[7:0]	26 to 19	I/O	ISO data bus of stream interface 1 Note	–	I	–
PACKETEN1	27	I/O	Packet enable signal I/O to/from stream interface 1 Note	H/L	I	–
TSERROR1	28	I/O	Packet error signal I/O to/from stream interface 1 Note	H/L	I	–
TSRW1	29	I/O	Data read/write enable signal I/O to/from stream interface 1 Note	–	I	–
SYNC1	30	I/O	Frame sync signal I/O to/from stream interface 1 Note	H/L	I	–
TSSUB1	32	I/O	I :Inputs the packet gap signal when the stream is input through the stream interface O :Not used. Connect this pin to V_{DD} or GND via a resistor.	H/L	I	–
STREAM2[7:0]	47 to 40	I/O	ISO data bus of stream interface 2 Note	–	I	VD[7:0]
PACKETEN2	33	I/O	Packet enable signal I/O to/from stream interface 2 Note	H/L	I	VSYNC
TSERROR2	34	I/O	Packet error signal I/O to/from stream interface 2 Note	H/L	I	HSYNC
TSRW2	36	I/O	Data read/write enable signal I/O to/from stream interface 2 Note	–	I	FLD
SYNC2	37	I/O	Frame sync signal I/O to/from stream interface 2. Note	H/L	I	–
TSSUB2	38	O	Not used. Leave open.	–	O	–

Note When this signal is switched for transmission or reception to/from IEEE1394, it must be controlled that output does not conflict.
To prevent a floating state, connect a pull-up or pull-down resistor to this pin.

Remark Active H/L: A high or low level can be selected as the active level.

(2) Video interface pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
VCLKI	50	I	Video clock input (27 MHz)	–	–	–
VCLKO	51	O	Video clock output (27 MHz)	–	–	–
VD[7:0]	47 to 40	I/O	Video data signal	–	–	STREAM2[7:0]
VSYNC	33	I/O	Vertical sync video signal Note	L	–	PACKETEN2
HSYNC	34	I/O	Horizontal sync video signal Note	L	–	TSERROR2
FLD	36	I/O	Field index signal Note	–	–	TSRW2
VPWM	53	O	PWM signal for video PLL	–	–	–

Note When this signal is switched for transmission or reception to/from IEEE1394, it must be controlled that output does not conflict.

(3) Audio interface pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
AMCLK48	104	I	Audio master clock input (for 48 kHz sampling frequency)	–	–	–
AMCLK44	103	I	Audio master clock input (for 44.1 kHz sampling frequency)	–	–	–
AMCLKO	101	O	Audio master clock output	–	–	–
PCM1	96	I/O	Audio PCM serial data Note With 2 channels: CH1 With 4 channels: CH1 or CH1 and CH2 mixed	–	–	–
PCM2	97	I/O	Audio PCM serial data Note With 2 channels: Mute With 4 channels: CH2	–	–	–
AEMP1	98	O	PCM1 emphasis ON/OFF for PCM1 output	H	–	–
AEMP2	100	O	PCM2 emphasis ON/OFF for PCM2 output	H	–	–
ALRCK	93	I/O	Audio LR clock Note L-ch: High R-ch: Low	–	–	–
ABCK	94	I/O	Audio bit clock Note	–	–	–
AFS[1:2]	48, 49	O	Audio sampling frequency AFS2 AFS1 44.1 kHz 0 1 48 kHz 0 0 32 kHz 1 0	–	–	–
APWM	102	O	PWM signal for audio PLL	–	–	–

Note The input changes according to the switching of the encode/decode mode. It must be controlled so that the output does not conflict when the mode is switched.
To prevent a floating state, connect a pull-up or pull-down resistor to this pin.

(4) SDRAM interface pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
MCLK	77	O	CLK pin connection for SDRAM	–	–	–
MRAS	76	O	RAS pin connection for SDRAM	–	–	–
MCAS	75	O	CAS pin connection for SDRAM	–	–	–
MWE	74	O	WE pin connection for SDRAM	–	–	–
MA[11:0]	92, 90 to 83, 81 to 79	O	Address pin connection for SDRAM	–	–	–
MD[15:0]	73 to 69, 66 to 64, 62 to 57, 55, 54	I/O	Data pin connection for SDRAM These pins must be pulled up or down and then must be directly connected to the SDRAM pins.	–	–	–

(5) Host interface pins

(a) Parallel interface pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
CS	117	I	Parallel interface chip select input	L	I	–
RWZ	119	I	Parallel interface read/write control input ISA bus, SH-1 bus : Write strobe 68000 bus : Read/write select signal	L	I	–
IOR	120	I	Parallel interface IO read control input ISA bus, SH-1 bus : Read strobe 68000 bus : Data strobe (DS)	L	I	–
IOCHRDY	123	O	Parallel interface ready output	L	O	–
AD[10:1]	116 to 107	I	Parallel interface address input	–	I	–
P_D[15:0]	143 to 141, 139 to 132, 130 to 128, 126, 125	I/O	Parallel interface data input/output	–	I	–
DMAREQ	122	O	DMA request output	L	O	SIO_CNTO
DMAACK	121	I	DMA acknowledge input for parallel interface	L	I	SIO_CNTI

(b) Serial interface pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
SO	145	O	Serial transmit data output for clocked serial interface (CSI)	–	O	P40
SI	146	I	Serial receive data input for clocked serial interface (CSI)	–	I	P41
SCK	147	O	Clock output for clocked serial interface (CSI)	–	O	P42
TXD	149	O	Serial transmit data output for asynchronous serial interface (UART)	–	O	P43
RXD	150	I	Serial transmit data input for asynchronous serial interface (UART)	–	I	P44
SCS	151	O	Chip select output for clocked serial interface (CSI)	–	O	P45
SIO_CNTI	121	I	Control input for asynchronous serial interface (UART) Externally input data is loaded in synchronization with the end of RXD of UART.	–	I	DMAACK
SIO_CNTO	122	O	Control output for asynchronous serial interface (UART)	–	O	DMAREQ

(c) Others

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
INT	124	O	Interrupt output to external device	H	O	–
PSSEL[1:0]	106, 105	I	Parallel/serial interface selection. These signals select a parallel or serial interface as the external interface. PSSEL[1:0] Selected interface 00 Serial interface (UART) 01 Parallel interface (ISA bus) 10 Parallel interface (68000 bus) 11 Parallel interface (SH-1 bus)	–	I	–

(6) Port pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
P30	204	I/O	Port 3. This is a 4-bit I/O port that can be set in the input or output mode in 1-bit units. P30 : Connect this pin to GND via a resistor. P32 : This pin outputs an interrupt to the external device to read the DV status. It cannot be used as a port pin when DV is used.	–	I	–
P31	152					–
P32	153					–
P33	154					–
P34	155					–
P40	145	I/O	Port 4. This is a 6-bit I/O port that can be set in the input or output mode in 1-bit units. P40 to P45 are multiplexed with the pins described under the heading Alternate Function (they cannot be used as general-purpose port pins).	–	I	SO
P41	146					SI
P42	147					SCK
P43	149					TXD
P44	150					RXD
P45	151					SCS

(7) External ROM connection pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
D[15:0]	196, 194 to 189, 186 to 178	I/O	External ROM data bus External ROM data bus used to access external ROM	–	I	–
A[17:1]	175, 174, 172, 171, 169 to 167, 165 to 156	O	External ROM address bus External ROM address bus used to access external ROM. A space of 256 KB can be addressed.	–	O	–
RDZ	176	O	ROM read This is a strobe signal that indicates a read cycle to the external ROM. It is inactive in the idle state.	L	O	–
WRZ	177	O	ROM write This is a strobe signal that indicates a write cycle to the external ROM.	L	O	–

(8) Clock and reset pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
RESETB	1	I	Reset. RESETB is asynchronous input. If a signal with a specified low-level width is input to this pin independently of the operating clock, a system reset is effected, taking precedence over all the other operations. This signal can also be used to clear the power-saving mode (HALT or software STOP), as well as for normal initialization and starting. **Caution RESETB is active-low.**	L	I	–
HS_CLK	202	I	Host clock. This pin inputs the clock that is to be supplied to the CPU core and internal peripheral I/O. This clock is input to the internal clock generator. An internal clock is generated according to the value of HCLKSEL and is supplied to the CPU core and internal peripheral I/O. Usually, input a clock of 27 MHz to this pin.	–	I	–
HCLKSEL	197	I	Host clock selection. This pin inputs the clock that is to be supplied to the CPU core and internal peripheral I/O. The relationship between the clock supplied by the HS_CLK pin (27 MHz) and the clock supplied to the CPU core and internal peripheral I/O is as follows: HCLKSEL: 0 — Internal clock frequency: 54 MHz — PLL operation: Multiplied by 2 HCLKSEL: 1 — Internal clock frequency: Clock stops. — PLL operation: PLL operation stops.	–	I	–

(9) Power supply, ground, and others

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
$3.3V_{DD}$	5, 31, 52, 63, 78, 95, 127, 140, 166, 187	–	3.3 V power supply. Supplies a positive voltage of 3.3 V to the I/O pins of the 3.3 V interface.	–	–	–
$2.5V_{DD}$	14, 67, 118, 170	–	2.5 V power supply. Supplies a positive voltage of 2.5 V to the respective internal blocks.	–	–	–
2.5GND	39, 91, 144, 195	–	Ground. These are ground pins. Connect all GND pins to a common ground.	–	–	–
3.3GND	9, 35, 56, 68, 82, 99, 131, 148, 173, 188					
$PLLAV_{DD}$	199	–	Analog power supply to multiplication circuit. Supplies a positive analog voltage to the PLL. Supply 2.5 V to this pin.	–	–	–
PLLAGND	200	–	Analog ground for multiplication circuit. Analog ground pin for PLL.	–	–	–
$PLLDV_{DD}$	198	–	Digital power supply to multiplication circuit. Supplies a positive digital voltage to the PLL. Supply 2.5 V to this pin.	–	–	–
PLLDGND	201	–	Digital ground for multiplication circuit. Digital ground pin for PLL.	–	–	–
IC(L)	203, 205 to 207	–	Internally connected pins Directly connect these pins to ground.	–	–	–
IFIROME	208	I	Internal ROM/external ROM select input 0: External ROM mode 1: Internal ROM mode	–	I	–

1.2 Connection of Unused Pins

The following table shows how to connect unused pins.

Table 1-1. Connection of Unused Pins (1/2)

Pin Name	I/O	Interface	Recommended Connection of Unused Pin
PHY_D[7:0]	I/O	I/O Buffer (LVTTL) in 9 mA With Bus Holder	Connect these pins to V_{DD} or GND via a resistor.
CTL[1:0]			
SCLK	I	I/O Buffer (LVTTL) with bus holder	
LREQ	O	3-state Output Buffer (LVTTL) 9 mA	Leave open
LPS	O	Output Buffer (LVTTL) 9 mA	
LINKON	I	Input Buffer (LVTTL)	Connect these pins to V_{DD} or GND via a resistor.
STREAM1[7:0]	I/O	I/O Buffer (LVTTL) 6 mA	
PACKETEN1			
TSERROR1			
TSRW1			
SYNC1			
STREAM2[7:0]			
PACKETEN2			
TSERROR2			
TSRW2			
SYNC2			
TSSUB1			
TSSUB2	O	Output Buffer (LVTTL) 6 mA	Leave open
P3[4:0]	I/O	I/O Buffer (LVTTL) Schmitt in 6 mA	Connect these pins to V_{DD} or GND via a resistor.
P40/SO			
P41/SI			
P42/SCK			
P43/TXD			
P44/RXD			
P45/SCS			
A[17:1]	O	I/O Buffer (LVTTL) 6 mA	
RDZ	O	Output Buffer (LVTTL) 6 mA	Leave open
WRZ			
D[15:0]	I/O	I/O Buffer (LVTTL) 6 mA	Connect these pins to V_{DD} or GND via a resistor.
AD[10:1]	I	Input Buffer (LVTTL)	
PSSEL[1:0]			
CS			
RWZ			
IOR			
DMAACK/SIO_CNTI			

Table 1-1. Connection of Unused Pins (2/2)

Pin Name	I/O	Interface	Recommended Connection of Unused Pin
INT	O	Output Buffer (LVTTL) 6 mA	Leave open
IOCHRDY			
DMAREQ/SIO_CNTO			
P_D[15:0]	I/O	I/O Buffer (LVTTL) 9 mA	Connect these pins to V_{DD} or GND via a resistor.
IFIROME	I	Input Buffer (LVTTL)	–
HS_CLK			
HCLKSEL			
RESETB	I	Output Buffer (LVTTL) Schmitt	

4.2.3 IC7802: uPD78F0988A

DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78F0988A, 78F0988A(A)

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD78F0988A and 78F0988A(A) are products in the μPD780988 Subseries in the 78K/0 Series that have flash memory in the place of the internal ROM of the μPD780988. Flash memory can be written or erased electrically with the device mounted on the board. Therefore, the μPD78F0988A and μPD78F0988A(A) are ideal for evaluation in system development, small-scale production, or systems likely to be upgraded frequently.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780988 Subseries User's Manual: U13029E
78K/0 Series Instruction User's Manual: U12326E

FEATURES

- Pin-compatible with mask ROM version (except V_{PP} pin)
- Flash memory: 60 KB[Note 1]
- Internal high-speed RAM: 1024 bytes
- Internal expansion RAM: 1024 bytes[Note 2]
- Operable in the same supply voltage range as the mask ROM version (V_{DD} = 4.0 to 5.5 V)

Notes 1. The capacity of the flash memory can be changed with the internal memory size switching register (IMS).
2. The capacity of the internal expansion RAM can be changed with the internal expansion RAM size switching register (IXS).

Remark For the differences between the flash memory versions and the mask ROM versions, refer to **1. DIFFERENCES BETWEEN μPD78F0988A AND MASK ROM VERSIONS.**

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD78F0988ACW	64-pin plastic SDIP (19.05 mm (750))	Standard (for general electrical equipment)
μPD78F0988AGC-AB8	64-pin plastic QFP (14 × 14)	Standard (for general electrical equipment)
μPD78F0988AGC-8BS	64-pin plastic LQFP (14 × 14)	Standard (for general electrical equipment)
μPD78F0988AGC(A)-AB8	64-pin plastic QFP (14 × 14)	Special (for high-reliability electrical equipment)
μPD78F0988AGC(A)-8BS	64-pin plastic LQFP (14 × 14)	Special (for high-reliability electrical equipment)

For details of the quality grade and its application fields, refer to **Quality Grades on NEC Semiconductor Devices (C11531E)**.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

Document No. U15801EJ1V0DS00 (1st edition)
Date Published October 2001 N CP(K)
Printed in Japan

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OVERVIEW OF FUNCTIONS

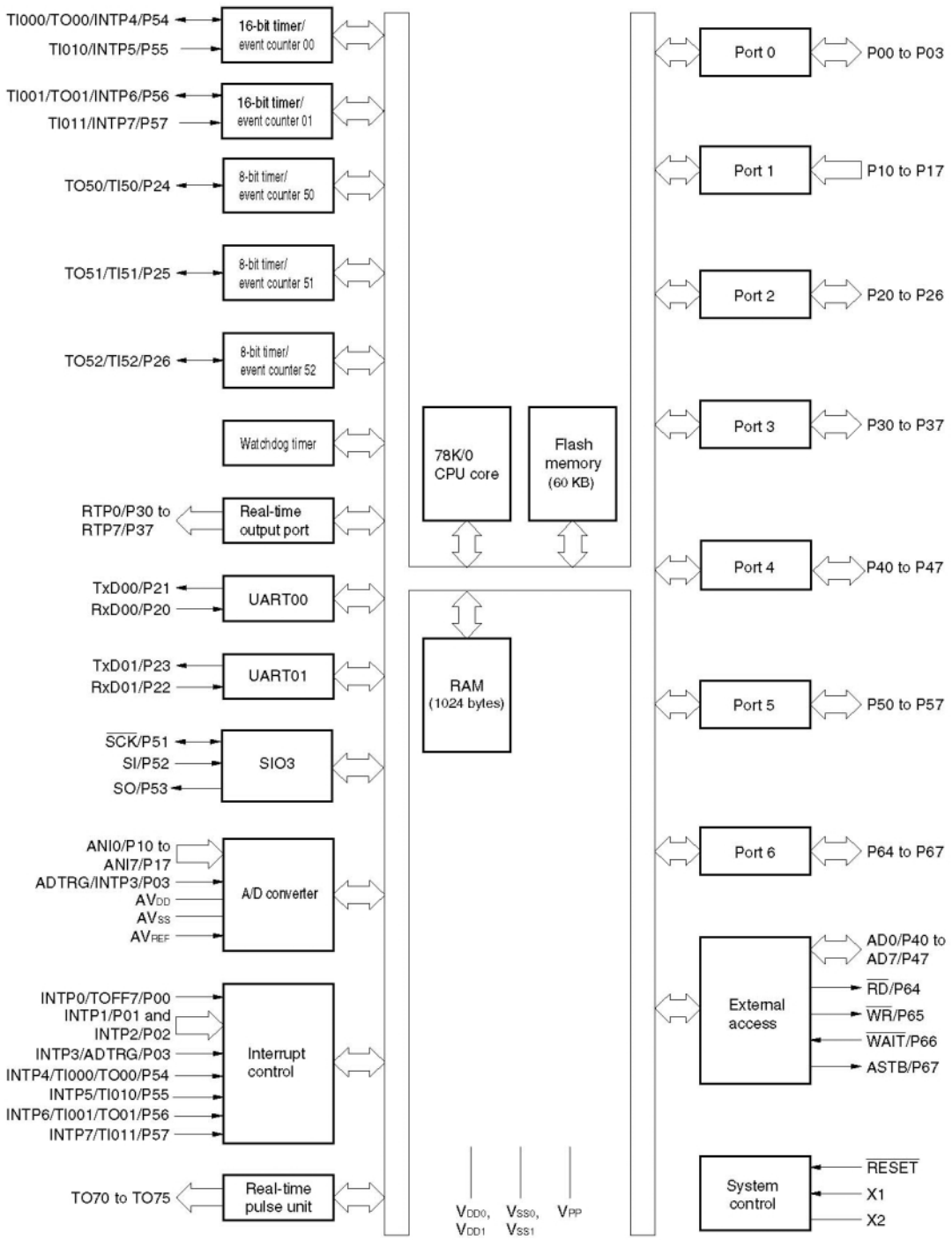
Item		Function
Internal memory	Flash memory	60 KB[Note 1]
	High-speed RAM	1024 bytes
	Expansion RAM	1024 bytes[Note 2]
Memory space		64 KB
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction cycle		On-chip instruction execution time variable function 0.24 μs/0.48 μs/0.96 μs/1.9 μs/3.8 μs (@ 8.38 MHz operation with system clock)
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports		Total: 47 • CMOS inputs: 8 • CMOS I/O: 39
Real-time output ports		• 8 bits × 1 or 4 bits × 2 • 6 bits × 1 or 4 bits × 1
A/D converter		• 10-bit resolution × 8 channels • Power supply voltage: AV_{DD} = 4.0 to 5.5 V
Serial interface		• UART mode: 2 channels • 3-wire serial I/O mode: 1 channel
Timer		• 16 bit timer/event counter: 2 channels • 8-bit timer/event counter: 3 channels • 10-bit inverter control timer: 1 channel • Watchdog timer: 1 channel
Timer output		11 (general-purpose outputs: 5, inverter control outputs: 6)
Vectored interrupt sources	Maskable	Internal: 16, external: 8
	Non-maskable	Internal: 1
	Software	1
Power supply voltage		V_{DD} = 4.0 to 5.5 V
Operating ambient temperature		T_A = −40 to +85°C
Package		• 64-pin plastic SDIP (19.05 mm (750))[Note 3] • 64-pin plastic QFP (14 × 14) • 64-pin plastic LQFP (14 × 14)

Notes 1. The capacity of the flash memory can be changed with the internal memory size switching register (IMS).

2. The capacity of the internal expansion RAM can be changed with the internal expansion RAM size switching register (IXS).

3. Standard quality grade products only.

BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0 4-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting.	Input	INTP0/TOFF7
P01				INTP1
P02				INTP2
P03				INTP3/ADTRG
P10 to P17	Input	Port 1 8-bit input only port	Input	ANI0 to ANI7
P20	I/O	Port 2 7-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting.	Input	RxD00
P21				TxD00
P22				RxD01
P23				TxD01
P24				TI50/TO50
P25				TI51/TO51
P26				TI52/TO52
P30 to P37	I/O	Port 3 8-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting.	Input	RTP0 to RTP7
P40 to P47	I/O	Port 4 8-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting.	Input	AD0 to AD7
P50	I/O	Port 5 8-bit I/O port Input/output can be specified in 1-bit units. LEDs can be driven directly. Use of an on-chip pull-up resistor can be specified by software setting.	Input	—
P51				$\overline{SCK}$
P52				SI
P53				SO
P54				INTP4/TI000/TO00
P55				INTP5/TI010
P56				INTP6/TI001/TO01
P57				INTP7/TI011
P64	I/O	Port 6 4-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting.	Input	$\overline{RD}$
P65				$\overline{WR}$
P66				$\overline{WAIT}$
P67				ASTB

3.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P00/TOFF7
INTP1			Input	P01
INTP2			Input	P02
INTP3			Input	P03/ADTRG
INTP4			Input	P54/TI000/TO00
INTP5			Input	P55/TI010
INTP6			Input	P56/TI001/TO01
INTP7			Input	P57/TI011
TI50	Input	External count clock input to 8-bit timer/event counter 50	Input	P24/TO50
TI51		External count clock input to 8-bit timer/event counter 51	Input	P25/TO51
TI52		External count clock input to 8-bit timer/event counter 52	Input	P26/TO52
TI000		External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture register (CR000, CR010) of 16-bit timer/event counter 00	Input	P54/INTP4/TO00
TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00	Input	P55/INTP5
TI001		External count clock input to 16-bit timer/event counter 01 Capture trigger input to capture register (CR001, CR011) of 16-bit timer/event counter 01	Input	P56/INTP6/TO01
TI011		Capture trigger input to capture register (CR001) of 16-bit timer/event counter 01	Input	P57/INTP7
TO50	Output	8-bit timer/event counter 50 output	Input	P24/TI50
TO51		8-bit timer/event counter 51 output	Input	P25/TI51
TO52		8-bit timer/event counter 52 output	Input	P26/TI52
TO00		16-bit timer/event counter 00 output	Input	P54/INTP4/TI000
TO01		16-bit timer/event counter 01 output	Input	P56/INTP6/TI001
RTP0 to RTP7	Output	Real-time output port that outputs pulses in synchronization with trigger signals outputs from the real-time pulse unit	Input	P30 to P37
TxD00	Output	Asynchronous serial interface serial data output	Input	P21
TxD01			Input	P23
RxD00	Input	Asynchronous serial interface serial data input	Input	P20
RxD01			Input	P22
$\overline{SCK}$	I/O	Serial interface serial clock input/output	Input	P51
SI	Input	Serial interface serial data input	Input	P52
SO	Output	Serial interface serial data output	Input	P53
ANI0 to ANI7	Input	A/D converter analog input	Input	P10 to P17
ADTRG	Input	External trigger signal input to the A/D converter	Input	P03/INTP3
TO70 to TO75	Output	Timer output for the 3-phase PWM inverter control	Hi-Z	–
TOFF7	Input	Timer output (TO70 to TO75) stop external input	Input	P00/INTP0
AD0 to AD7	I/O	Address/data bus for expanding memory externally	Input	P40 to P47
$\overline{RD}$	Output	Strobe signal output for reading from external memory	Input	P64
$\overline{WR}$		Strobe signal output for writing to external memory	Input	P65
$\overline{WAIT}$	Input	Wait insertion at external memory access	Input	P66
ASTB	Output	Strobe output that externally latches address information output to ports 4 and 5 to access external memory	Input	P67
AV_{REF}	Input	A/D converter reference voltage input	–	–
AV_{DD}	–	A/D converter analog power supply	–	–

3.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
AV_{SS}	–	A/D converter ground potential	–	–
$\overline{RESET}$	Input	System reset input	–	–
X1	Input	Connecting crystal resonator for system clock oscillation	–	–
X2	–		–	–
V_{DD0}	–	Positive power supply for ports	–	–
V_{SS0}	–	Ground potential for ports	–	–
V_{DD1}	–	Positive power supply except for ports	–	–
V_{SS1}	–	Ground potential except for ports	–	–
V_{PP}	–	High-voltage application during program write/verify. In the normal operation mode, connect directly to V_{SS0}.	–	–

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.
For the I/O circuit configuration of each type, refer to Figure 3-1.

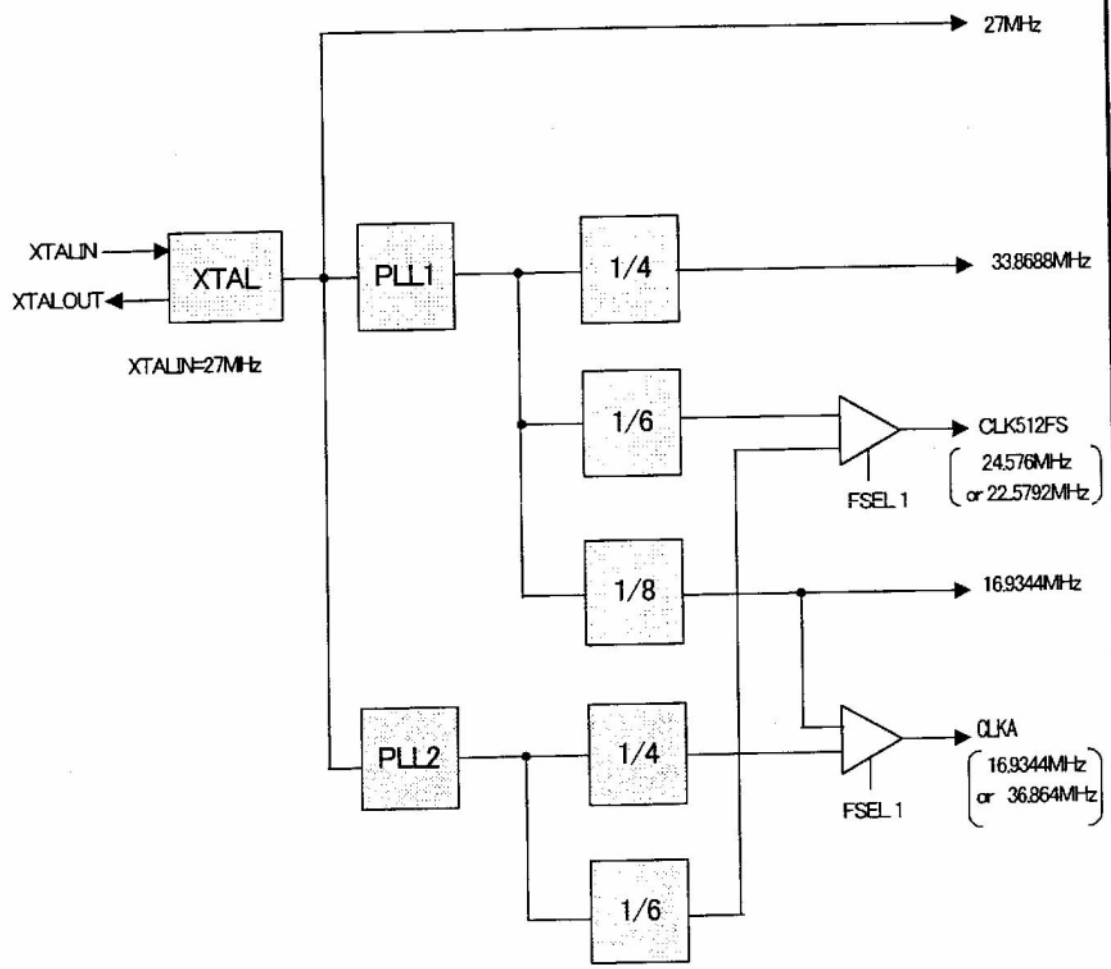
Table 3-1. Types of Pin I/O Circuits

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0/TOFF7	8-C	I/O	Input: Independently connect to V_{SS0} via a resistor. Output: Leave open
P01/INTP1			
P02/INTP2			
P03/INTP3/ADTRG			
P10/ANI0 to P17/ANI7	25	Input	Independently connect to V_{DD0} or V_{SS0} via a resistor.
P20/RxD00	8-C	I/O	Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P21/TxD00	5-H		
P22/RxD01	8-C		
P23/TxD01	5-H		
P24/TI50/TO50	8-C		
P25/TI51/TO51			
P26/TI52/TO52			
P30/RTP0 to P37/RTP7	5-H		
P40/AD0 to P47/AD7			
P50			
P51/$\overline{SCK}$	8-C		
P52/SI	5-H		
P53/SO			
P54/INTP4/TI000/TO00			
P55/INTP5/TI010			
P56/INTP6/TI001/TO01			
P57/INTP7/TI011			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
TO70 to TO75	4	Output	Leave open.
$\overline{RESET}$	2	Input	–
AV_{DD}	–	–	Connect to V_{DD0}.
AV_{REF}			Connect to V_{SS0}.
AV_{SS}			
V_{PP}			Connect directly to V_{SS0}.

4.2.4 IC7605: BU2288FV

ROHM Products semiconductor IC Type BU2288FV Page 2/7

Block Diagram



FSEL1	CLK512FS	CLKA
OPEN	22.5792MHz	16.9344MHz
L	24.576MHz	36.864MHz

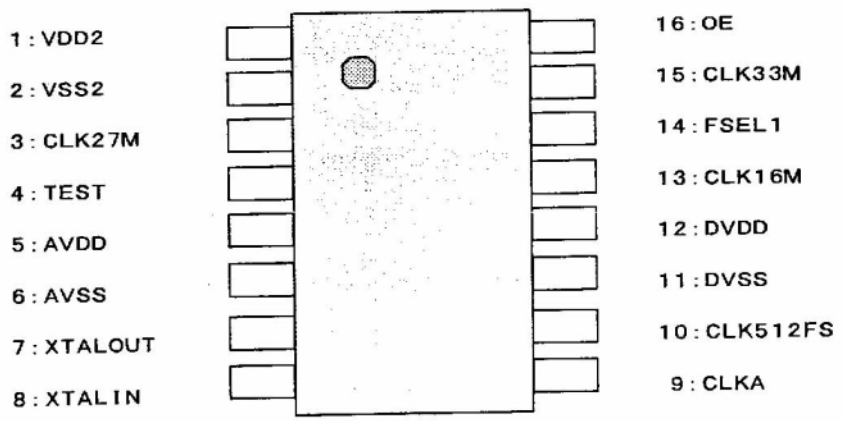
Fig. −1

Date 5/Sep./'00 Specification

ROHM CO., LTD. Specification No. TSZ02201-BU2288FV-1-2

Explanation for terminal function

PIN No.	PIN NAME	FUNCTION
1	VDD2	Digital VDD for 27MHz clock output
2	VSS2	Digital GND for 27MHz clock output
3	CLK27M	27MHz clock output
4	TEST	Output for test
5	AVDD	Analog VDD
6	AVSS	Analog GND
7	XTALOUT	Standard crystal output
8	XTALIN	Standard crystal input
9	CLKA	clock output (FSEL1=Open:16.9344MHz, FSEL1=L:36.864MHz)
10	CLK512FS	clock output (FSEL1=Open:22.5792MHz, FSEL1=L:24.576MHz)
11	DVSS	Digital GND
12	DVDD	Digital VDD
13	CLK16M	16.9344MHz clock output
14	FSEL1	Output select :with pull-up Open:16.9344MHz(9pin), 22.5792MHz(10pin) L :36.864MHz(9pin), 24.576MHz(10pin)
15	CLK33M	33.8688MHz clock output
16	OE	Output enable(open:enable, L:disable) :with pull-up



4.2.5 IC7604: BA7082F

ROHM | Product: Semiconductor IC | Type: BA7082F | Page 1/8

STRUCTURE Silicon Monolithic Integrated Circuits

TYPE BA7082F

PACKAGE OUTLINE Fig-1 (Plastic molded)

BLOCK DIAGRAM Fig-2 (Block Diagram)

Function VCO with sencitivity adjustment function and 1/2 Frequency demultiplier.

Features
- It is possible to set up frequency by external parts (Resistor and Capacitor).
- It is possible to set up frequency sencitivity by added resistor.Because it has a built-in amplifer for sencitivity adjustment.
- It is possible to change output by SW.Because it has 1/2 Frequency demultiplier.
- It has a pin to adjust f_o.
- Built-in three switching circuits for changing Frequency sensitivity.

Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Supply voltage	$V_{cc\ max}$	7.0	V
Power dissipation	Pd	※ 500	mW
Operating temp range	Topr	−20~70	℃
Storage temp range	Tstg	−55~125	℃

※ at put on Glass epxy PCB (50×50mm², t=1.6mm)
To use at temperatures higher than Ta=25℃, derate 5mW/℃.

Operating suypply voltage range	Vcc	4.5~5.5	V

◎ This product is not designed for protection against radioactive rays.

ROHM assumes no responsibility for the use of any circuits described herein,conveys no license under any patent or other right,and makes no representations that the circuits are free from patent infringement.

Design	Check	Approval	Date	Specification
K. Ohtsuka	M. Matano	'95. Mar. 6 R. Hayashi	'95/ 2/28	Rev. A
			ROHM CO., LTD.	Specification No. TSZ02201-BA7082F-1-2

A4 3.7 (1×100×50) S

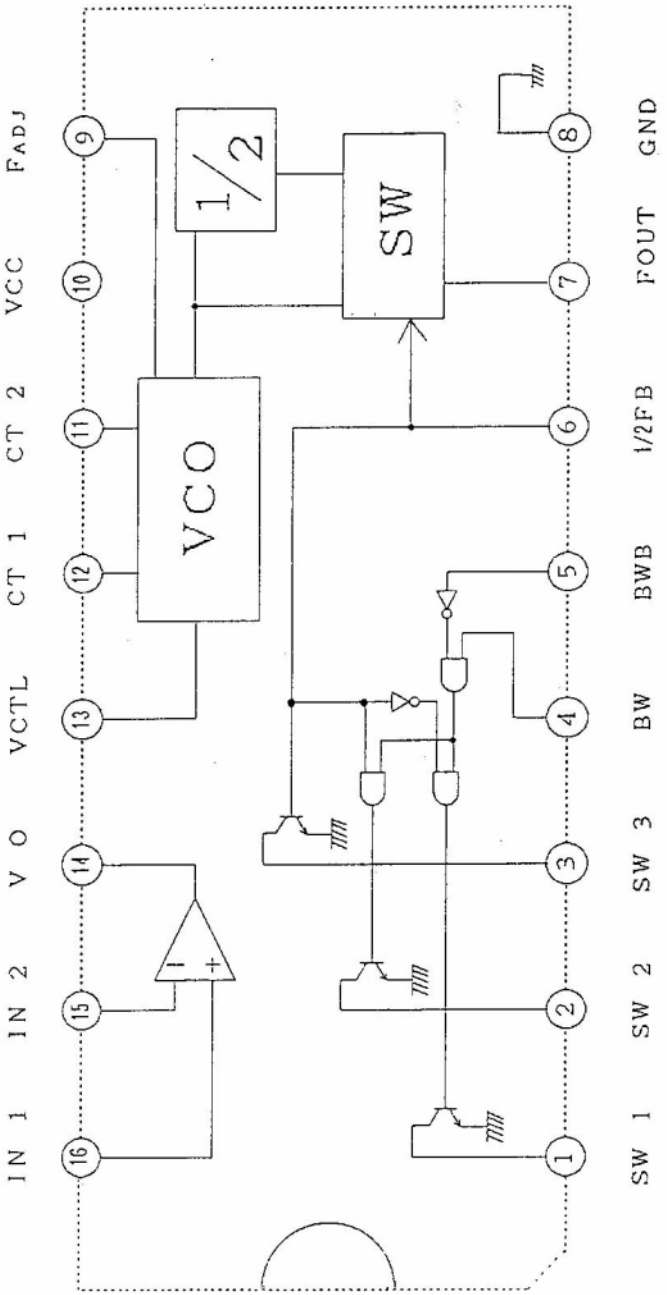
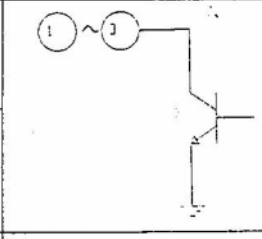
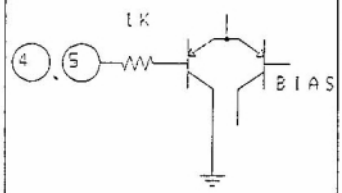
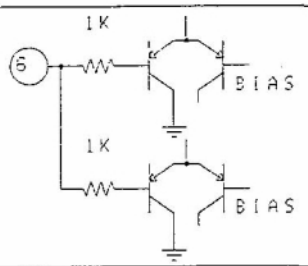
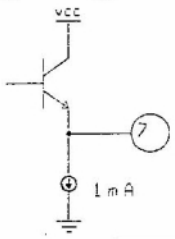
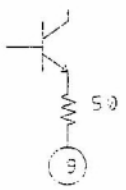


Fig-2 Block diagram

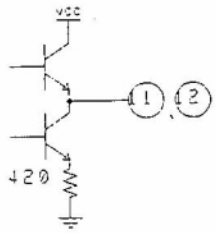
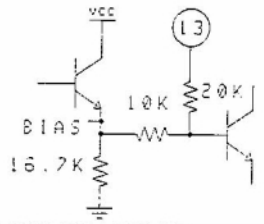
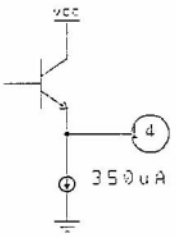
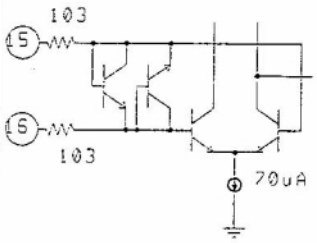
Date '95/ 2/28	Specification
ROHM CO., LTD.	Specification No. TSZ02201-BA7082F-1-2

ROHM | Products: Semiconductor IC | Type: BA7082F | Page: 7/8

No.	Symbol	IN	OUT	normal DC Voltage	Internal pin configuration	Description
1	SW1			L 0.1V		Pin 1-3 are output pins at LOGIC parts for adjustment frequency sencitivity. These pins are open collector output.
2	SW2		O	—		
3	SW3			OPEN 5V		
4	BW					Pin 4,5 are input pins at logic parts for adjustment frequency sencitivity.
5	BWB					
6	1/2FB	O		—		Pin 6 is input pin at LOGIC parts for adjustment frequency sencitivity and changing 1/2 Frequency demultuplier. "H" is through output. and "L" is 1/2 Frequency demultiplier output.
7	Fout		O	3.6V		VCO Output.
8	GND	—	—	0V	GND	GND
9	FADJ	—	—	2.5V		Pin9 is a pin to adjust f0. It is possible to adjust f0 by added resistor(RADJ). If Value of RADJ down, oscillation frequency up. (Use to RADJ>22kΩ).

Date '95/ 2/28	Specification
ROHM CO., LTD.	Specification No. TSZ02201-BA7082F-1-2

ROHM	Products: Semiconductor IC	Type: BA7082F	Page: 8/8

No.	Symbol	IN	OUT	normal DC Voltag	Internal pin configuration	Description
10	VCC	–	–	5.0V	VCC	VCC
11	CT2	–	–	1.9V		Pin 11,12 are added capasitor pins for oscillation. Use to added capacitor betweeen CT1 and CT2. If value of capacitor down, oscillation frequency up.
12	CT1					
13	VCTL	○		2.5V		Pin13 is control pin for VCO. A regular this pin connect pin14(VO).
14	VO		○	2.5V		Pin14 is output pin at Amlplfier for sencitivity ajdustment. Adjustment amplifier GAIN by added resistor.
15	IN2	○		2.5V		Pin15,16 are input pins at amplifier for sencitivity adjustment. In1 ; normal input In2 ; inversion input
16	IN1					

Date '95/ 2/28	Specification
ROHM CO., LTD.	Specification No. TSZ02201-BA7082F-1-2

4.3 List of Abbreviations

Divio 1.8 Board
2V5
+2V5 Power supply for Link+Codec IC7431
3V3
+3V3 Power supply
3V3_A
+3V3 Analog power supply for PHY IC7400
3V3_D
+3V3 Digital power supply for PHY IC7400
3V3_DLY
+3V3 Power supply for IC7500
3V3_LINK
+3V3 Power supply for Link+Codec IC7431
3V3_F
+3V3 Power supply for optional Flash memory IC7432
3V3_RAM
+3V3 Power supply for SDRAM IC7430
3V3_uP
+3V3 Power supply for Micro-controller IC7802
3V3_32kHz
+3V3 Power supply for audio format adaptation circuitry IC7507 & IC7508
3V3_AC
+3V3 Power supply for audio system clock generator IC7605 & IC7606
+5V
+5V Power supply
5V_PLL
+5V Power supply for VCO of audio PLL IC7604
A(1:17)
Flash adress lines of uPD72893
A_MUTE
Audio Mute
ABCK
Audio Bit Clock
AD(1:10)
Address bus lines for Host I/F of Link+Codec IC7431
AEMP1
PCM1 emphasis ON/OFF for PCM1 output
AFS1
Audio sampling frequency indication signal
ALRCLK
Audio Word Select
AMCLK44
11,2896MHz (=256*44.1kHz) audio master clock signal for 44.1kHz audio
AMCLK48
12,288MHz (=256*48kHz) audio master clock signal for 32kHz and 48kHz audio
APWM
PWM signal for audio PLL
BUFENn_AUD
Buffer Enable Audio
BUFENn_VID
Buffer Enable Video
CLK27M_CON
27MHz Clock to Digital Board
CS
Parallel interface chip select input of Link+Codec IC7431
CTL(0:1)
Link interface control lines
CTSN
Clear to Send
D(0:15)
Flash data lines of Link+Codec IC7431
DV_STATUS
Interupt pin for reading DV-status
HS_CLK
Video clock input of Link+Codec IC7431
INT
Interrupt request output of Link+Codec IC7431 (input to Micro-Controller)
IOR
Parallel interface IO read control input of Link+Codec IC7431
ISPN
In System Programming signal (used for programming IC7802)
LKON
Link-on signal output
LPS
Link power status input
LREQ
Link request input
MA(0:10)
SDRAM adress lines of Link+Codec IC7431
MCAS
SDRAM column address strobe signal
MCLK
SDRAM clock signal
MD(0:15)SDRAM data lines of Link+Codec IC7431
MRAS
SDRAM row-address strobe signal
MWE
SDRAM write enable signal
PCM1
Audio Serial Data Output of Link+Codec IC7431
PCM1_NEW
"MSB justified" to I2S converted audio serial data; audio serial data input of audio DAC UDA1334A
PD(0:15)
Data bus lines for Host I/F of Link+Codec IC7431
PHY_D(0:7)
Data bus connection between PHY and LINK device
RESETn
DVIO board reset
RESET_FM
Reset signal driven by Flashmaster programming device
RESTB
Reset input of Link+Codec IC7431
RTSN
Request to Send
RWZ
Parallel interface read/write control input of Link+Codec IC7431
RXD
Receive Data
SCLK
Link control output clock
TXD
Transmit Data
VPP
+10V switchable programming voltage of microcontroller
YUV(0:7)
Digital Video

5. Spare parts list

DVIO 1.8 PWB

Various

1400	2422 543 01115	RES XTL SM 24M576 12P CX-11F R
1500	2422 025 17084	CON BM V 60P F 0.80 179161 R
1501	2422 025 16543	CON BM H 4P M 2.00 PH SMD R
1502	2422 086 11075	FUSE SM F 750MA 125V UL R
1800	2422 543 89022	RES XTL SM 6M000 20P CX-5F R
1901	2422 025 17106	CON BM H 4P F 0.8 IEEE R
1903	2422 025 16542	CON BM H 2P M 2.00 PH SMD R

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2400	2238 586 59812	0603 50V 100NP80M
2401	3198 017 41050	0603 10V 1µF COL R
2402	4822 126 14506	270pF 5% 50V 0603
2403	4822 124 80151	47µF 16V
2404	2238 586 59812	0603 50V 100NP80M
2405	2238 586 59812	0603 50V 100NP80M
2406	2238 586 59812	0603 50V 100NP80M
2407	2238 586 59812	0603 50V 100NP80M
2408	2238 586 59812	0603 50V 100NP80M
2412	4822 122 33741	10pF 10% 50V
2413	4822 122 33741	10pF 10% 50V
2415	4822 124 80151	47µF 16V
2416	2238 586 59812	0603 50V 100NP80M
2417	2238 586 59812	0603 50V 100NP80M
2418	2238 586 59812	0603 50V 100NP80M
2419	2238 586 59812	0603 50V 100NP80M
2420	2238 586 59812	0603 50V 100NP80M
2431	4822 124 80151	47µF 16V
2432	2238 586 59812	0603 50V 100NP80M
2433	2238 586 59812	0603 50V 100NP80M
2434	2238 586 59812	0603 50V 100NP80M
2435	2238 586 59812	0603 50V 100NP80M
2436	2238 586 59812	0603 50V 100NP80M
2437	2238 586 59812	0603 50V 100NP80M
2438	2238 586 59812	0603 50V 100NP80M
2439	2238 586 59812	0603 50V 100NP80M
2440	2238 586 59812	0603 50V 100NP80M
2441	2238 586 59812	0603 50V 100NP80M
2442	2238 586 59812	0603 50V 100NP80M
2443	2238 586 59812	0603 50V 100NP80M
2444	2238 586 59812	0603 50V 100NP80M
2445	2238 586 59812	0603 50V 100NP80M
2446	2238 586 59812	0603 50V 100NP80M
2447	2238 586 59812	0603 50V 100NP80M
2449	2238 586 59812	0603 50V 100NP80M
2450	4822 124 23002	10µF 16V
2451	2238 586 59812	0603 50V 100NP80M
2452	2238 586 59812	0603 50V 100NP80M
2453	2238 586 59812	0603 50V 100NP80M
2454	2238 586 59812	0603 50V 100NP80M
2455	2238 586 59812	0603 50V 100NP80M
2456	2238 586 59812	0603 50V 100NP80M
2501	2238 586 59812	0603 50V 100NP80M
2502	2238 586 59812	0603 50V 100NP80M
2503	2238 586 59812	0603 50V 100NP80M
2504	2238 586 59812	0603 50V 100NP80M
2505	2238 586 59812	0603 50V 100NP80M
2506	4822 124 80151	47µF 16V
2507	4822 124 80151	47µF 16V
2508	2238 586 59812	0603 50V 100NP80M
2512	2238 586 59812	0603 50V 100NP80M
2513	2238 586 59812	0603 50V 100NP80M
2514	4822 124 80151	47µF 16V
2520	2238 586 59812	0603 50V 100NP80M
2521	4822 124 80151	47µF 16V
2522	4822 124 80151	47µF 16V
2523	5322 126 11583	10nF 10% 50V 0603
2524	5322 126 11583	10nF 10% 50V 0603
2525	4822 124 80151	47µF 16V
2526	2238 586 59812	0603 50V 100NP80M
2527	2238 586 59812	0603 50V 100NP80M
2528	2238 586 59812	0603 50V 100NP80M
2529	2238 586 59812	0603 50V 100NP80M
2534	2238 586 59812	0603 50V 100NP80M
2600	2238 586 59812	0603 50V 100NP80M
2601	4822 124 23002	10µF 16V
2602	3198 017 44740	0603 10V 470nF COL
2603	2238 586 59812	0603 50V 100NP80M
2605	2238 586 59812	0603 50V 100NP80M
2606	3198 016 31020	0603 25V 1nF
2607	2238 586 59812	0603 50V 100NP80M
2608	2238 586 59812	0603 50V 100NP80M
2609	2238 586 59812	0603 50V 100NP80M
2610	2238 586 59812	0603 50V 100NP80M
2611	2238 586 59812	0603 50V 100NP80M
2612	2238 586 59812	0603 50V 100NP80M
2613	2238 586 59812	0603 50V 100NP80M
2614	3198 017 44740	0603 10V 470nF COL
2617	2238 586 59812	0603 50V 100NP80M
2618	2238 861 18229	50V 22P PM1 R
2801	4822 126 11669	27pF
2802	4822 126 11669	27pF
2803	2238 586 59812	0603 50V 100NP80M
2804	2238 586 59812	0603 50V 100NP80M
2805	4822 124 80151	47µF 16V
2806	2238 586 59812	0603 50V 100NP80M
2807	4822 124 80151	47µF 16V
2808	2238 586 59812	0603 50V 100NP80M
2809	2238 586 59812	0603 50V 100NP80M
2810	2238 586 59812	0603 50V 100NP80M
2812	2238 586 59812	0603 50V 100NP80M
2813	2238 586 59812	0603 50V 100NP80M
2814	5322 124 41945	22µF 20% 35V
2816	2238 586 59812	0603 50V 100NP80M
2818	2238 586 59812	0603 50V 100NP80M
2820	2238 586 59812	0603 50V 100NP80M
2822	3198 016 31020	0603 25V 1nF

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3400	4822 051 30103	10k 5% 0.062W
3401	2322 734 65609	RST SM 0805 RC12H 56Ω PM1 R
3402	2322 734 65609	RST SM 0805 RC12H 56Ω PM1 R
3403	4822 117 12139	22Ω 5% 0.062W
3404	2322 734 65609	RST SM 0805 RC12H 56Ω PM1 R
3405	2322 734 65609	RST SM 0805 RC12H 56Ω PM1 R
3406	2322 704 65102	RST SM 0603 RC22H 5k1 PM1
3407	4822 051 30103	10k 5% 0.062W
3408	4822 117 13632	100k 1% 0603 0.62W
3409	4822 117 12902	8k2 1% 0.063W 0603
3410	4822 117 12139	22Ω 5% 0.062W
3413	4822 117 12139	22Ω 5% 0.062W
3414	4822 117 12139	22Ω 5% 0.062W
3415	4822 117 12139	22Ω 5% 0.062W
3416	4822 117 12139	22Ω 5% 0.062W
3417	4822 117 12139	22Ω 5% 0.062W
3418	4822 117 12139	22Ω 5% 0.062W
3419	4822 117 12139	22Ω 5% 0.062W
3420	4822 117 12139	22Ω 5% 0.062W
3421	4822 117 12139	22Ω 5% 0.062W
3422	4822 117 12139	22Ω 5% 0.062W
3423	4822 117 12139	22Ω 5% 0.062W
3424	4822 117 12139	22Ω 5% 0.062W
3425	4822 051 30103	10k 5% 0.062W
3426	4822 051 30103	10k 5% 0.062W
3427	4822 051 30103	10k 5% 0.062W
3428	4822 051 30103	10k 5% 0.062W
3429	4822 051 30103	10k 5% 0.062W
3430	4822 051 30103	10k 5% 0.062W
3431	4822 051 30103	10k 5% 0.062W
3432	4822 051 30103	10k 5% 0.062W
3433	4822 051 30103	10k 5% 0.062W
3434	4822 051 30103	10k 5% 0.062W
3435	4822 051 30103	10k 5% 0.062W
3436	4822 051 30103	10k 5% 0.062W
3437	4822 051 30103	10k 5% 0.062W
3438	4822 051 30103	10k 5% 0.062W
3439	4822 051 30103	10k 5% 0.062W
3440	4822 051 30103	10k 5% 0.062W
3441	4822 051 30103	10k 5% 0.062W
3442	4822 051 30103	10k 5% 0.062W
3443	4822 051 30103	10k 5% 0.062W
3444	4822 051 30103	10k 5% 0.062W
3445	4822 051 30103	10k 5% 0.062W
3446	4822 051 30103	10k 5% 0.062W
3447	4822 051 30103	10k 5% 0.062W
3448	4822 051 30103	10k 5% 0.062W
3449	4822 051 30103	10k 5% 0.062W
3450	4822 051 30103	10k 5% 0.062W
3451	4822 051 30103	10k 5% 0.062W
3452	4822 051 30103	10k 5% 0.062W
3453	4822 051 30102	1k 5% 0.062W
3454	4822 051 30103	10k 5% 0.062W
3455	4822 051 30103	10k 5% 0.062W
3456	4822 051 30103	10k 5% 0.062W
3457	4822 051 30103	10k 5% 0.062W
3458	4822 051 30103	10k 5% 0.062W
3459	4822 051 30103	10k 5% 0.062W
3460	4822 051 30103	10k 5% 0.062W
3461	4822 117 12925	47k 1% 0.063W 0603
3462	4822 051 30103	10k 5% 0.062W
3463	4822 051 30103	10k 5% 0.062W
3464	4822 051 30103	10k 5% 0.062W
3465	4822 051 30103	10k 5% 0.062W
3466	4822 051 30103	10k 5% 0.062W
3467	4822 051 30103	10k 5% 0.062W
3468	4822 051 30103	10k 5% 0.062W
3469	4822 051 30103	10k 5% 0.062W
3470	4822 051 30103	10k 5% 0.062W
3471	4822 051 30103	10k 5% 0.062W
3472	4822 051 30102	1k 5% 0.062W
3473	4822 051 30103	10k 5% 0.062W
3474	4822 051 30102	1k 5% 0.062W
3475	4822 051 30103	10k 5% 0.062W
3476	4822 051 30103	10k 5% 0.062W
3477	4822 051 30103	10k 5% 0.062W
3478	4822 051 30102	1k 5% 0.062W
3481	4822 051 30103	10k 5% 0.062W
3482	4822 051 30103	10k 5% 0.062W
3483	4822 051 30103	10k 5% 0.062W
3484	4822 051 30103	10k 5% 0.062W
3485	4822 051 30103	10k 5% 0.062W
3486	4822 051 30103	10k 5% 0.062W
3487	4822 051 30103	10k 5% 0.062W
3488	4822 051 30103	10k 5% 0.062W
3489	4822 051 30103	10k 5% 0.062W
3490	4822 051 30103	10k 5% 0.062W
3491	4822 051 30103	10k 5% 0.062W
3492	4822 051 30103	10k 5% 0.062W
3493	4822 051 30103	10k 5% 0.062W
3494	4822 051 30103	10k 5% 0.062W
3495	4822 051 30103	10k 5% 0.062W
3496	4822 051 30103	10k 5% 0.062W
3497	4822 051 30103	10k 5% 0.062W
3498	4822 051 30103	10k 5% 0.062W
3499	4822 051 30103	10k 5% 0.062W
3502	4822 051 30479	47Ω 5% 0.062W
3503	4822 051 30479	47Ω 5% 0.062W
3504	4822 051 30479	47Ω 5% 0.062W
3505	4822 051 30479	47Ω 5% 0.062W
3506	4822 051 30479	47Ω 5% 0.062W
3507	4822 051 30479	47Ω 5% 0.062W
3508	4822 051 30479	47Ω 5% 0.062W
3509	4822 051 30479	47Ω 5% 0.062W
3510	4822 051 30479	47Ω 5% 0.062W
3514	4822 051 30479	47Ω 5% 0.062W
3515	4822 051 30479	47Ω 5% 0.062W
3516	4822 051 30479	47Ω 5% 0.062W
3517	4822 051 30101	100Ω 5% 0.062W
3518	4822 051 30101	100Ω 5% 0.062W
3519	4822 117 12891	220k 1% ERJ3Ω
3520	4822 117 12891	220k 1% ERJ3Ω
3530	4822 117 12139	22Ω 5% 0.062W
3531	4822 117 12139	22Ω 5% 0.062W
3532	4822 117 12139	22Ω 5% 0.062W
3533	4822 117 12139	22Ω 5% 0.062W
3534	4822 117 12139	22Ω 5% 0.062W
3535	4822 117 12139	22Ω 5% 0.062W
3536	4822 117 12139	22Ω 5% 0.062W
3537	4822 117 12139	22Ω 5% 0.062W
3538	4822 117 12139	22Ω 5% 0.062W
3539	4822 117 12139	22Ω 5% 0.062W
3540	4822 117 12139	22Ω 5% 0.062W
3541	4822 117 12139	22Ω 5% 0.062W
3542	4822 117 12139	22Ω 5% 0.062W
3543	4822 117 12139	22Ω 5% 0.062W
3544	4822 117 12139	22Ω 5% 0.062W
3545	4822 117 12139	22Ω 5% 0.062W
3546	4822 117 12139	22Ω 5% 0.062W
3547	4822 117 12139	22Ω 5% 0.062W
3548	4822 117 12139	22Ω 5% 0.062W
3549	4822 117 12139	22Ω 5% 0.062W
3550	4822 117 12139	22Ω 5% 0.062W
3551	4822 117 12139	22Ω 5% 0.062W
3552	4822 117 12139	22Ω 5% 0.062W
3553	4822 117 12139	22Ω 5% 0.062W
3554	4822 117 12139	22Ω 5% 0.062W
3555	4822 117 12139	22Ω 5% 0.062W
3556	4822 117 12139	22Ω 5% 0.062W
3557	4822 117 12139	22Ω 5% 0.062W
3558	4822 117 12139	22Ω 5% 0.062W

3559	4822 117 12139	22Ω 5% 0.062W
3560	4822 117 12139	22Ω 5% 0.062W
3561	4822 117 12139	22Ω 5% 0.062W
3562	4822 051 30103	10k 5% 0.062W
3563	4822 117 12917	1Ω 5% 0.062W CASE0603
3564	4822 117 12139	22Ω 5% 0.062W
3600	4822 117 12891	220k 1% ERJ3Ω
3601	4822 117 12917	1Ω 5% 0.062W CASE0603
3602	4822 051 30103	10k 5% 0.062W
3603	4822 117 12917	1Ω 5% 0.062W CASE0603
3605	2120 358 90533	RTRM CER SM 22k H RH03ADC R
3606	4822 117 12706	10k 1% 0.063W CASE0603 RC22H
3607	2322 702 60184	RST SM 0603 RC21 180k PM5 R
3608	4822 117 12891	220k 1% ERJ3Ω
3609	2322 704 65604	RST SM 0603 RC22H 560k PM1 R
3610	2322 704 62003	RST SM 0603 RC22H 20k PM1 R
3610	5322 117 13024	33k 1% 0.063W 0603 RC22H
3612	4822 117 12706	10k 1% 0.063W CASE0603 RC22H
3613	2322 704 65102	RST SM 0603 RC22H 5k1 PM1
3614	4822 117 13632	100k 1% 0603 0.62W
3617	4822 051 30103	10k 5% 0.062W
3618	4822 051 30103	10k 5% 0.062W
3800	4822 051 30331	330Ω 5% 0.062W
3801	4822 051 30103	10k 5% 0.062W
3802	4822 051 30223	22k 5% 0.062W
3803	4822 051 30103	10k 5% 0.062W
3804	4822 051 30103	10k 5% 0.062W
3806	4822 051 30103	10k 5% 0.062W
3807	4822 051 30103	10k 5% 0.062W
3808	4822 051 30008	0Ω jumper
3809	4822 051 30103	10k 5% 0.062W
3810	4822 051 30103	10k 5% 0.062W
3812	4822 051 30103	10k 5% 0.062W
3814	4822 051 30472	4k7 5% 0.062W
3815	5322 117 13047	330Ω 1% 0.063W 0603 RC22H
3816	5322 117 13018	1k0 1% 0.063W 0603 RC22H
3817	4822 051 30103	10k 5% 0.062W
3818	4822 051 30103	10k 5% 0.062W
3819	4822 051 30102	1k 5% 0.062W
3820	4822 117 12925	47k 1% 0.063W 0603
3821	4822 051 30103	10k 5% 0.062W
3822	4822 117 13632	100k 1% 0603 0.62W
3823	5322 117 13018	1k0 1% 0.063W 0603 RC22H
3824	5322 117 13042	3k9 1% 0.063W 0603 RC22H
3825	4822 051 30101	100Ω 5% 0.062W
3826	4822 051 30101	100Ω 5% 0.062W
3827	4822 051 30103	10k 5% 0.062W
3828	4822 051 30101	100Ω 5% 0.062W
3829	4822 117 12925	47k 1% 0.063W 0603
3831	4822 117 13632	100k 1% 0603 0.62W
3832	4822 051 30103	10k 5% 0.062W
3833	4822 051 30103	10k 5% 0.062W
3834	4822 051 30103	10k 5% 0.062W
3835	4822 051 30102	1k 5% 0.062W
3836	4822 051 30472	4k7 5% 0.062W
3837	4822 051 30103	10k 5% 0.062W
3838	4822 051 30102	1k 5% 0.062W
3839	4822 051 30222	2k2 5% 0.062W

5400	4822 157 11499	BLM11P600SPT
5401	4822 157 11499	BLM11P600SPT
5431	4822 157 11499	BLM11P600SPT
5432	4822 157 11499	BLM11P600SPT
5433	4822 157 11499	BLM11P600SPT
5501	4822 157 11499	BLM11P600SPT
5503	4822 157 11499	BLM11P600SPT
5504	4822 157 11499	BLM11P600SPT
5505	4822 157 11499	BLM11P600SPT
5600	4822 157 11499	BLM11P600SPT
5601	4822 157 11499	BLM11P600SPT
5602	4822 157 11499	BLM11P600SPT
5603	4822 157 11499	BLM11P600SPT
5800	4822 157 11499	BLM11P600SPT
5801	4822 157 11499	BLM11P600SPT
5802	4822 157 71593	10µH 10%

6801	9340 548 52115	PDZ5.1B
6802	4822 130 11397	BAS316
6803	4822 130 11397	BAS316
6804	4822 130 11397	BAS316

7400	9322 182 04671	IC SM UPD72852GB-8EU (NEC0) Y
7430	9322 144 59668	IC SM MT48LC1M16A1TG-7S (MRN)R
7431	9322 184 70671	IC SM UPD72893GD-LML (NEC0) Y
7433	9322 142 88668	IC SM LF25CDT (ST00) R
7501	9352 685 96115	IC SM 74LVC1GU04GW (PHSE) R
7505	9352 029 90118	IC SM 74LVT16244BDGG (PHSE) R
7506	9352 668 39118	IC SM UDA1334ATS/N2 (PHSE) R
7507	9351 751 40118	IC SM 74LV74PW (PHSE) R
7508	9352 685 96115	IC SM 74LVC1GU04GW (PHSE) R
7601	2722 171 08709	OSC XTL SM 27MHZ 120P FXO-31 R
7602	9352 456 40115	IC SM 74HCT1G04GW (PHSE) R
7604	9322 186 60668	IC SM BA7082F (RHM0) R
7605	9322 186 59668	IC SM BU2288FV (RHM0) R
7606	9351 751 40118	IC SM 74LV74PW (PHSE) R
7608	9352 685 96115	IC SM 74LVC1GU04GW (PHSE) R
7800	9340 310 30215	PDTC144ET (
7801	9322 186 70668	IC SM LM2931D (ST00) R
7802	3103 607 40011	IC SM UPD78F0988AGC DV91XX0105
7803	3198 010 42310	BC847BW
7804	3198 010 42310	BC847BW
7805	3198 010 42310	BC847BW
7806	9340 310 30215	PDTC144ET (
7807	9352 683 81115	IC SM 74LVC1G32GW (PHSE) R
7808	9340 560 36235	BSH111
7809	9352 683 81115	IC SM 74LVC1G32GW (PHSE) R
7810	3198 010 42320	BC857BW
7811	3198 010 42310	BC847BW